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| | TENTAT | IVE SPECIFICATIONS |
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| | | |
| | Product Type | Power Supply IC for CCD Module |
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| | • | IR3M63U6 |
| | Model No. | IKJWOJOO |
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| , | VTL: 44:: C4: | inne containe 24 mans including the command amounting |
| 7 | | ions contains <u>24</u> pages including the cover and appendix. tive specifications are subject to change to improve characteristics. |
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Engineering Department IV
Opto-Analog Devices Division
Electronic Components Group
SHARP CORPORATION



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 - ·Office electronics
 - •Instrumentation and measuring equipment
 - · Machine tools
 - · Audiovisual equipment
 - ·Home appliances
 - ·Communication equipment other than for trunk lines
 - (2) These contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
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 - Mainframe computers
 - traffic control systems
 - ·Gas leak detectors and automatic cutoff devices
 - •Rescue and security equipment
 - ·Other safety devices and safety equipment, etc.
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- Please direct all queries regarding the products covered herein to a sales representative of the company.



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1. General Description

The Sharp IR3M63U6 is a power supply IC for CCD camera modules. This single chip can simultaneously offer positive and negative output voltages for CCD power supply from a single input, with a buck switching power supply, charge pumps and regulators. Each output can be controlled by CTL input, and its order of priority is determined by internal control not to damage CCDs.

2. Features

- (1) Power supply voltage: 4.5V~10V
- (2) Buck switching power supply: output voltage 3.6V, frequency 1MHz
- (3) Boost / inverting charge pump frequency: 200kHz
- (4) Linear regulator 1: output voltage 3.3V, maximum output current 120mA

150mA (no load on linear regulator 2)

- (5) Linear regulator 2: output voltage 1.8V, maximum output current 50mA
- (6) Boost charge pump + linear regulator

15V / max. 12mA

(7) Inverting charge pump + linear regulator

-8V / max. 2.5mA

- (8) Containing power supply sequence controller
- (9) Containing over-current protection circuits
- (10) P type silicon substrate monolithic IC
- (11) Lead free
- (12) 32-pin VQFN (5.2 mm x 5.2 mm) plastic package
- (13) Not designed or rated as radiation hardened

3. Pin Connections

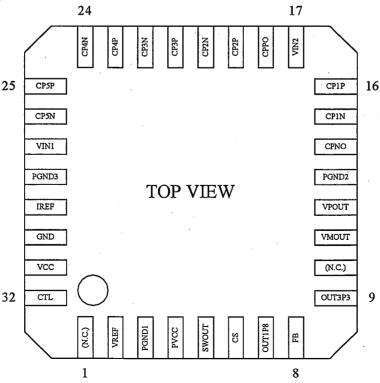


Fig. 1



4. Pin Description

| Pin No. | Pin Name | I/O | Vol./ Vth | Equivalent Circuit | Description |
|------------|------------------|--------------|---------------------------|--------------------|---|
| 32 | CTL | I | 1.5V at Vcc = 5V | CTL O | Control input pin for 1.8V, 3.3V, 15V and -8V outputs. (High: Start; Low: Stop) |
| 2 | VREF | - | 1.25V | GND VREF | Output pin for 1.25V reference voltage. Normally open. |
| 5 | swout | O | | PVcc SWOUT | Output pin for 3.6V buck switching power supply. Connect an inductor and a diode. |
| 6 | CS | I | - | CS O GND | Sense voltage input (high) pin for over-current control of 3.6V power supply. |
| 7 9 | OUT1P8 OUT3P3 | O | - | OUT3P3 OUT1P8 | Output pin for 3.3V / 1.8V regulator. Connect to GND through a capacitor. |
| 11 | VMOUT | 0 | | VREF FB GND VMOUT | Output pin for -8V regulator. Connect to GND through a capacitor. |
| 12 | VPOUT | 0 | - | CPPO VPOUT | Output pin for 15V regulator. Connect to GND through a capacitor. |



| Pin No. Name I/O Vol./ Vth Equivalent Circuit Output capacitor connection pin for charge pump. CPIN CPIN CONNECT TO MINIOR CONNECT TO CONNECT TO CONNECT TO CONNECT A CAPACITOR CAPACI | inverting |
|--|--|
| charge pump. CPNO CPIN CPNO CPNO Connect to GND through a capacitor Flying capacitor 1 negative pin. Connect a connect or connect to con | inverting |
| A Connect a connector from CDINI to C | r for regulating. |
| 15 CP1N Connect a capacitor from CP1N to C | CP1P. |
| Flying capacitor 1 positive pin. Connect a capacitor from CP1P to C PGND PGND | |
| Output capacitor connection pin for boost charge pump. CPPPO CPPPO CPPPO CPPO C | |
| Flying capacitor 2 positive pin. Connect a capacitor from CP2P to C | P2N. |
| 20 CP2N 22 CP3N 24 CP4N CP4N CP4N CP5P CP5P CP5P CP4N CP5N CP5N CP4N CP5N CP4N CP5N CP5 | P2P, N to CP4P. |
| 21 CP3P 23 CP4P 25 CP5P CP5P CP5P Flying capacitor 3, 4 and 5 positive Connect capacitors from CP3P to CP4P to CP4N, and from CP5P | P3N, |
| Flying capacitor 5 negative pin. Connect a capacitor from CP5N to C | CP5P. |
| PGND | |
| Oscillation frequency setting pin for charge pumps. Connect to GND through a resistor. | |
| 3 PGND1 GND pin (3.6V buck switching power | er supply) |
| 13 PGND2 28 PGND3 GND pin (charge pumps) | |
| 30 GND pin (control circuits) | |
| 4 PVCC =VCC Power supply pin (3.6V buck switch | ing power supply) |
| Power supply (control input), input it voltage monitor and sense voltage in for over-current control of 3.6V pow | for 3.6V output uput (low) pin ver supply. |
| Power supply pin (inverting charge p Connect to CP4P pin. | |
| Power supply pin (charge pumps) | |
| Connect to FB pin. | |

SHARP

5. Block Diagram and Basic Connections

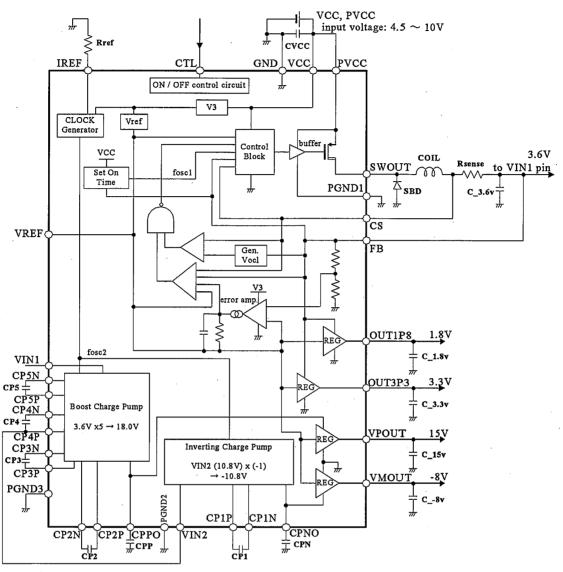


Fig. 2

6. External Components List

| Symbol | Parts Name | Value | Size | Model No. | Maker | Voltage Limit (standard) |
|--------|---|----------------|------|--------------|-------------|-----------------------------|
| Rref | Resistor for charge pump freq. setting | 120kΩ | 1005 | | | - |
| cvcc | Input power supply capacitor | 2.2 μ F | 1608 | *MK107BJ105K | Taiyo Yuden | Vcc x 2 |
| COIL | Inductor | 10 μ Η | 3225 | CBC3225T100M | Taiyo Yuden | - |
| SBD | Schottky diode for regenerative operation | | 2125 | RB551V-30 | Rohm | Vcc |
| Rsense | Current sense resistor | $200 m \Omega$ | 1608 | ERJ3RSFR20 | Matsushita | - |
| C_3.6v | 3.6V output capacitor | 2.2 μ F | 1608 | JMK107BJ225K | Taiyo Yuden | 6.3 |
| C_3.3v | 3.3V output capacitor | 1 μ F | 1005 | JMK105BJ105K | Taiyo Yuden | 6.3 |
| C_1.8v | 1.8V output capacitor | 1μ F | 1005 | JMK105BJ105K | Taiyo Yuden | 6.3 |
| C_15v | Output capacitor for boost | 1μ F | 1608 | TMK107BJ105K | Taiyo Yuden | 25 |
| C8v | Output capacitor for inverting | 1μ F | 1608 | EMK107BJ105K | Taiyo Yuden | 16 |
| CPN | Power supply capacitor for inverting | 1μ F | 1608 | EMK107BJ105K | Taiyo Yuden | 16 |
| CP1 | Flying capacitor 1 | 1μ F | 1608 | EMK107BJ105K | Taiyo Yuden | 16 |
| CPP | Power supply capacitor for boost | 1μ F | 1608 | TMK107BJ105K | Taiyo Yuden | 25 |
| CP2 | Flying capacitor 2 | 1μ F | 1005 | JMK105BJ105K | Taiyo Yuden | 6.3 |
| CP3 | Flying capacitor 3 | 1 μ F | 1005 | JMK105BJ105K | Taiyo Yuden | 6.3 |
| CP4 | Flying capacitor 4 | 1μ F | 1005 | JMK105BJ105K | Taiyo Yuden | 6.3 |
| CP5 | Flying capacitor 5 | 1μ F | 1005 | JMK105BJ105K | Taiyo Yuden | 6.3 |

* using 2 pieces of luF in parallel



7. Operation Description

(1) Power Supply Generation

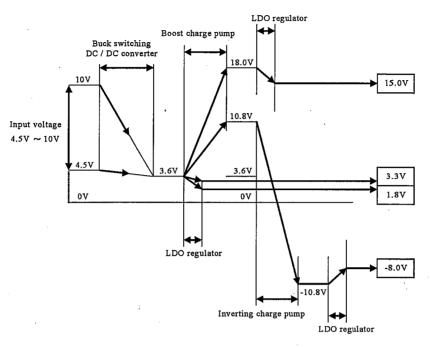


Fig. 3

- (i) Buck switching DC / DC converter creates 3.6V from input voltage.
- (ii) LDO linear regulator 1 makes 3.3V, and LDO linear regulator 2 makes 1.8V from 3.6V input.
- (iii) After 3.6V input is boosted to 18.0V (5 times higher), 15V output is generated through an LDO linear regulator.
- (iv) After 3.6V input is boosted to 10.8V (3 times higher) and then inverted to -10.8V, -8V output is generated through an LDO linear regulator.



(2) Start / Stop Sequence

Input terminal CTL controls start / stop of 1.8V, 3.3V, 15V and -8V outputs, respectively. (High: Start; Low: Stop)

Not to damage CCDs, the following priority is set in start / stop sequence by inside settings.

Start Sequence:

Start sequence by the following order: $1.8V \rightarrow 3.3V \rightarrow 15V \rightarrow -8V$ Outputs are observed in this IC for the regulations to start in the order above. (Refer to Fig. 4)

Stop Sequence:

1.8V, 3.3 V, 15V and -8V outputs are turned off simultaneously.

1.8V, 3.3V and 3.6V outputs are only stopped their voltage generations.

15V and -8V outputs are stopped their voltage generations, and their output capacitors are discharged.

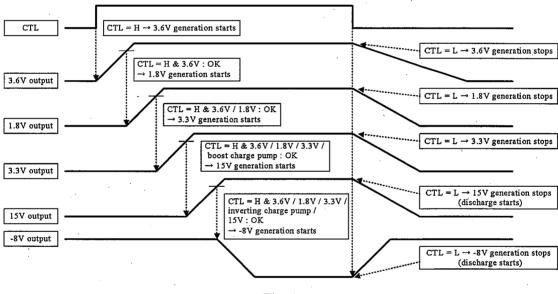


Fig. 4



(3) 3.6V Regulator

3.6V regulator starts operating when the level of CTL changes to H. It monitors output voltage and inductor current, when they are lower than regulation levels, output MOS transistor turns on for the appointed time. If the output voltage is still lower than its regulation level after the appointed time, the output MOS transistor remains on.

Over-current protection works in fold-back type drooping characteristic after the regulation starts.

(4) 3.3V Regulator, 1.8V Regulator

3.3V and 1.8V outputs are generated from 3.6V power supply. The currents are automatically limited by the maximum ability to provide set inside, and these circuits are also protected by the over-current protection of 3.6V power supply.

(5) Charge Pumps, 15V Regulator, -8V Regulator

When 3.6V power supply is set, charge pumps start operating. According to the appointed output permission conditions, each regulator (15V, -8V) starts operating to generate output voltage.

The regulators are protected against over-current by limiting maximum current provided to capacitors.

(6) Over-current Protection

Each output is protected against over-current. The details are mentioned above in (3) \sim (5).



8. Absolute Maximum Ratings

Please use this product within the following absolute maximum ratings all the time, including startup and shutdown.

| | | · · · · · · · · · · · · · · · · · · · | | |
|---------------------------------|--------|---------------------------------------|-------------|----------------|
| Parameter | Symbol | Conditions | Rating | Unit |
| Power supply voltage | Vcc | VCC, PVCC | 20.0 | V |
| Input pin voltage | Vini | CTL | -0.3 ~ 20.0 | V |
| Power dissipation (*1) | PD | Ta ≦ 25 °C | 1428 | mW |
| Power dissipation derating (*1) | ΔPD | Ta > 25 ℃ | 14.3 | mW/℃ |
| Operating temperature range | Topr | | -30 ∼ 85 | ${\mathcal C}$ |
| Storage temperature range | Тѕтс | | -55 ∼ 150 | ${\mathcal C}$ |

(*1) natural convection, on-board (based on SEMI 42-96)

Fig. 5 shows power dissipation temperature characteristic.

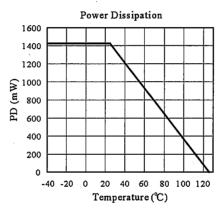


Fig. 5

9. Notes

- (1) Connect all GND pins (GND, PGND1, PGND2, PGND3) together as close as possible to this IC not to make any voltage difference between these GND pins, at startup and shutdown.
- (2) Connect all Vcc pins (VCC, PVCC) together as close as possible to this IC not to make any voltage difference between these Vcc pins, at startup and shutdown.
- (3) Form GND patterns to reduce its impedance.
- (4) Place the decoupling capacitor (CVCC) between Vcc and GND as close as possible to this IC, and do not short the GND or Vcc pins nearer to the IC than the decoupling capacitor.
- (5) Form the line patterns of IREF and VREF pins not to cause noise on them.

 The following pins have signals of larger amplitude in this IC, be careful of wiring them.

 Both sides of flying capacitors for charge pumps (CP1~5)
 - ·Output of switching regulator (SWOUT)
- (6) Do not leave the input pin (CTL) floating. Connect the pin to GND or Vcc when it is not in use.



10. Electrical Characteristics

Unless otherwise specified: Ta = 25°C, VCC = PVCC = 5V, CTL = 5V, other pins are connected according to "5. Block Diagram and Basic Connections" and "6. External Components List."

| connected according | to 5. Bio | ck Diagram and Dasic Connections | unu 0. 1. | Atomai Co | mpononts | <u> </u> |
|---|-----------|---|-----------|------------|----------|----------|
| Parameter | Symbol | Conditions | Min. | Тур. | Max. | Unit |
| Power supply voltage | Vcco | VCC, PVCC | 4.5 | | 10.0 | V. |
| Quiescent current at operation | Ivcc | CTL = H, no load | - | 19 | 38 | mA |
| Shutdown current | Iccs | CTL = L | - | - | 3 | μΑ |
| Oscillation frequency SW | foscs | SWOUT, maximum frequency | 500 | 1000 | 1800 | kHz |
| Oscillation frequency CP | foscc | VIN2, charge pump power supply | 150 | 200 | 250 | kHz |
| Standard voltage | Vref | VREF | 1.231 | 1.250 | 1.269 | V |
| 3.3V voltage | V3p3a | OUT3P3, Io = $0 \sim 120$ mA (outflow) | 3.168 | 3.300 | 3.432 | V |
| | V3p3b | OUT3P3, Io = 0 ~ 150mA (outflow), no load on OUT1P8 | 3.168 | 3.300 | 3.432 | V |
| 1.8V voltage | V1p8 | OUT1P8, Io = $0 \sim 50$ mA (outflow) | 1.728 | 1.800 | 1.872 | V |
| Boosted voltage | Vp | VPOUT, Io = $0 \sim 12$ mA (outflow) | 14.62 | 15.00 | 15.38 | V |
| Inverted voltage | Vm | VMOUT, Io = $0 \sim 2.5$ mA (inflow) | -7.68 | -8.00 | -8.32 | V |
| Control logic threshold H | Vith | CTL H threshold | 0.9 | 1.5 | 2.5 | V |
| Control logic threshold hysteresis width | Vihys | Hysteresis width at H → L | 0.1 | 0.3 | 0.5 | V |
| 3.6V output over-current detection voltage | Vcs | FB = 3.6 V (*1) | 80 | 100 | 120 | mV |
| 3.3V output maximum current | Imaxla | OUT3P3 (outflow) | 120 | - | - | mA |
| | Imax1b | OUT3P3 (outflow), no load on OUT1P8 | 150 | , - | - | mA |
| Boosted output maximum current | Iomax2 | VPOUT (outflow) | 12 | - | - | mA |
| Inverted output maximum current | Iomax3 | VMOUT (inflow) | 2.5 | - | - | mA |
| 1.8V output maximum current | Iomax4 | OUT1P8 (outflow) | 50 | - | - | mA |

^(*1) The voltage difference between CS and FB pins when the oscillation at SWOUT stops, after raising CS pin voltage from FB pin voltage.



11 Package and packing specification

[Applicability]

This specification applies to an IC package of the LEAD-FREE delivered as a standard specification.

1. Storage Conditions.

- 1-1. Storage conditions required before opening the dry packing.
 - · Normal temperature : 5~40°C
 - Normal humidity: 80% (Relative humidity) max.
 - · Storage period : One year max.
 - *"Humidity" means "Relative humidity"

1-2. Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

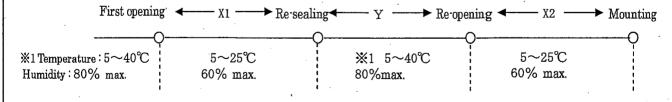
- (1) Storage conditions for one-time soldering. (Convection reflow*¹, IR/Convection reflow.*¹)
 - Temperature : 5~25℃
 - Humidity: 60% max.
 - · Period: 96 hours max. after opening.
- (2) Storage conditions for two-time soldering. (Convection reflow.*1, IR/Convection reflow.*1)
 - a. Storage conditions following opening and prior to performing the 1st reflow.
 - Temperature : 5~25℃
 - Humidity: 60% max.
 - · Period: 96 hours max. after opening.
 - b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.
 - Temperature: 5~25℃
 - Humidity: 60% max.
 - · Period: 96 hours max. after completion of the 1st reflow.

1-3. Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows:

- (1) Storage temperature and humidity.
 - ※1: External atmosphere temperature and humidity of the dry packing.



- (2) Storage period.
 - X1+X2: Refer to Section 1-2(1) and (2)a, depending on the mounting method.
 - Y : Two weeks max.

^{*1:} Air or nitrogen environment.



2. Baking Condition.

- (1) Situations requiring baking before mounting.
 - Storage conditions exceed the limits specified in Section 1-2 or 1-3.
 - Humidity indicator in the desiccant was already red (pink) when opened.
 (Also for re-opening.)
- (2) Recommended baking conditions.
 - Baking temperature and period : $120+10/-0^{\circ}$ for $2\sim3$ hours.
 - The above baking conditions do not apply since the embossed carrier tape are not heat-resistant. Replace the devices on heat-resistant carrier.
- (3) Storage after baking.
 - After baking, store the devices in the environment specified in Section 1-2 and mount immediately.
- 3. Surface mount conditions.

The following soldering conditions are recommended to ensure device quality.

3-1. Soldering.

- (1) Convection reflow or IR/Convection reflow. (one-time soldering or two-time soldering in air or nitrogen environment)
 - Temperature and period :

A) Peak temperature.

250℃ max.

B) Heating temperature.

40 to 60 seconds as 220℃

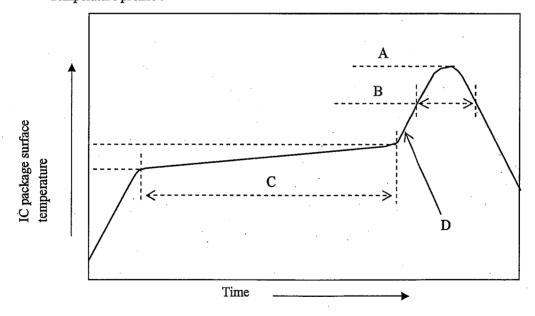
C) Preheat temperature.

It is 150 to 200℃, and is 120±30 seconds

D) Temperature increase rate.

It is 1 to 3°C/seconds

- · Measuring point : IC package surface.
- · Temperature profile:





4. Condition for removal of residual flux.

(1) Ultrasonic washing power: 25 watts / liter max.

(2) Washing time: Total 1 minute max.

(3) Solvent temperature : 15~40°C

5. Package outline specification.

Refer to the attached drawing.

(Plastic body dimensions do include burr of resin.)

The contents of LEAD-FREE TYPE application of the specifications. (*2)

6.Markings.

6-1. Marking details. (The information on the package should be given as follows.)

(1) Product name

3M63

(2) Company name

S

(3) Date code

(Example) YYWWX

YY

Denotes the production year. (Last two digits of the year.)

ww →

Denotes the production week. $(01 \cdot 02 \cdot \sim \cdot 52 \cdot 53)$

 $X \rightarrow$

Denotes the production ref. code (1 digit).

6-2. Marking layout.

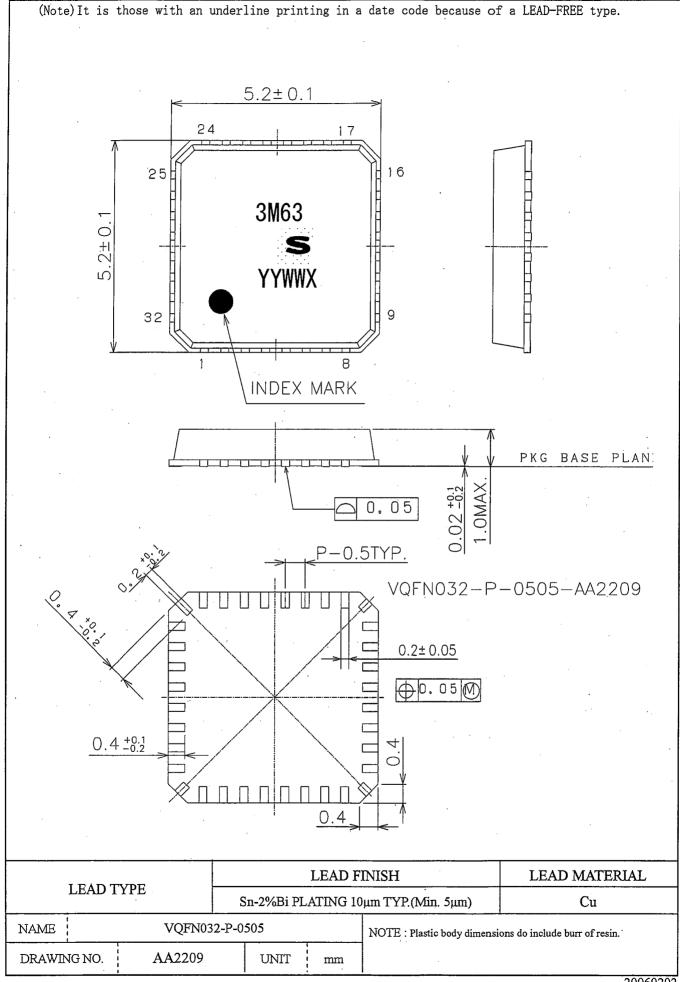
The layout is shown in the attached drawing.

(However, this layout does not specify the size of the marking character and marking position.)

*2 The contents of LEAD-FREE TYPE application of the specifications.

| LEAD FINISH or BALL TYPE | LEAD-FREE TYPE (Sn-2%Bi) 10μm TYP.(Min. 5μm) | | |
|--|---|--|--|
| DATE CODE | They are those with an underline. | | |
| The word of " LEAD FREE" is printed on the packing label | Printed | | |







7.Packing specifications (Embossed carrier tape specifications)

This standard applies to the embossed carrier tape specifications for ICs supplied by SHARP CORPORATION. SHARP's embossed carrier tape specifications are generally based on those described in JIS C 0806 (Japanese Industrial Standard) and EIA481A.

7-1. Tape structure

The embossed carrier tape is made of conductive plastic. The embossed portions of the carrier tape are filled with IC packages and a top covering tape is used to enclose them.

7-2. Taping reel and embossed carrier tape size

For the taping reel and embossed carrier tape sizes, refer to the attached drawing.

7-3,IC package enclosure direction in embossed carrier tape

The IC package enclosure direction in the embossed portion relative to the direction in which the tape is pulled is indicated by an index mark on the package (indicating the No. 1 pin) shown in the attached drawing.

7-4. Missing IC packages in embossed carrier tape

The number of missing IC packages in the embossed carrier tape per reel should not exceed either 1 or 0.1 % of the total contained on the tape per reel, whichever is larger. There should never be more than two consecutive missing IC packages.

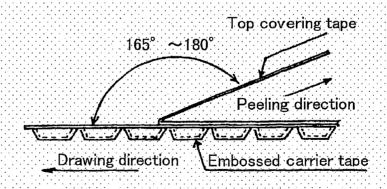
7-5. Tape joints

There is no joint in an embossed carrier tape.

7-6. Peeling strength of the top covering tape

Peeling strength must meet the following conditions.

- (1) Peeling angle at 165~180°.
- (2) Peeling speed at 300mm/min.
- (3) Peeling strength at $0.2 \sim 0.7 \,\mathrm{N}$ ($20 \sim 70 \,\mathrm{gf}$)





7-7. Packing

- (1) The top covering tape (leader side) at the leading edge of the embossed carrier tape, and the trailing edge of the embossed carrier tape, should both be held in place with paper adhesive tape at least 30 mm in length.
- (2) The leading and trailing edges of the embossed carrier tape should be left empty (with embossed portions not filled with IC packages) in the attached drawing.
- (3) The number of IC packages enclosed in the embossed carrier tape per reel should generally comply with the list given below.

| Number of IC Packages/ | Number of IC Packages/ | Number of IC Packages/ |
|------------------------|-----------------------------|------------------------------|
| Reel | Inner carton | Outer carton |
| 2500 devices / Reel | 2500 devices / Inner carton | 12500 devices / Outer carton |

7-8. Indications

The following should be indicated on the taping reel and the packing carton.

- Part Number (Product Name) Storage Quantity Packed Date
- Manufacture's Name (SHARP)

Note: The IC taping direction is indicated by "EL" suffixed to the part number.

EL: Equivalent to "L" of the JIS C 0806 standard..

7-9. Protection during transportation

The IC packages should have no deformation and deterioration of their electrical characteristics resulting from transportation.

8. Precautions for use.

- (1) Opening must be done on an anti-ESD treated workbench.

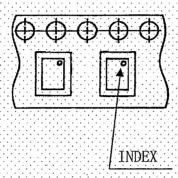
 All workers must also have undergone anti-ESD treatment.
- (2) The devices should be mounted within one year of the date of delivery.



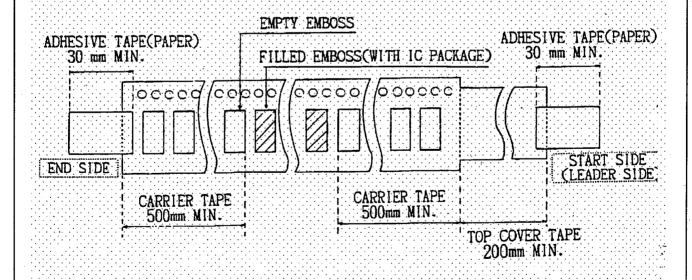
EMBOSS TAPING TYPE (EL)

IC TAPING DIRECTION

THE DRAWING DIRECTION OF TAPE



LEADER SIDE AND END SIDE OF TAPE



| Į | | | | | | | | | |
|---|--------|------------------------|--------|------|-------------|------|-------------|-----|--------|
| | 名称 | i i | | | | 備考 | | | |
| | NAME | Emboss taping type(EL) | | | EL) | NOTE | | | |
| | | | 1 1 | 単位 | | | | , | |
| | DRAWIN | G NO. | CV522 | UNIT | mm | | | | |
| | | | | | | | | 0.0 | 0.0000 |

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