FAIRCHILD SEMICONDUCTOR®

January 2007

FSQ211- Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged SenseFET
- Precision Fixed Operating Frequency (67KHz)
- Consumes Under 0.2W at 265VAC & No Load with Advanced Burst-Mode Operation
- Internal Start-up Circuit
- Pulse-by-Pulse Current Limiting
- Over-Voltage Protection (OVP)
- Over-Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under-Voltage Lockout (UVLO) with Hysteresis
- Built-in Soft Start
- Secondary Side Regulation

Applications

- Charger & Adapter for Mobile Phone, PDA & MP3
- Auxiliary Power for White Goods, PC, C-TV & Monitor

Related Application Notes

- AN-4137, 4141, 4147 (Flyback)
- AN-4134 (Forward)
- AN-4138 (Charger)

Description

The FSQ211 consists of an integrated Pulse Width Modulator (PWM) and SenseFET, and is specifically designed for high performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high-voltage power switching regulator which combines a VDMOS SenseFET with a voltage mode PWM control block. The integrated PWM controller features include a fixed oscillator, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection, and temperature compensated precision-current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSQ211 device reduces total component count, design size and weight, while increasing efficiency, productivity and system reliability. This device provides a basic platform that is well suited for the design of cost-effective flyback converters.

8DIP **8LSOP**

Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)}$
FSQ211	8DIP	Q211	650V	67KHz	14Ω

FPS™ is a trademark of Fairchild Semiconductor Corporation

Typical Application & Output Power Table

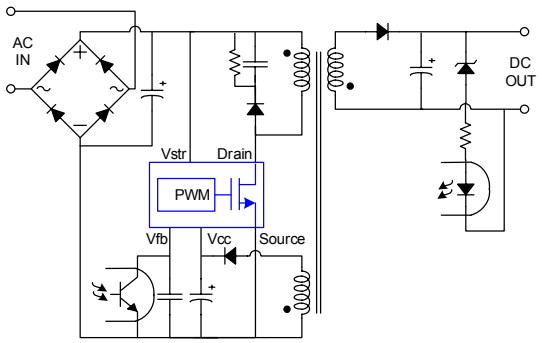


Figure 1. Typical Flyback Application

OUTPUT POWER TABLE		
Product	**Open Frame(1)**	
	230VAC ± 15%(2)	**85~265VAC**
FSQ211	13W	8W

Notes:
1. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sinker, at 50°C ambient.
2. 230 VAC or 100/115 VAC with doubler.

Internal Block Diagram

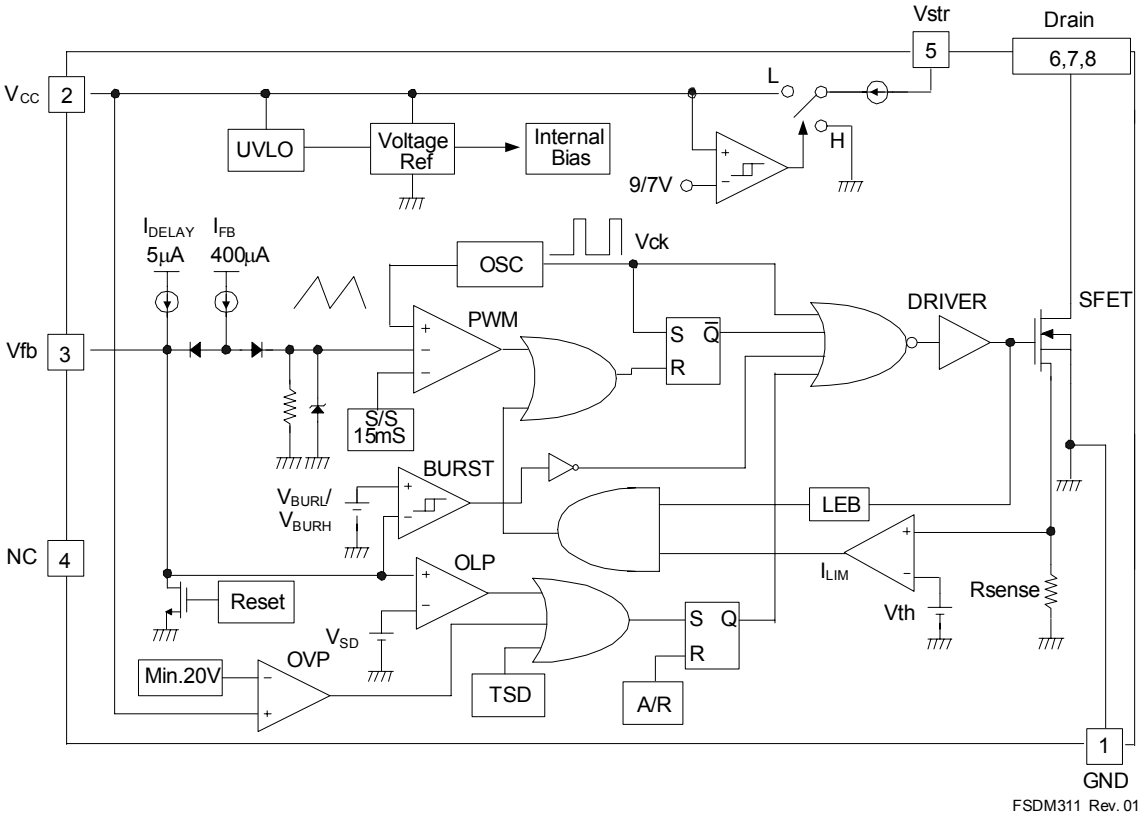


Figure 2. Functional Block Diagram of FSQ211

Pin Assignments

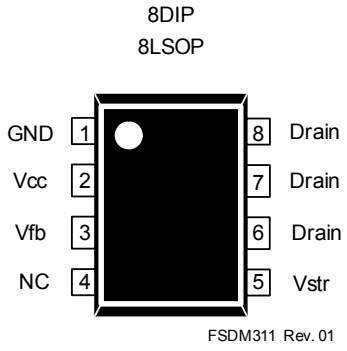


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Pin	Pin Function Description
1	GND	**Ground**. SenseFET source terminal on primary side and internal control ground.
2	Vcc	**Positive supply voltage input**. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (9V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	**Feedback**. Inverting input to the PWM comparator with its normal input level lies between 0.5V and 2.5V. It has a 0.4mA current source connected internally, while a capacitor and opto-coupler are typically connected externally. A feedback voltage of 4.5V triggers over-load protection (OLP). There is a time delay while charging external capacitor Cfb from 3V to 4.5V using an internal 5uA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
4	NC	**No Connection**.
5	Vstr	**Start up**. This pin connects directly to the rectified AC line voltage source. At start up, the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 9V, the internal switch stops charging the capacitor.
6,7,8	Drain	**SenseFET Drain**. The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer is recommended to decrease leakage inductance.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

(T_A=25°C, unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DRAIN}	Drain Pin Voltage	650	V
V_{STR}	Vstr Pin Voltage	650	V
V_{DG}	Drain-Gate Voltage	650	V
V_{GS}	Gate-Source Voltage	±20	V
I_{DM}	Drain Current Pulsed(1)	1.5	A
I_D	Continuous Drain Current (Tc=25°C)	0.5	A
I_D	Continuous Drain Current (Tc=100°C)	0.32	A
E_{AS}	Single Pulsed Avalanche Energy(2)	10	mJ
V_{CC}	Supply Voltage	20	V
V_{FB}	Feedback Voltage Range	-0.3 to V_{STOP}	V
P_D	Total Power Dissipation	1.40	W
T_J	Operating Junction Temperature	Internally limited	°C
T_A	Operating Ambient Temperature	-25 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C

Notes:
1. Repetitive rating: Pulse width is limited by maximum junction temperature
2. L = 24mH, starting Tj = 25°C

Thermal Impedance

(T_A=25°C, unless otherwise specified)

Symbol	Parameter	Value	Unit
8DIP			
θ_{JA}	Junction-to-Ambient Thermal Impedance(1)	88.84	°C/W
θ_{JC}	Junction-to-Case Thermal Impedance(2)	13.94	°C/W

Notes:
1. Free standing with no heatsink; Without copper clad.
   (Measurement Condition – Just before junction temperature T_J enters into OTP)
2. Measured on the DRAIN pin close to plastic interface.

All items are tested with the standards JESD 51-2 and 51-10 (DIP).

Electrical Characteristics

(T_A=25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET SECTION						
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS}=650V, V_{GS}=0V	-	-	25	mA
		V_{DS}=520V, V_{GS}=0V, T_C=125°C	-	-	200	
$R_{DS(ON)}$	Drain-Source On-State Resistance(1)	V_{GS}=10V, I_D=0.5A	-	14	19	Ω
g_{fs}	Forward Trans-Conductance	V_{DS}=50V, I_D=0.5A	1.0	1.3	-	S
C_{ISS}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	162	-	pF
C_{OSS}	Output Capacitance		-	18	-	
C_{RSS}	Reverse Transfer Capacitance		-	3.8	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=325V, I_D=1.0A	-	9.5	-	ns
t_r	Rise Time		-	19	-	
$t_{d(off)}$	Turn-Off Delay Time		-	33	-	
t_f	Fall Time		-	42	-	
Q_g	Total Gate Charge	V_{GS}=10V, I_D=1.0A, V_{DS}=325V	-	7.0	-	nC
Q_{gs}	Gate-Source Charge		-	3.1	-	
Q_{gd}	Gate-Drain (Miller) Charge		-	0.4	-	
CONTROL SECTION						
f_{OSC}	Switching Frequency		61	67	73	KHz
Δf_{OSC}	Switching Frequency Variation(2)	-25°C ≤ T_A ≤ 85°C	-	±5	±10	%
D_{MAX}	Maximum Duty Cycle		60	67	74	%
V_{START}	UVLO Threshold Voltage	V_{FB}=GND	8	9	10	V
V_{STOP}		V_{FB}=GND	6	7	8	V
I_{FB}	Feedback Source Current	0V ≤ V_{FB} ≤ 3V	0.35	0.40	0.45	mA
$t_{S/S}$	Internal Soft Start Time		10	15	20	ms
V_{REF}	Reference Voltage(3)		4.2	4.5	4.8	V
$\Delta V_{REF}/\Delta T$	Reference Voltage Variation with Temperature(2)(3)	-25°C ≤ T_A ≤ 85°C	-	0.3	0.6	mV/°C
BURST MODE SECTION						
V_{BURH}	Burst Mode Voltage	Tj=25°C	0.6	0.7	0.8	V
V_{BURL}			0.45	0.55	0.65	V
$V_{BUR(HYS)}$		Hysteresis	-	150	-	mV
PROTECTION SECTION						
I_{LIM}	Peak Current Limit		0.31	0.35	0.39	A
T_{SD}	Thermal Shutdown Temperature(3)		125	145	-	°C
V_{SD}	Shutdown Feedback Voltage		4.0	4.5	5.0	V
V_{OVP}	Over Voltage Protection		20	-	-	V
I_{DELAY}	Shutdown Delay Current	3V ≤ V_{FB} ≤ V_{SD}	4	5	6	uA
TOTAL DEVICE SECTION						
I_{OP}	Operating Supply Current (control part only)	V_{CC} ≤ 16V	-	1.5	3.0	mA
I_{CH}	Start-Up Charging Current	V_{CC}=0V , V_{STR}=50V	450	550	650	uA

Notes:

1. Pulse test: Pulse width ≤ 300us, duty ≤ 2%
2. These parameters, although guaranteed, are tested in EDS (wafer test) process
3. These parameters, although guaranteed, are not 100% tested in production

Typical Performance Characteristics

(These characteristic graphs are normalized at Ta = 25°C)

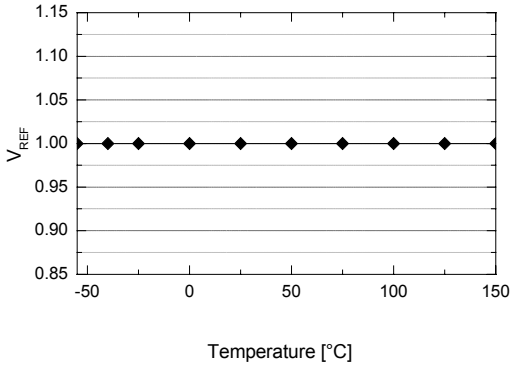


Figure 4-L. Reference Voltage (V_{REF}) vs. T_A

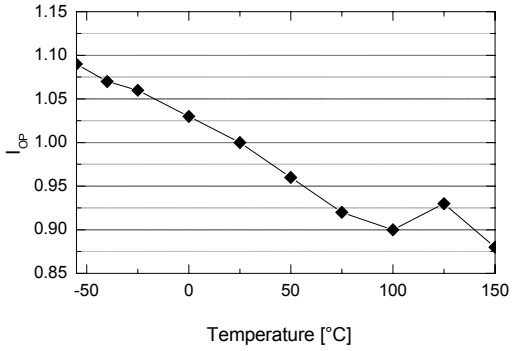


Figure 4-R. Operating Supply Current (I_{OP}) vs. T_A

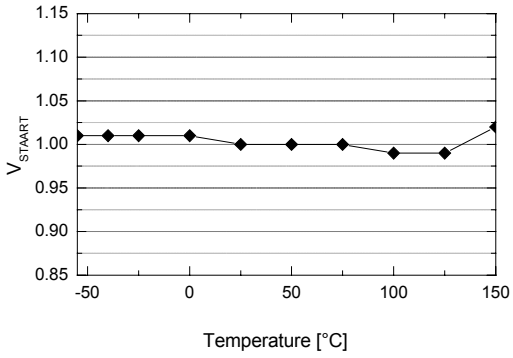


Figure 5-L. Start Threshold Voltage (V_{START}) vs. T_A

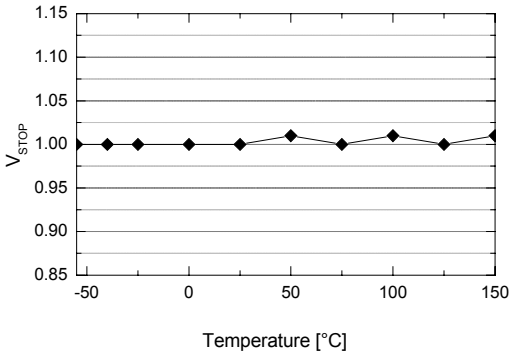


Figure 5-R. Stop Threshold Voltage (V_{STOP}) vs. T_A

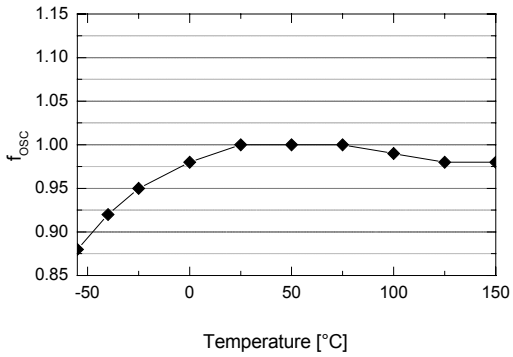


Figure 6-L. Operating Frequency (f_{OSC}) vs. T_A

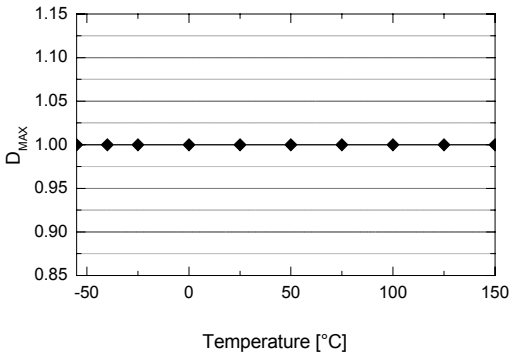


Figure 6-R. Maximum Duty Cycle (D_{MAX}) vs. T_A

Typical Performance Characteristics (continued)

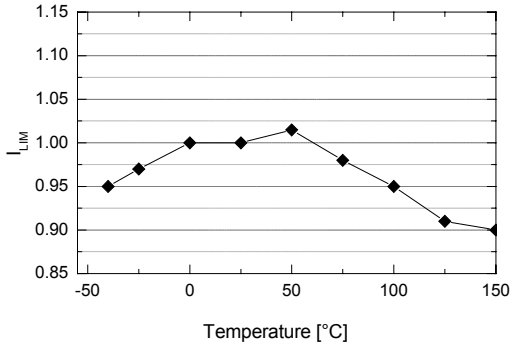


Figure 7-L. Peak Current Limit (ILIM) vs. TA

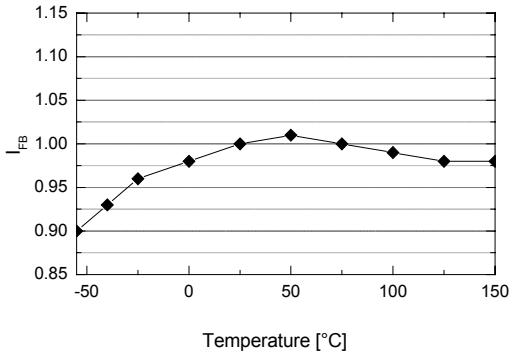


Figure 7-R. Feedback Source Current (IFB) vs. TA

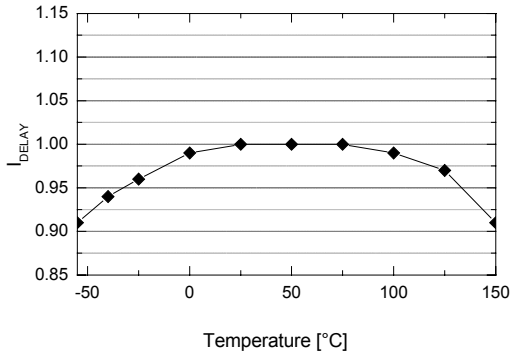


Figure 8-L. Shutdown Delay Current (I_{DELAY}) vs. T_A

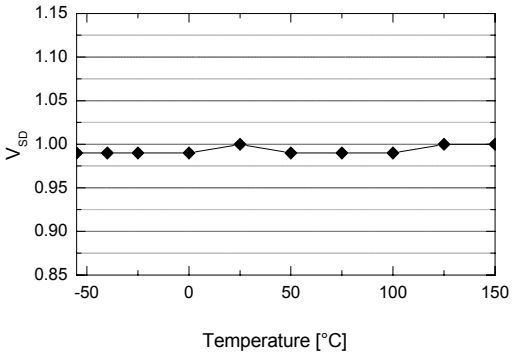


Figure 8-R. Shut Down Feedback Voltage (V_{SD}) vs. T_A

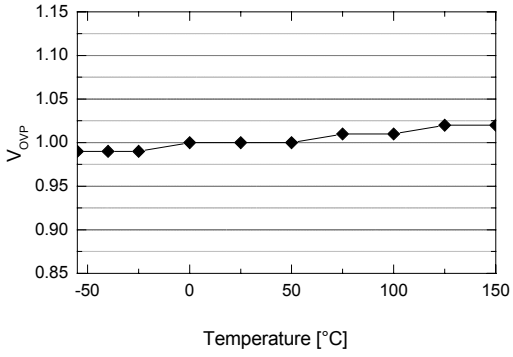


Figure 9-L. Over-Voltage Protection (V_{OVP}) vs. T_A

Functional Description

1. Startup: At startup, the internal high-voltage current source supplies the internal bias and charges the external Vcc capacitor as shown in Figure 10. In the case of the FSQ211, when Vcc reaches 9V, the device starts switching and the internal high-voltage current source stops charging the capacitor. The device is in normal operation provided that Vcc does not drop below 7V. After startup, the bias is supplied from the auxiliary transformer winding.

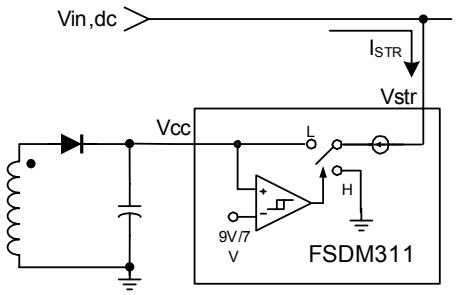


Figure 10. Internal Startup Circuit

Calculating the Vcc capacitor is an important step to design with the FSQ211. At initial start-up in the FSQ211, the maximum value of start operating current I_{START} is about 100uA, which supplies current to UVLO and Vref Blocks. The charging current I_{Vcc} of the Vcc capacitor is equal to Istr - 100uA. After Vcc reaches the UVLO start voltage, only the bias winding supplies Vcc current to the device. When the bias winding voltage is not sufficient, the Vcc level decreases to the UVLO stop voltage and the internal current source is activated again to charge the Vcc capacitor. To prevent this Vcc fluctuation (charging/discharging), the Vcc capacitor should be chosen to have the value between 10uF and 47uF.

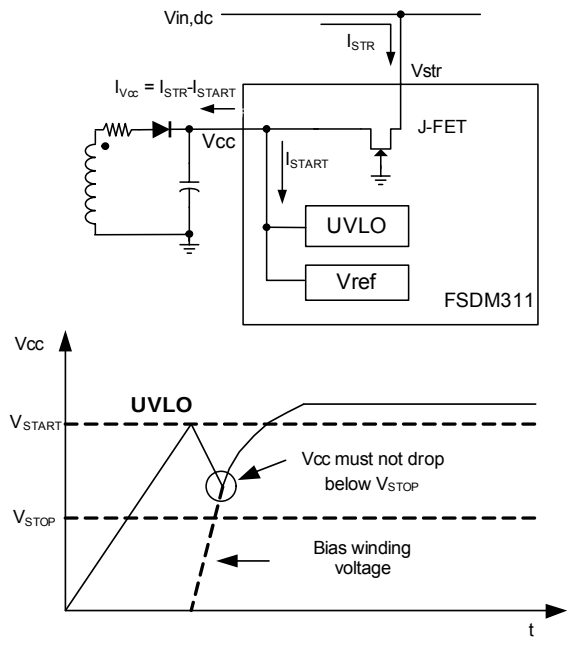


Figure 11. Charging Vcc Capacitor through Vstr

2. Feedback Control: The FSQ211 is the voltage mode controlled device as shown in Figure 12. Usually, an opto-coupler and shunt regulator like KA431 are used to implement the feedback network. The feedback voltage is compared with an internally generated sawtooth waveform. This directly controls the duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage Vfb is pulled down, and it reduces the duty cycle. This happens when the input voltage increases or the output load decreases.

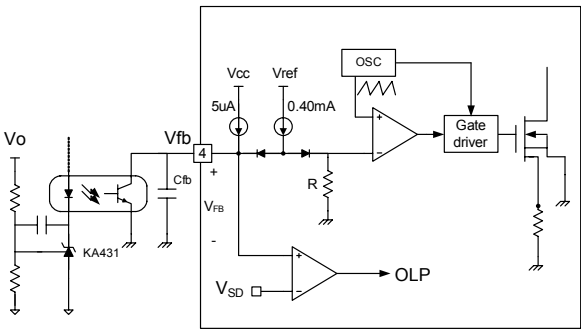


Figure 12. PWM and Feedback Circuit

3. Leading Edge Blanking (LEB): At the instant the internal SenseFET is turned on, the primary side capacitance and secondary side rectifier diode reverse recovery typically cause a high current spike through the SenseFET. Excessive voltage across the Rsense resistor leads to incorrect pulse-by-pulse current limit protection. To avoid this, a leading edge blanking (LEB) circuit disables pulse-by-pulse current limit protection block for a fixed time (t_{LEB}) after the SenseFET turns on.

4. Protection Circuit: The FSQ211 has several protective functions such as over-load protection (OLP), over voltage protection (OVP), under voltage lock out (UVLO) and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, the reliability can be improved without increasing costs. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage V_{STOP} (7V), the protection is reset and the internal high-voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage V_{START} (9V), the device resumes normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

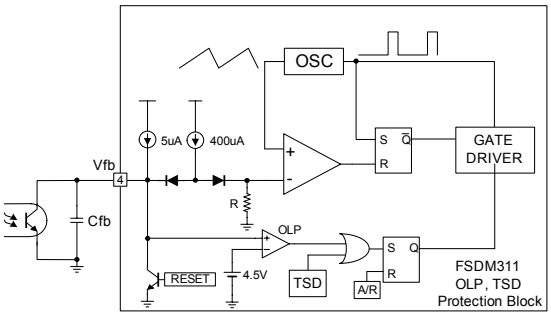
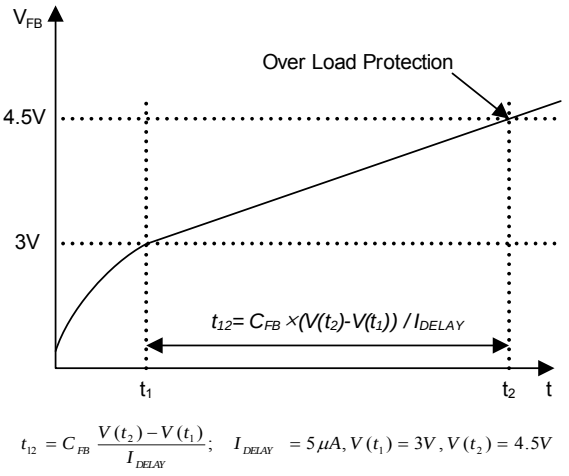


Figure 13. Protection Block

4.1 Over Load Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS is operating normally, the over load protection (OLP) circuit can be activated during the load transition. To avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. If the output consumes more than the maximum power determined by I_{LIM}, the output voltage (Vo) decreases below its rating voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5uA current source (I_{DELAY}) starts to charge Cfb slowly up to Vcc. In this condition, V_{FB} increases until it reaches 4.5V, when the switching operation is terminated as shown in Figure 14. The shutdown delay time is the time required to charge Cfb from 3V to 4.5V with 5uA current source.



$$t_{12} = C_{FB}\frac{V(t_2)-V(t_1)}{I_{DELAY}};\quad I_{DELAY} = 5\mu A, V(t_1) = 3V, V(t_2) = 4.5V$$

Figure 14. Overload Protection (OLP)

4.2 Thermal Shutdown (TSD): The SenseFET and the control IC are integrated, making it easier for the control IC to detect the temperature of the SenseFET. When the temperature exceeds approximately 145°C, thermal shutdown is activated.

5. Soft-Start: The FPS has an internal soft-start circuit that slowly increases the feedback voltage together with the SenseFET current right after it starts up. The typical soft-start time is 15msec, as shown in Figure 15, where progressive increment of the SenseFET current is allowed during the start-up phase. Soft-start circuit progressively increases current limits to establish proper working conditions for transformers, inductors, capacitors and switching device. It also helps to prevent transformer saturation and reduces the stress on the secondary diode.

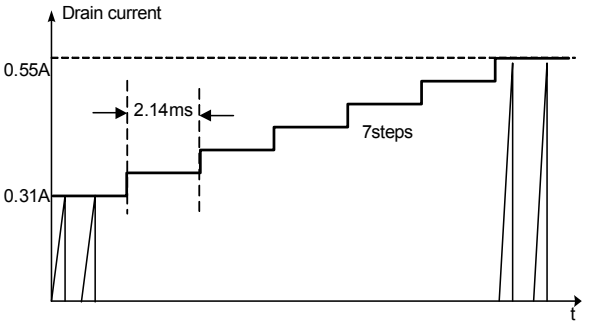


Figure 15. Internal Soft-Start

6. Burst operation: To minimize the power dissipation in standby mode, the FSQ211 enters burst mode operation. As the load decreases, the feedback voltage decreases. The device automatically enters burst mode when the feedback voltage drops below V_{BURL}(0.55V). At this point, switching stops and the output voltages start to drop. This causes the feedback voltage to rise. Once is passes V_{BURH}(0.70V), switching starts again. The feedback voltage falls and the process repeats. Burst mode operation alternately enables and disables switching of the power MOSFET to reduce the switching loss in the standby mode.

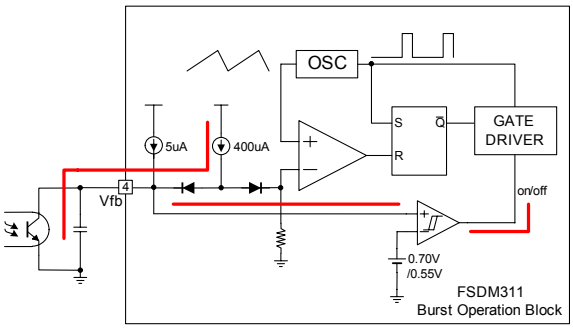


Figure 16. Burst Operation Block

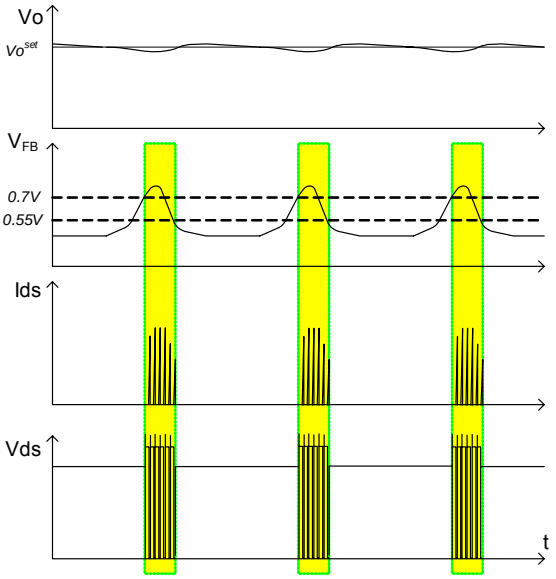


Figure 17. Burst Operation Function

Application Tips

1. Methods of Reducing Audible Noise

Switching mode power converters have electronic and magnetic components, which generate audible noises when the operating frequency is in the range of 20~20,000 Hz. Even though they operate above 20 kHz, they can make noise depending on the load condition. Designers can employ several methods to reduce these noises. Here are three of these methods:

Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin and coil; and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise, but, it can crack the core. This is because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect, depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. It is possible to use a zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of 2~4 kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4 kHz. When the fundamental frequency of noise is located in this range, one perceives the noise as louder, although the noise intensity level is identical. Refer to Figure 18. Equal Loudness Curves.

When FPS acts in burst mode and the burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of burst mode operation lies in the range of 2~4 kHz, adjusting the feedback loop can shift the burst operation frequency. To reduce the burst operation frequency, increase a feedback gain capacitor (C_F), opto-coupler supply resistor (R_D) and feedback capacitor (C_B); and decrease a feedback gain resistor (R_F), as shown in Figure 19.

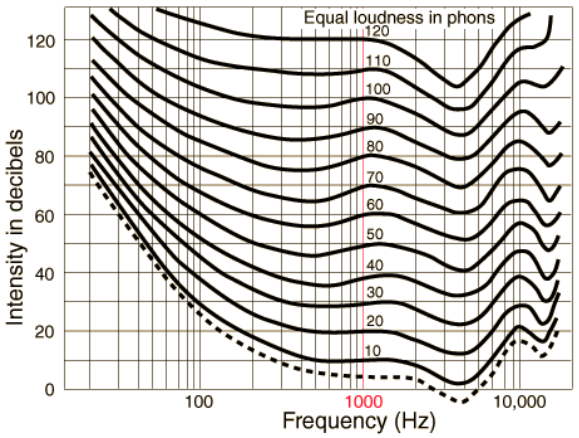


Figure 18. Equal Loudness Curves

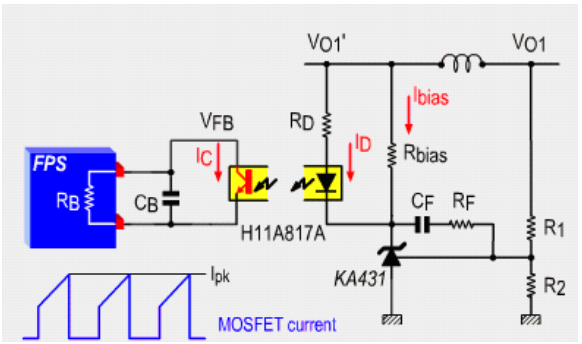


Figure 19. Typical Feedback Network of FPS

2. Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)

AN-4138: Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch (FPS™)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)

AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

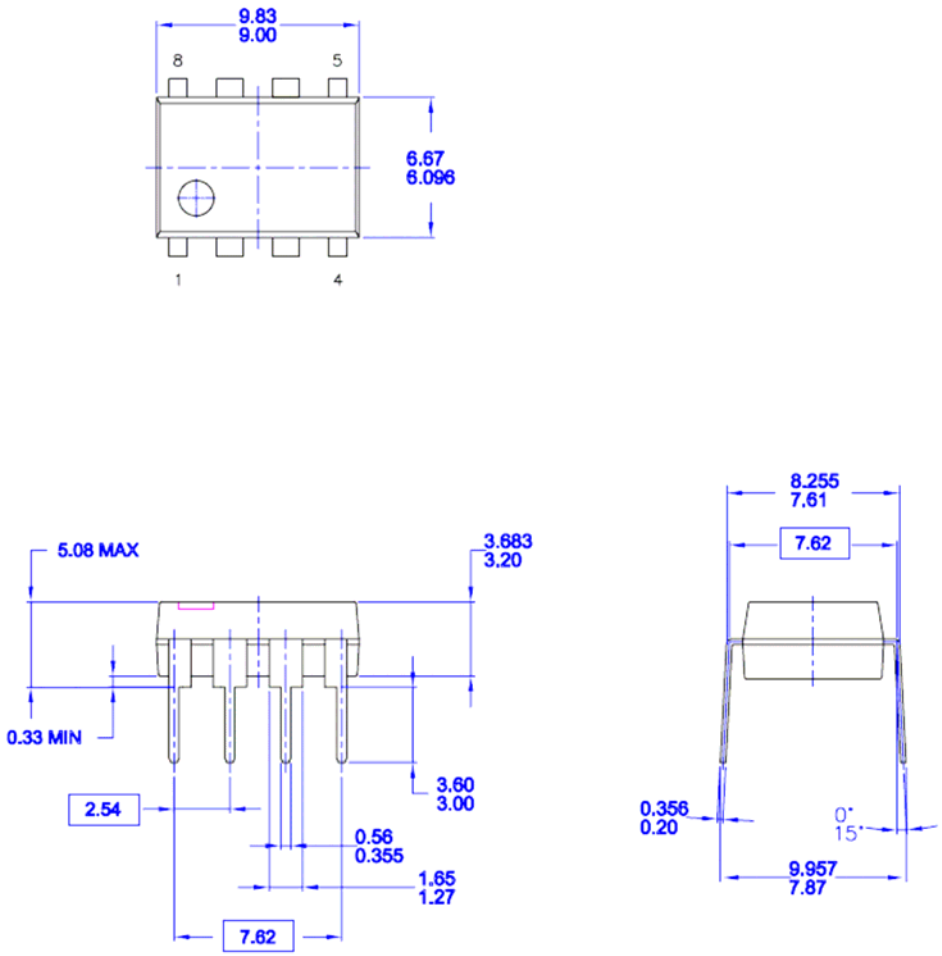
AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for FPS Applications

Physical Dimensions

Dimensions are in millimeters (inches) unless otherwise noted.

8-DIP



FSQ211 Rev.01

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

MKT-N08FrevB

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	PowerEdge™	SuperFET™
ActiveArray™	FASTr™	LittleFET™	PowerSaver™	SuperSOT™-3
Bottomless™	FPS™	MICROCOUPLER™	PowerTrench®	SuperSOT™-6
Build it Now™	FRFET™	MicroFET™	QFET®	SuperSOT™-8
CoolFET™	GlobalOptoisolator™	MicroPak™	QS™	SyncFET™
CROSSVOLT™	GTO™	MICROWIRE™	QT Optoelectronics™	TCM™
DOME™	HiSeC™	MSX™	Quiet Series™	TinyLogic®
EcoSPARK™	I^2C™	MSXPro™	RapidConfigure™	TINYOPTO™
E^2CMOS™	*i-Lo*™	OCX™	RapidConnect™	TruTranslation™
EnSigna™	ImpliedDisconnect™	OCXPro™	µSerDes™	UHC™
FACT™	IntelliMAX™	OPTOLOGIC®	ScalarPump™	UniFET™
FACT Quiet Series™		OPTOPLANAR™	SILENT SWITCHER®	UltraFET®
Across the board. Around the world.™		PACMAN™	SMART START™	VCX™
The Power Franchise®		POP™	SPM™	Wire™
Programmable Active Droop™		Power247™	Stealth™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I19