UX 2105

155Mbps Limiting Amplifier

General Description

The UX2105 is a high gain limiting amplifier designed for SDH/SONET fiber optical receiver systems, accepting a wide range of input AC voltages and providing constant-amplitude voltage swings with some temperature compensation. It integrates a signal detector, with programmable LOS threshold, an optional output disable function and automatic squelch function. It is available in TSSOP 16-pin packages.

Features

- ✧ +3.3V or +5V Power Supply
- ✧ 1mV Differential Input Sensitivity (BER=10^{-10})
- ✧ OUTP/OUTN are CMOS Configuration, Simply AC-coupling
- ✧ Alarm Level Compatible with PECL, TTL and CMOS Level
- ✧ Pin Compatible with the Mindspeed MC2045 and MAXIM MAX3645

Pin Configuration

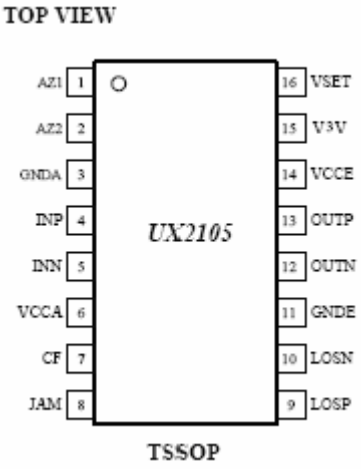

Figure 1. Pin Configuration TSSOP 16

Typical Application Circuit

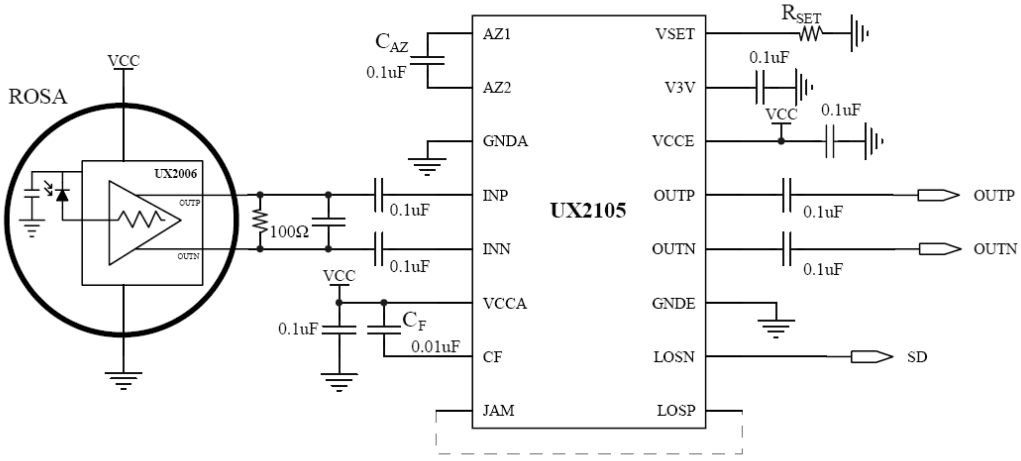

Figure 2. Typical Application Circuit

Pin Description

Pin No.	Name	Function
1	AZ1	Auto-zero capacitor pin. A capacitor connected between this pin and AZ2 sets the time constant of the offset correction loop. The offset correction is disabled when the AZ1 and AZ2 pins are shorted together.
2	AZ2	See AZ1.
3	GNDA	Analog Supply Ground. Must be at same potential as GNDE pin.
4	INP	Positive data input
5	INN	Negative data input
6	VCCA	Analog Supply Voltage. Must be at the same potential as the VCCE pin.
7	CF	Level-detect filter capacitor pin. Connect a capacitor between this pin and VCCA.
8	JAM	The squelch function is disabled when JAM is connected to ground. The automatic squelch function is enabled when JAM is connected to the LOSP.
9	LOSP	Positive Loss-of-Signal output, CMOS level, compatible with PECL and TTL. LOSP is low when the level of the input signal is above the preset threshold set by the VSET input. LOSP is high when the signal level drops below the threshold. Normally connected to JAM pin to enable automatic squelch function to operate.
10	LOSN	Negative Loss-of-signal output, CMOS level, compatible with PECL and TTL. LOSN is high when the level of the input signal is above the preset threshold set by the VSET input. LOSN is low when the signal level drops below the threshold. Indicates Input signal level status.
11	GNDE	Digital Supply Ground. Must be the same potential as the GNDA pin.
12	OUTN	Negative data output, the output buffer is CMOS structure.
13	OUTP	Positive data output, the output buffer is CMOS structure.
14	VCCE	Digital Supply Voltage. Must be at the same potential as the VCCA pin.
15	V3V	5V to 3V conversion output pin.No connection or can connect a capacitor between this pin and GND.
16	VSET	Loss-of-Signal Threshold Pin. Resistor (R_{SET}) to ground sets the LOS threshold. This pin can be left open if the LOS detect function is not required and JAM is connected to ground, otherwise connect VSET to ground.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply(Note 1)	6	V
T_A	Operating ambient	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C

Recommended Operating Conditions

Symbol	Parameter	Rating	Units
V_{CC}	Power supply(Note 1)	3.0 to 5.5	V
T_A	Operating ambient	-40 to +85	°C

Note 1: Related to Ground

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{OS}	Equivalent input Offset Voltage			50	μV
V_{TH}	LOS Sensitivity Range	2		20	mV_{P-P}
HYS	LOS Hysteresis (Note 2)	1	2	4	dB
I_{CC}	Power-Supply Current (Note 3)		43.5		mA

Note 2: Optical, 10log ($V_{DEASSERT}/V_{ASSERT}$).

Note 3: LOSN is at CMOS level, no load terminated to the outputs, with I/O current in the output buffer.

AC Characteristics

(V_{CC}=+3.0V to +5.5V, Typical values are at V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

Symbol	Parameter		Min	Typ	Max	Units
BW	Input Bandwidth@upper -3dB point: Gain>70dB		190	242		MHz
F_{LFC}	Low-Frequency Cutoff	C_{AZ} = open		169		KHz
		C_{AZ} = 0.1μF		21		
V_{IN}	Input signal voltage	Single ended	0.5		800	mV
		Differential	1		1600	
V_{AMP}	Output Amplitude (Note 4)		600		880	mV
R_{IN}	Input Resistance			20		KΩ
C_{IN}	Input Capacitance				2	pF
T_R,T_F	Data Output Transition Time (Note 5)			600	1000	ps
T_{PWD}	Pulse-Width Distortion(Note 6)			100	300	ps
T_{LOS}	LOS Assert/Deassert Time				100	μs

Note 4: Single ended; the output buffer is CMOS structure, shown in Figure3.

Note 5: 20% to 80%

Note 6: T_{PWD}= [(width of wider pulse)-(width of narrower pulse)]/2.

Applications Information

CMOS Output Buffer

CMOS structure, please refer to Figure3. Current sources are integrated internal in the output buffer circuit. Different from PECL output, no 50Ω to (V_{CC}-2V) termination here. The output common mode voltage is at half of V_{CC}. The current flows through the chip partly from the current sources, so it corresponds to that of other similar products with ECL load. AC coupling is required at OUTN and OUTP, and the external capacitors are employed to insulate the DC level with external circuits, as shown in *Typical Application Circuit*.

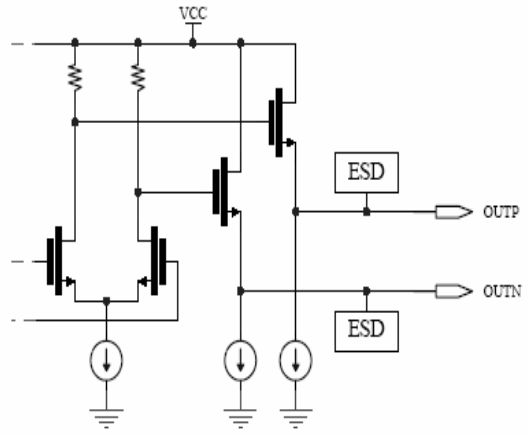

Figure 3. Output Buffer Circuit

LOS Output Terminations

In UX2105, the LOS interface operates three logic states with different termination techniques respectively. When LOSN is connected directly to external circuits, it operates CMOS level; When terminated by a pull up resistor (4.7～10KΩ), see Figure4, it compatible with TTL level; When terminated by 50Ω to (V_{CC}-2V), see Figure5, it compatible with PECL level. The corresponding logic states list in table *LOS Level Status*.

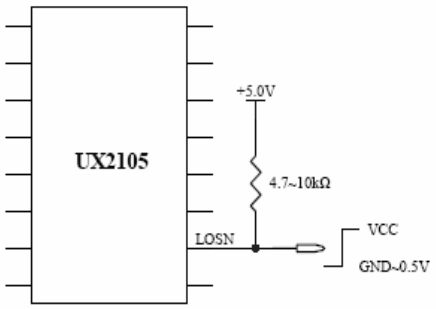

Figure 4. Equivalent TTL Termination Circuit at LOSN

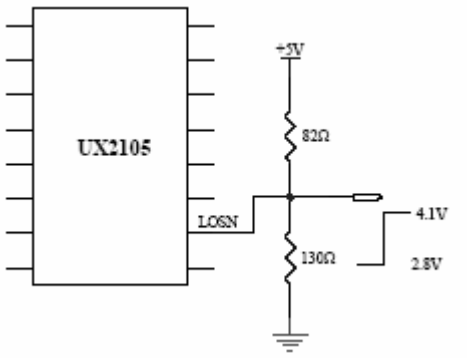

Figure 5. Equivalent PECL Termination Circuit at LOSN

LOS level status

Logic State	CMOS	PECL	TTL
High	V_{CC}	V_{CC}-0.9V	V_{CC}
Low	Ground	V_{CC}-2.2V	Ground to 0.5V

Package Outline

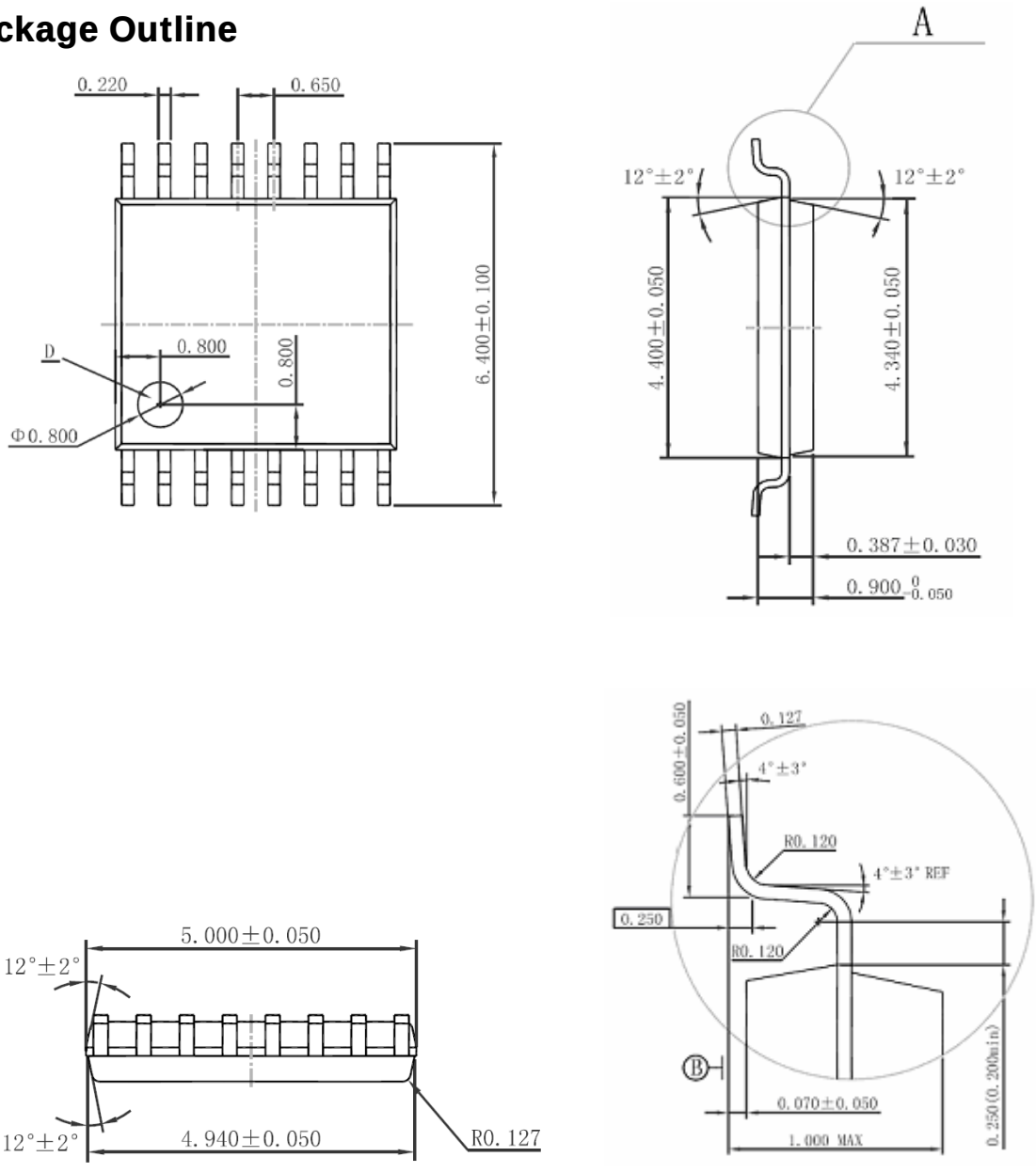

Figure 6. TSSOP16 Package