DATA SHEET

UAA3546

Single chip DECT transceiver

Product specification

2003-July-15

Philips Semiconductors

PHILIPS

FEATURES

- Economical solution for a radio in DECT cordless telephones
- Integrated low phase noise VCO with no production tuning required
- Fully integrated receiver with high sensitivity
- Dedicated PLL synthesizer
- 3 dBm output preamplifier with an integrated switch
- 3-line serial interface bus
- Low current consumption from 2.7 V supply
- Compatible with Philips Semiconductors' baseband chips (ABC & Vega family) and other baseband.
- Reduction of control signals.

APPLICATIONS

1880 to 1930 MHz DECT band cordless telephones.

GENERAL DESCRIPTION

The UAA3546 BiCMOS device is a low power, highly integrated circuit, for 1.9GHz cordless phone applications in the DECT band.

It features a fully integrated receiver, from antenna filter output to the demodulated data output, a fully integrated VCO, a synthesizer to implement a phase-locked loop and a TX preamplifier to drive the external transmit power amplifier (CGY20xx series or UAA359x series).

The synthesizer's main divider is driven by the prescaler output in the range of 1880 to 1930 MHz and is programmed via a 3-wire serial bus. The reference divider ratio is programmable. Outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. Only a passive loop filter is necessary. The charge-pump current is set to 3.5mA for fast switching.

The VCO is powered from an internally regulated voltage source and includes integrated varicap diodes and integrated coils. Its tuning range is guaranteed. The VCO and the synthesizer are switched on one slot before the active slot to lock the VCO to the required channel frequency. Just before the active slot, the synthesizer is switched off, allowing open loop modulation of the VCO during transmission. When opening the loop, the frequency pulling (due to switching off the synthesizer) can be maintained within the DECT specification.

The device is designed to operate from 2.7 V nominal supply. Separate power and ground pins are provided to the different parts of the circuit. The ground leads should be short-circuited externally to prevent large currents flowing across the die and thus causing damage.

All VCC must also be at the same potential (VCC).

QUICK REFERENCE DATA

VCC = 2.8 V; Tamb =25°C, F_{XTAL}=13.824MHz; programming in mode 2; bit slic = 0 and modulation frequency deviation = 288 kHz in receive mode; unless otherwise specified. Characteristics for which only a typical value is given are not tested. Measured and guaranteed on Philips Semiconductors board.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vcc	Supply voltage	.	2.7	2.8	3.6	V
Icc(rx)	Receiver supply current	PLL in open loop mode	-	54	68	mA
Icc(tx)	Transmitter supply current	PLL in open loop mode	-	33	45	mA
Icc(synth)	Synthesizer supply current		-	0.7	4.5	mA
Icc(pd)	Power down supply current	.	-	4	10	uA
$f_{o(RF)}$	RF output frequency	.	1880		1930	MHz
f_{XTAL}	Crystal reference input frequency on the REFCLK pin	.	-	10.368 or 13.824	-	MHz
T_{amb}	Ambiant temperature	.	-10	-	+60	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3546HN	HVQFN32	Plastic, heatsink very thin quad flat package; no leads; 32 terminals; body 5x5x0.85 mm	SOT617-1

BLOCK DIAGRAM

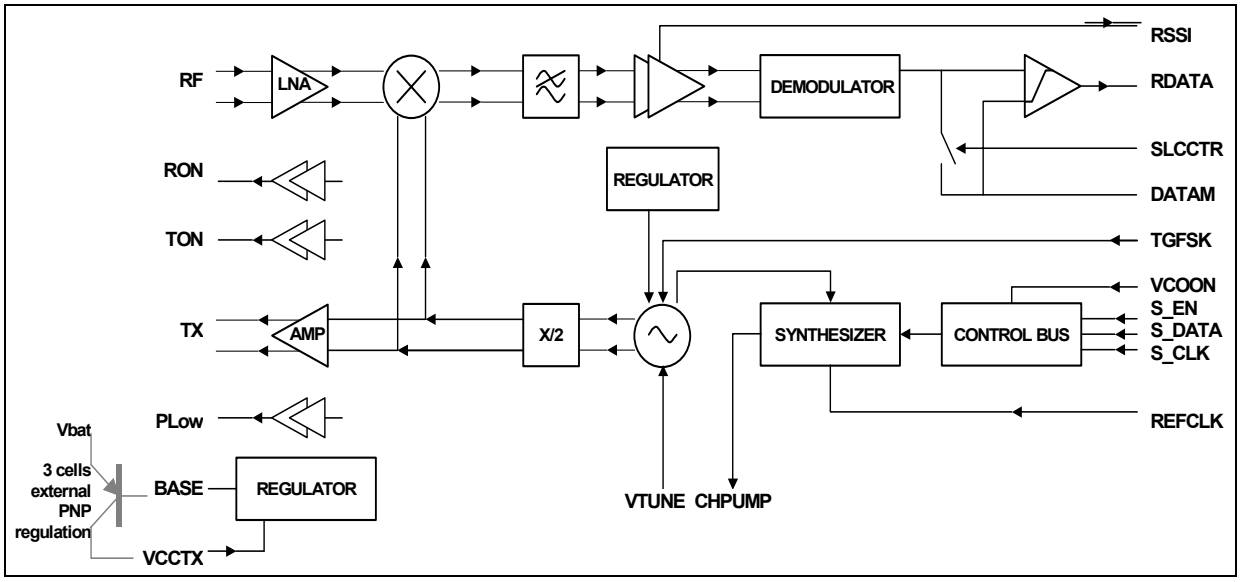


Figure 1 - Typical block diagram

PINNING

SYMBOL	PIN	DESCRIPTION
VREG	1	VCO regulated voltage
VCCREG	2	Positive supply voltage for the VCO regulator
VCCIF	3	Positive supply voltage for the synthesizer part
RDATA	4	Receiver data output
REFCLK	5	Synthesizer reference frequency input
S_DATA	6	Programming bus data input
S_EN	7	Programming bus enable input
S_CLK	8	Programming bus clock input
SLCCTR	9	Receiver threshold control input
RSSI	10	Received Signal Strength Indicator output
VCOON	11	VCO power on input (must be connected to GND if not used)
DATAM	12	Receiver threshold storage input
VCCRX	13	Positive supply voltage for the receiver part
RFB	14	Receiver differential input B
RFA	15	Receiver differential input A
GNDRX	16	Negative supply voltage for the receiver part
R_ON	17	Receiver pin diode control signal output
T_ON	18	Transmitter pin diode control signal output
GNDTX	19	Negative supply voltage for the transmitter part
TXB	20	Transmitter differential output B
TXA	21	Transmitter differential output A
BUSMODE	22	Programming bus configuration input
VCCTX	23	Positive supply voltage for the transmitter part
-	24	reserved (must be connected to GND)
PLOW	25	"Low power" digital output signal to the power amplifier. If not used, must be connected to ground, and bit Plow always programmed to '0'.
BASE	26	External PNP base control output (connect to GND if not used)
-	27	reserved (must be connected to GND)
TEST	28	Test pin (must be connected to GND)
CP	29	Charge-pump output
VTUNE	30	VCO coarse control input
DCOMP	31	Drift compensation input
TGFSK	32	VCO fine control input
GND	diepad	Negative supply voltage

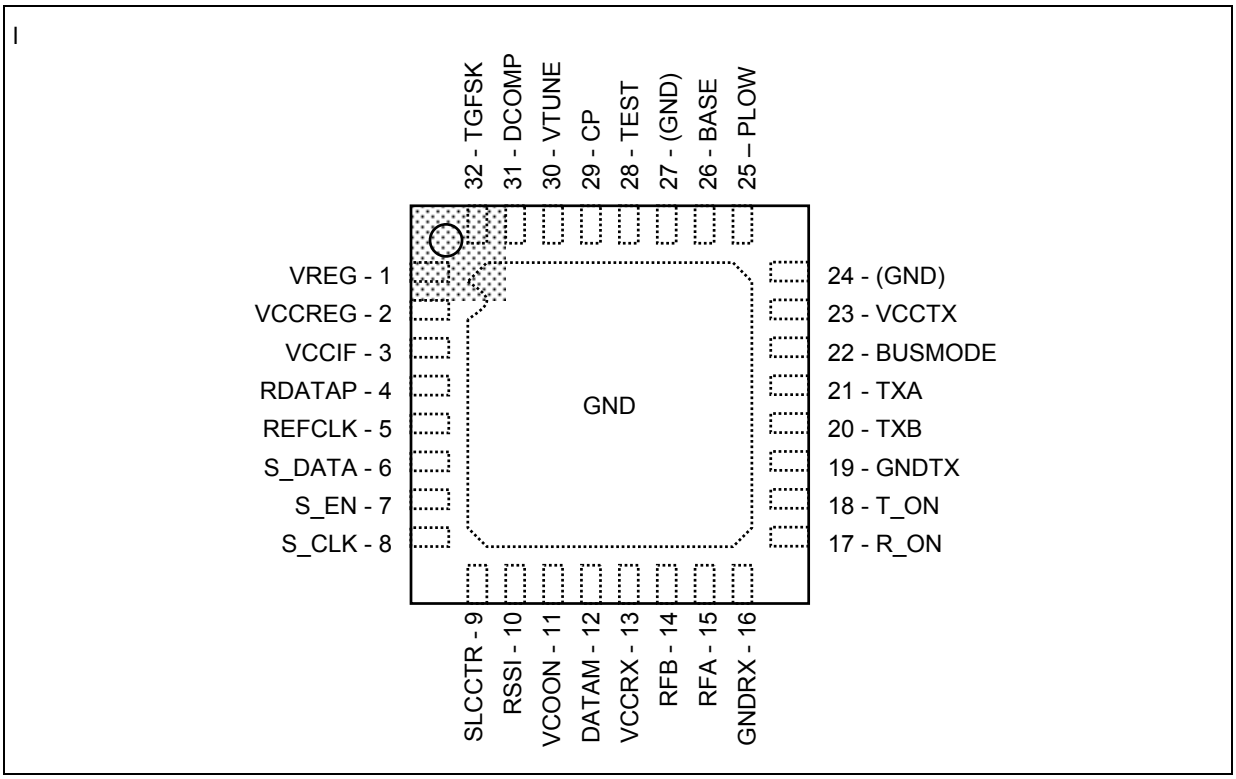


Table 1 - pinning configuration for HVQFN32 package (Top view)

F**UNCTIONAL DESCRIPTION**

Transmit chain

VCO, and prescaler

The fully integrated VCO operates at a multiple of the DECT 1.9GHz frequency. It is supplied by an on-chip regulator (VREG), which minimizes frequency disturbances due to VCC variations. The VCO signal is fed into a prescaler. The large difference between the transmitted and VCO frequencies reduces transmitter-oscillator coupling problems. The output of the prescaler is used to drive the synthesizer main divider and this output can also be switched to either the TX preamplifier or the RX LO output buffer. The high isolation obtained from the prescaler ensures very small frequency changes when turning on the TX preamplifier or the RX part. In TX mode, the oscillator can be directly modulated with GFSK filtered data at pin TGFSK.

In order to compensate for VCO self-heating effect, an 8.2nF capacitor is connected to the DCOMP (pin 31).

After each power-up reset defined by a supply change from 0V to VCC, a VCO calibration sequence starts, based on the capability of the PLL to reach the lowest and highest frequency of the extended DECT band with the middle VCO band during the standard locking period of a blind slot. If one of these border frequencies is not achievable (i.e. the CP output is not in the correct voltage range), the selected VCO band will be shifted to a low or high VCO band accordingly. The calibration sequence uses the reference clock and timing control signal of the baseband; but the frequency programmed using the bus is overwritten to target the border frequencies during the locking time. The active 2 slots following the blind slots used for the calibrations are disabled, TON and RON pin diode control signals remain off, so no incorrect RF signal is transmitted.

The VCO can also be re-calibrated by programming the bit vcocal to 1 and back to 0. The following two blind slots will be used for the calibration. Together with bit vcocal =1, the bit trx must be 1 so the transceiver is in receive mode and doesn’t transmit odd frequencies.

TX PREAMPLIFIER

The TX preamplifier amplifies the RF signal up to a level of 3 dBm typical that is suitable for use with Philips Semiconductors' DECT power amplifiers. Under reset conditions, the TX preamplifier is on during blind slot. By using the relevant programming bit, it's possible to use the SLCCTR signal in transmit mode to control TX preamplifier start and stop time in the frame.

In order to control the low power pin of the external power amplifier, a pin PLOW is available which reflect in TX mode the content of bit Plow.

External regulator

Together with an external PNP transistor, it's possible to overpass the maximum rating 3.6V supply voltage of the transceiver. In this configuration, a 3 cells supply can be implemented withstanding up to 5.5V and converted into 2.8V.

This additional regulator is designed to maintain the VCC pin supply high enough during power down state, and can wake-up in few tens of microseconds. It can be used also to supply the power amplifier with the adequate external PNP and decoupling capacitor.

When not used, the 'base' pin must be connected to GND.

Synthesizer

MAIN DIVIDER

The main divider is clocked by the RF signal from the prescaler; at frequencies from 1880 to 1930 MHz. Any main divider ratio from 2176 to 2303 inclusive can be programmed.

REFERENCE DIVIDER

The reference divider is clocked by the signal at pin REFCLK. The circuit operates with digital input levels as well as analog from 300mVpp to 1.0Vpp at a frequency of 13.824 MHz. By programming the relevant 'refd0' bit, the reference frequency can be changed for 10.368MHz or 13.864MHz.

PHASE COMPARATOR

The output of the main and reference dividers drive the phase comparator. It produces current pulses at pin CP. The pulse duration is equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP sinks current. If the reference divider edge arrives first, CP sources current. An internal resistor defines the DC value of the charge-pump current. Additional circuitry is included to ensure that the gain of the phase detector remains linear even for small phase errors.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. These 3 lines are data (S_DATA), clock (S_CLK) and enable (S_EN).

The data sent to the device is loaded in bursts framed by S_EN. S_CLK and S_DATA lines are used to program the register. S_DATA should change value on the non-active edge of S_CLK. Only the last bits serially clocked into the device are retained within the register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The last bit entered is b0. For the divider ratio N, the first bit entered is the most significant (MSB).

The circuit can operate in 3 different programming modes called mode 2,3 and 4 respectively, and are described below (see TIMING DIAGRAM on page 17).

The external pin called 'Busmode' selects the programming mode. If 'Busmode' is connected to the ground voltage, the transceiver is in mode 2 or mode 3 depending of the external pin VCOON use. If 'Busmode' is connected to the supply voltage, the transceiver is in mode 4.

MODE 2

In mode 2, S_CLK rising edge is active and S_DATA signal is active high. S_EN must be LOW to capture a new programming sequence, while S_EN goes high after a programming sequence to switch on the synthesizer and

write in the main divider. During synthesizer operation, S_EN should be kept high. The register data format is shown in on page 10.

A programming sequence is detected if at least one rising edge occurs on S_CLK while S_EN is low. If no programming sequence is detected, the following S_EN rising edge is interpreted as a power-down request, and called 'S_EN stop pulse'. The VCOON input pin should be connected to ground in this mode.

MODE 3

The mode 3 is identical to mode 2 with the exception of the input signal VCOON. This additional signal coming from the ABC baseband family is used to power down the transceiver replacing the 'S_EN stop pulse'. The signal VCOON falling edge puts the IC in power down mode, while its rising edge has no effect.

MODE 4

In mode 4, the S_DATA signal is active low (that means the 0 volt voltage on the pin correspond to a information '1' in the register) and the S_CLK signal falling edge is active. S_EN must be high (connected to the supply voltage) to capture a new programming sequence. Two different word lengths can be loaded into the circuit, selected accordingly to their address in b0. The long one corresponds to the synthesizer programming, and is enter prior to the PLL locking. The short one is due just before the active slot to control the PLL loop opening.

By setting the bit test to 1, the long word can be extended and access to additional control bits is available. The data format is shown in Table 3 or Table 4 on page 10.

Receiver

The receiver is a fully integrated RF+IF strip and demodulator. It provides all the required channel filtering and generates analog RSSI and a switched output for PHILIPS Semiconductors' baseband chip. Very few off-chip components are required and all of these can be placed without trimming. The chip is designed to operate from a power supply voltage, which can fall to 2.7V. The input is the RF antenna signal, derived from the band filter or the antenna switch. The outputs are the RSSI voltage, representing the instantaneous signal strength and two high level demodulator output signals RDATA, DATAM. DATAM is switched by SLCCTR to generate the external slicer threshold, and an internal circuitry takes into account the possible delay in the SLCCTR signal falling edge. This circuitry, called RX threshold compensation, is set when bit Nrxcomp = 0 and it is assumed than SLCCTR rising edge occurs while a signal is present at antenna and the SLCCTR falling edge could occur up to the SYNCH word first 2 identical bits. If bit Nrxcomp = 1, the external capacitor on the DATAM pin stores the slicer threshold and the SLCCTR rising edge could therefore occur before any signal at antenna and the SLCCTR falling edge must occur during the PREAMBLE word to obtain optimal performance. The latter setup is suitable for the radio link scanning and synchronization.

During the blind slot, while the PLL is settling, an internal voltage source is activated to precharge the external capacitor on the DATAM pin to a voltage close to the required slicer threshold.

OPERATING MODES

Three operating modes are available in this chip (see timing diagrams from page 17) depending of the Busmode pin voltage.

MODE 2

The Reduced Signal Mode (Mode 2), the serial bus programming controls the IC functions and timing.
The S_EN signal controls the chip timing. After the register programming, the S_EN rising edge programs the PLL, closes the loop, powers on the VCO and if the bit 'trx' = 0 and the bit 'ppaon' = 0, turns on the TX preamplifier. On the falling edge of this first pulse of S_EN, the loop is opened (unless the bit 'pll' is set to 1) and the receiver switches on if the 'trx' bit=1. A second rising edge on S_EN, the 'stop pulse', is required at the end of the wanted slot to power down the IC. This 'stop pulse' should occur without any S_CLK rising edge during preceding S_EN low-level state. Otherwise, this second pulse will be considered as a new programming and IC will start a new cycle (a blind slot followed by an active slot).
In order to drive the RX pin diode, the R_ON pin reflects the receiver's internal power-on signal. The TX pin diode could be respectively driven by the T_ON signal, reflecting the active transmit slot timing or, if bit 'ppaon' = 1or bit 'ton' = 1, the SLCCTR signal state during the TX slot.

MODE 3

The Advanced Signal Mode (Mode 3) is close to mode 2. The difference comes from the VCOON pin. The falling edge powers down the IC, instead of the S_EN stop pulse.

MODE 4

In the External signal Mode (Mode 4), the serial bus is totally new and fit with other baseband family. In this mode, the pin "Busmode" is connected to the positive supply voltage.
The S_EN signal controls the chip timing. The IC is powered up when S_CLK or S_EN are high. During programming, the S_CLK is used for bit validation so S_EN is maintained high. For the other part of the cycle, S_CLK is maintained high.
At the end of the active slot, either the S_CLK signal goes low putting the IC into power down mode; or a new programming occurs to start a new blind slot.
In order to drive the RX pin diode, the R_ON pin reflects the receiver's internal power-on signal. The TX pin diode could be respectively driven by the T_ON signal, reflecting the active transmit slot timing or, if bit 'ppaon' = 1 or bit 'ton' = 1, the SLCCTR signal.

REDUCED INTERFACE.

In order to reduce the number of physical lines connecting the baseband to the transceiver, a specific interface is proposed below.

On the transceiver side, the pins RSSI and TGFSK could be connected together. TGFSK is used when the transceiver is in TX mode, while RSSI is used in RX mode. It's still possible to adjust the TGFSK level by adding a serial resistor in the signal going only to TGFSK, without affecting the RSSI level. The modulation signal level reduction is then approximately 15kΩ/(R+ 15kΩ).

The pins SDATA and SLCCTR could also be connected together. SLCCTR is only active when the transceiver is on, while SDATA is only active when the IC is in power-down This configuration supposes that SLCCTR signal is not used during transmit blind slot period, meaning that the bit 'ppaon' = 0 and bit 'ton' = 0 while the transceiver is in mode 4.

The figure below illustrates this interface on the transceiver side:

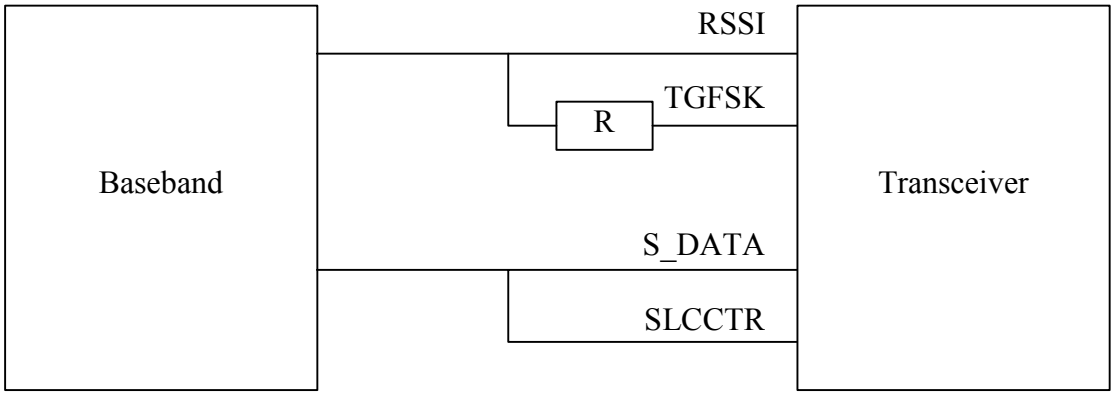


Figure 2 - Combining interface signals

See user manual for complementary info.

BIT PROGRAMMING

Table 2 - Mode 2 and mode3 bus programming (Busmode pin to ground)

First IN (MSB)											
b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12
Plow / Nrxcomp 0	0	0	0	slic 0	0	0	0	0	0	tpow1 0	vcocal 0
										(LSB)	Last IN
b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
refd0 1	pll 0	ppaon0	ton 0	0	N = b 0XXXXX						trx

Table 3 - Mode 4 bus programming (LONG WORD) (BusMode pin to VCC)

First IN (MSB) **[b23..b12] only effective if b11=1**											
b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12
0	0	0	slic 0	0	0	0	0	0	tpow1 0	vcocal 0	refd0 1
										(LSB)	Last IN
b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
test 0	ppaon 0	ton 0	0	N						$\overline{\text{trx}}$	address 1

Note: In mode 4, the '1' corresponds to a low level signal (typically ground) on SDATA pin.

Table 4 - Mode 4 bus programming (SHORT WORD) (Busmode pin to VCC)

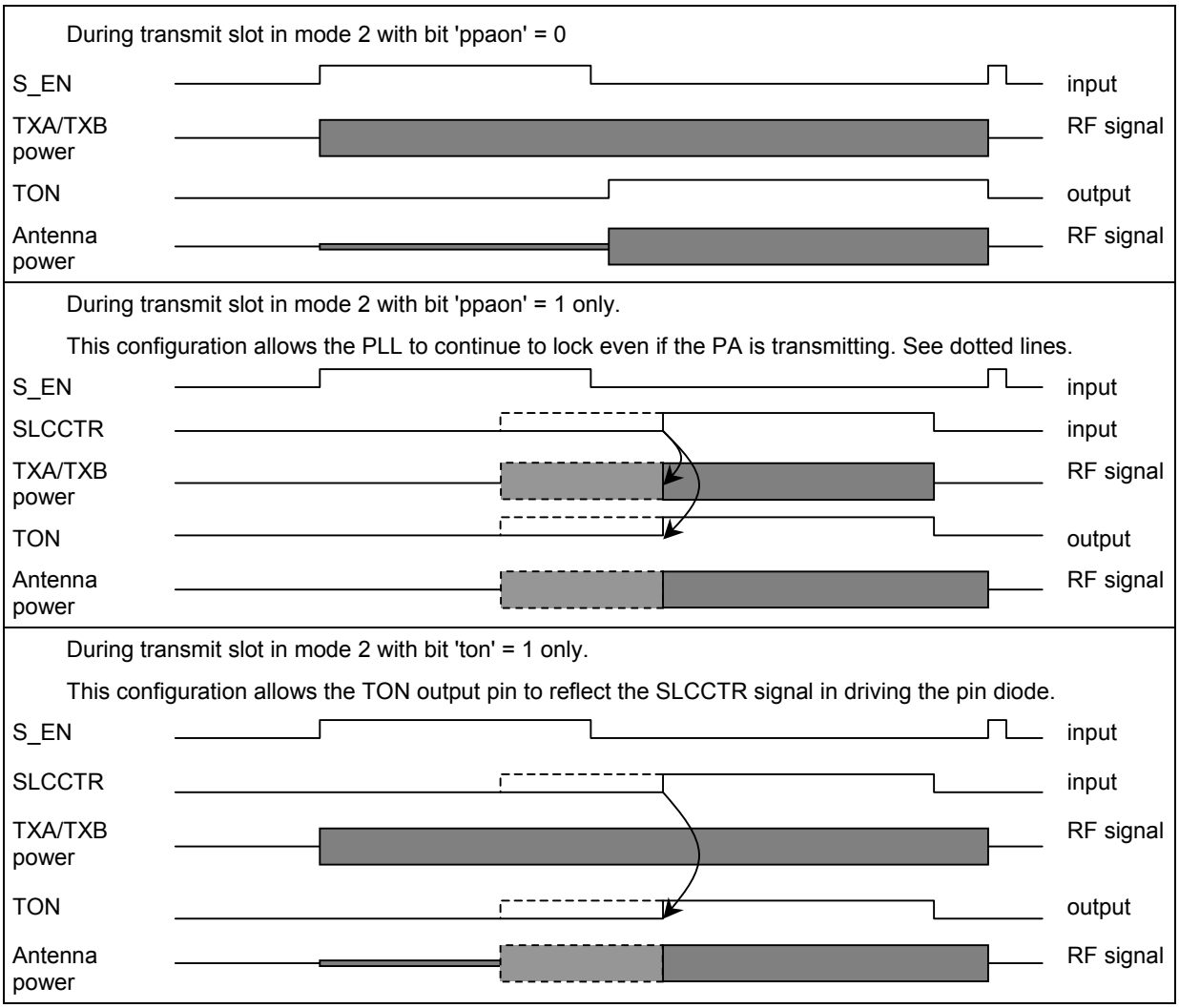
First IN (MSB)	SHORT WORD	(LSB) Last IN
b2	b1	b0
Plow / Nrxcomp 0	pll 0	address 0

Note: In mode 4, the '0' corresponds to a high level signal (typically Vcc) on SDATA pin.

Bits description

- Bit trx : defines if the transceiver will be used in transmit mode (bit trx = '0') or receive mode (bit trx = '1') during the following active slot. So for transmit mode, bit b0 = '0' in mode 2 and 3, or bit b1 = '1' in mode 4 ; and for receive mode, bit b0 = '1' in mode 2 and 3, or bit b1 = '0' in mode 4.
- Bits N : Define the main divider ratio (see Table 2, Table 3, Table 7 and Table 8).
- Bit ton : In transmit mode, when set to 1 defines that SLCCTR signal controls the TON output signal; otherwise TON is high only during active slot (see page 17).
- Bit ppaon : In transmit mode, defines if the SLCCTR signal is used during transmit slot to control the TX preamplifier on/off status. Default is 0 and the SLCCTR is not used as input during transmit slot.

Table 5 - Effect of bit 'ppaon' during transmit slot.



- Bit pll : Defines what is the PLL loop status during active slot. The default is 0, for PLL open loop during active slot.
- Bits refd0 : defines the reference divider ratio. Default is 0 so the reference division ratio is 12.

Table 6 - Reference divider ratio

Bit refd0	Divider ratio
0	12 (reset state)
1	16

Bit vcocal : This bit defines the VCO recalibration request and acts as a reset signal of the VCO calibration. When set to 1, the VCO calibration request is stored internally; but the VC0 calibration will start only if this bit returns to 0. The 2 slots immediately after the 0 programming are used for calibration where the active part is masked. The VCO recalibration request overwrites the power-up reset VCO calibration. It's recommended to set the bit vcocal to 1 together the bit trx to be in receiving mode.

- Bit tpow1 : Increases the transmitted power. Default is low power, low level.
- Bit slic : Defines in receive, if set to 1, that the analog demodulator signal is present on RDATA, this configuration is present for evaluation purpose only. Default is 0 for digital output. Note that this bit must set to 0 in transmit and receive for normal operation and performances.

- Bit Nrxcomp : When set to 1 during receive slot, stops the RX threshold post-preamble compensation by shorting the internal and external capacitors storing the threshold voltage on DATAM pin. Default is 0, RX threshold compensation ON.
- Bit Plow : Defines, when in transmit, the level on the Plow digital output pin during the blind and active slot in mode 2 and mode 3 ; and only during active slot for mode 4. In receive mode, the pin remains low.
- Bit test : Defines whether the front programming data should be used for test mode programming (only available in mode 4)

Table 7 - Main divider ratio and synthesized frequency in mode 2 or 3

Band	N						trx	Main div (n) [N,trx]	Synth freq 0.864* (2176+n)	Chan. freq 0.864* (2176+n-trx)	
A	0	0	0	0	0	1	0	2	1881.792	1881.792	TX
A	0	0	0	0	0	1	1	3	1882.656	1881.792	RX
A	0	0	1	0	1	0	0	20	1897.344	1897.344	TX
A	0	0	1	0	1	0	1	21	1898.208	1897.344	RX
B	0	0	1	1	0	1	0	26	1902.528	1902.528	TX
B	0	0	1	1	0	1	1	27	1903.392	1902.528	RX
B	0	1	0	1	1	0	0	44	1918.08	1918.08	TX
B	0	1	0	1	1	0	1	45	1918.944	1918.08	RX
C	0	1	0	0	1	1	0	38	1912.896	1912.896	TX
C	0	1	0	0	1	1	1	39	1913.76	1912.896	RX
C	0	1	1	1	0	0	0	56	1928.448	1928.448	TX
C	0	1	1	1	0	0	1	57	1929.312	1928.448	RX

Table 8 - Main divider ratio and synthesized frequency in mode 4

Band	N						$\overline{trx}$	Main div (n) [N,trx]	Synth freq 0.864* (2176+n)	Chan. freq 0.864* (2176+n-trx)	
A	0	0	0	0	0	1	1	2	1881.792	1881.792	TX
A	0	0	0	0	0	1	0	3	1882.656	1881.792	RX
A	0	0	1	0	1	0	1	20	1897.344	1897.344	TX
A	0	0	1	0	1	0	0	21	1898.208	1897.344	RX
B	0	0	1	1	0	1	1	26	1902.528	1902.528	TX
B	0	0	1	1	0	1	0	27	1903.392	1902.528	RX
B	0	1	0	1	1	0	1	44	1918.08	1918.08	TX
B	0	1	0	1	1	0	0	45	1918.944	1918.08	RX
C	0	1	0	0	1	1	1	38	1912.896	1912.896	TX
C	0	1	0	0	1	1	0	39	1913.76	1912.896	RX
C	0	1	1	1	0	0	1	56	1928.448	1928.448	TX
C	0	1	1	1	0	0	0	57	1929.312	1928.448	RX

Note: In mode 4, the '1' corresponds to a low level signal (typically ground) on SDATA pin.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Vcc	Maximum supply voltage		-0.3	+3.6	V
V_{PIN}	Maximum voltage on all input pins except BASE		-0.3	+3.6	V
V_{BASE}	Maximum voltage on BASE pin		-0.3	+6.0	V
Pi(max)	Maximum power at receiver input			15	dBm
∆GND	Difference in ground supply voltage applied between all ground pins			0.01	V
T_{amb}	Ambiant temperature		-10	+60	°C
T_{stg}	Storage temperature		-55	+125	°C
T_j	Junction temperature		-	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handle MOS devices.

All pins complain with “EIA/JESD22-A114-A Class2 (Oct. 97)”.

LATCH-UP

Qualification phase reveals that the pin REFCLK is susceptible to latch-up if a negative current larger than 60mA is drawn out of the UAA3546HN, corresponding to a negative pin voltage (below the ground voltage).

Under normal conditions, the REFCLK signal level is attached to the positive supply voltage and connected through a serial capacitor. The latch-up condition is not applicable in the practical implementation.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
T_{stg}	Thermal resistance from junction to ambiant for HVQFN package	In free air with die pad connected	30	K/W

CHARACTERISTICS

VCC = 2.8 V; Tamb =25°C, F_{XTAL}=13.824MHz; programming in mode 2; bit slic = 0 and modulation frequency deviation = 288 kHz in receive mode; unless otherwise specified. Characteristics for which only a typical value is given are not tested. Measured and guarantied on Philips Semiconductors board in HVQFN32 package.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
Vcc	Supply voltage	External supply	2.7	2.8	3.6	V
		Supplied by Vsup	2.65	2.8	-	V
Icc(rx)	Receiver supply current	PLL in open loop mode	-	54	68	mA
Icc(tx)	Transmitter supply current	PLL in open loop mode	-	33	45	mA
Icc(synth)	Synthesizer supply current	.	-	0.7	4.5	mA
Icc(pd)	Power down supply current	.	-	4	10	uA
$f_{o(RF)}$	RF output frequency	.	1880	-	1930	MHz
T_{amb}	Ambiant temperature	.	-10	-	+60	°C
Synthesizer						
f_{XTAL}	Crystal reference input frequency	Depends on programming	-	10.368 or 13.824	-	MHz
R_{REF}	Reference divider ratio	.	-	12 or 16	-	.
V_{xtal}	Signal input level (peak to peak)	Square-wave	300	-	1000	mV
f_{PC}	Phase comparator frequency	.	-	0.864	-	MHz
Iocp	Charge-Pump output current	Vcp = 1/2 Vcc	-	3.5	-	mA
CSR864	Carrier to -864kHz spurious level ratio	over $f_{o(RF)}$	-	-60	-40	dBc
Tlock	Minimum time for PLL locking	From F0 reaching F9±10kHz	-	-	300	us
External regulator						
Vbat	3 batteries output voltage	.	3.2	3.6	5.5	V
Vsup	regulated output voltage	.	2.65	2.8	3.6	V
Vdrop	voltage drop from Icc=50mA to Icc=350mA	for Vbat = 3.6V	-	5	100	mV
VCO						
F_{VCO}	oscillator frequency defined at TX output	over full temperature	1880	-	1930	MHz
V_{VTUNE}	Charge Pump in- & Tuning output	.	0.4	-	Vcc-0.4	V
G_{VCO}	mean VCO tuning input gain	defined at TX output over the DECT band	-	60	-	MHz/V
G_{MOD}	VCO modulation input gain	defined at TX output over the DECT band for V_{TGFSK} = 0.5 V_{DC}	-	1.65	-	MHz/V
Z_{MOD}	VCO modulation input impedance	In TX mode only [1]	-	15	-	kOhm

[1] In RX mode, this pin is high impedance for an eventual connection to RSSI pin.

TX PREAMPLIFIER						
$Po_{(TX)}$	TX preamplifier output power (with bit tpow1 = 0)	at Tamb = 25°C	0.5	+3	+6	dBm
		over full temperature	-1	+3	+7	dBm
$FTVCO_{TX}$	VCO feed through at TX output	Referred to $Po_{(TX)}$ measured at 1.9GHz	-	-35	-20	dBc
RoTX	Parallel reel part of the impedance	measured at 1.9GHz	-	300	-	Ohm
CoTX	Parallel imaginary part of the impedance	measured at 1.9GHz	-	0.1	-	pF
CNR250k	carrier-to-noise ratio at TX output carrier offset	Df =250 kHz in open loop	-	-107	-87	dBc/Hz
CNR4684k	carrier-to-noise ratio at TX output carrier offset	Df = 4684 kHz In open loop	-	-132	-126	dBc/Hz
CNR6412k	carrier-to-noise ratio at TX output carrier offset	Df = 6412kHz In open loop	-	-136	-129	dBc/Hz
$Dfo_{(Pushing)}$	frequency shift due to 100mV drop on supply	V_{VTUNE} set by the PLL on f_{VCO} = 1.9 GHz. V_{TGFSK} = 0 V and a 50 Ω TX load.	-	0	+10	kHz
$Dfo_{(Pulling)}$	frequency shift due to disabling the synthesizer (measured 20 μs after disabling the synthesizer)	V_{VTUNE} set by the PLL on f_{VCO} = 1.9 GHz. V_{TGFSK} = 0 V and a 50 Ω TX load.	-	0	+/-15	kHz
$Dfo_{(DRIFT)}$	frequency drift	V_{VTUNE} set by the PLL on f_{VCO} = 1.9 GHz. measured during 500 us	-	0	10	kHz
RECEIVER						
All performances are measured at the receiver balun input, and a 3dB loss is assumed for the path to the antenna. The values expressed in dBc refer to the wanted signal level and are positive for interfering signals higher than the wanted signal.						
$Vmax_{RSSI}$	Maximum RSSI output voltage under high RX input signal level	.	-	1.65	2.0	V
V_{RSSI}	RSSI output voltage. Monotonic over range -96dBm to -36dBm	with -30 dBm	1.1	1.4	1.75	V
		with -60 dBm	0.8	0.95	1.15	V
		with -90 dBm	-	0.45	0.65	V
Ton	wake up time from the power up signal to correct RSSI output	RSSI signal reach its final value ±150mV at –60 dBm input level [2]	-	20	40	us
SB-3	sensitivity at input for BER < 10^{-3}	.	-	-96	-93	dBm
SB-5	power range for BER < 10^{-5}	.	+12	-	-76	dBm
IM3	Intermodulation rejection for BER < 10^{-3}	Wanted @-83dBm; level of interferers in channels N+2 and N+4	+33	+44	-	dBc
Rco	co-channel rejection for BER<10^{-3}	Wanted @-76dBm	-10	-8	-	dBc

[2] Measured without parallel capacitor on RSSI pin.

RN+/-1	Adjacent channel rejection for BER<10^{-3}	Wanted @-76dBm	+13	+22	-	dBc
RN+/-2	Bi-Adjacent channel rejection for BER<10^{-3}	Wanted @-76dBm	+34	+42	-	dBc
RN+/->3	Rejection with ≥3 channel spacing for BER<10^{-3}	Wanted @-76dBm	+40	+45	-	dBc
BLnear	Rejection of a blocking signal in the range 5MHz to 100MHz from the band	Wanted @-83dBm	+47	+56	-	dBc
BLfar	Rejection of a blocking signal at 100MHz from the band	Wanted @-83dBm	+59	+65	-	dBc
RoRX	Parallel reel part of the impedance	measured at 1.9GHz	-	65	-	Ohm
CoRX	Parallel imaginary part of the impedance	measured at 1.9GHz	-	1.5	-	pF
LOGIC INTERFACE						
Vih	HIGH level input voltage	.	1.4	-	Vcc +0.6	V
Vil	LOW level input voltage	.	0	-	+0.4	V
Ibias	Input bias current logic 1 or logic 0	.	-5	-	+5	uA
Voh	HIGH level output voltage	For RDATA output	2.0	2.4	2.7	V
Vol	LOW level output voltage	For RDATA output	-	-	0.4	V
tt	Transition time on R_DATAP 10%↔90%	with 30pF load	-	70	-	ns
Ioh	Source output current capability	In high level state on RON or TON pins into Vdc = 0.7V	8	22		mA
Iol	Sink output current capability	In low level state on RON or TON pins into Vdc = Vcc - 0.7V	8	22	-	mA
F_{S_CLK}	Programming frequency	.	-	-	14	MHz
ta, tb	S_DATA settling and maintain time	from S_CLK	30	-	-	ns
tc	Last S_CLK to S_EN latch-in time	.	1	-	-	us
td	S_EN to TON (or RON) time	Bit ppaon = ‘0’	-	0.5	-	us
te	S_EN stop pulse width	.	1	-	-	us
tf	Timing from Start signal to first S_CLK edge	in mode 4	1	-	-	us
tg	S_EN latch-in to SLCCTR rising edge in RX	Receiver settling time	20	-	-	us

TIMING DIAGRAM

Timing diagram in mode 2

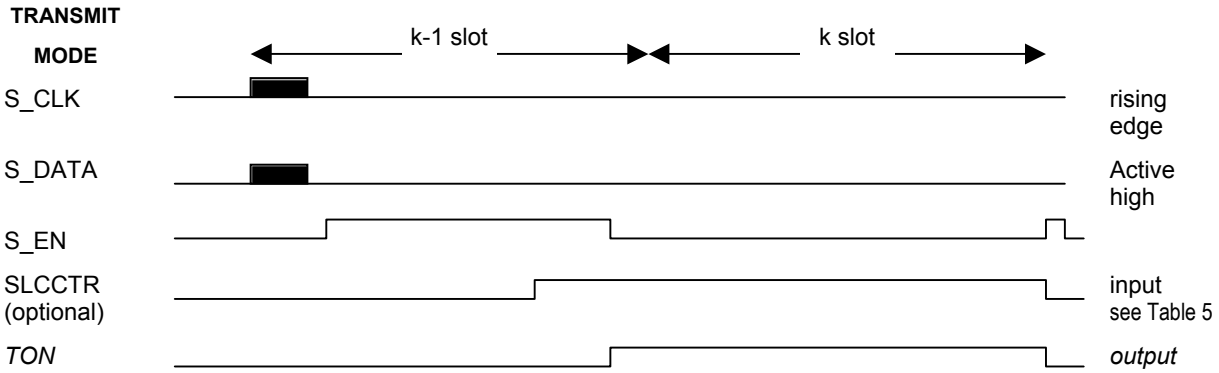


Figure 3 - Mode 2 transmit timing diagram (with the VEGA baseband family)

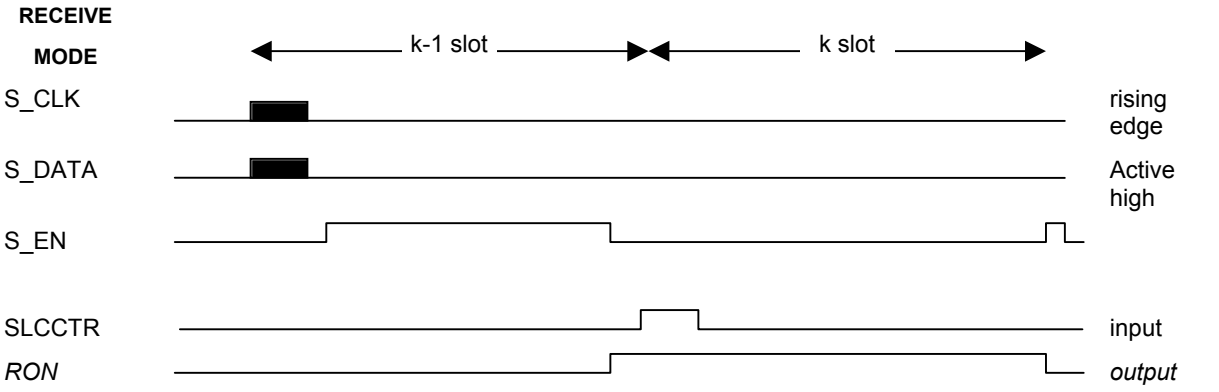


Figure 4 - Mode 2 receive timing diagram (with the VEGA baseband family)

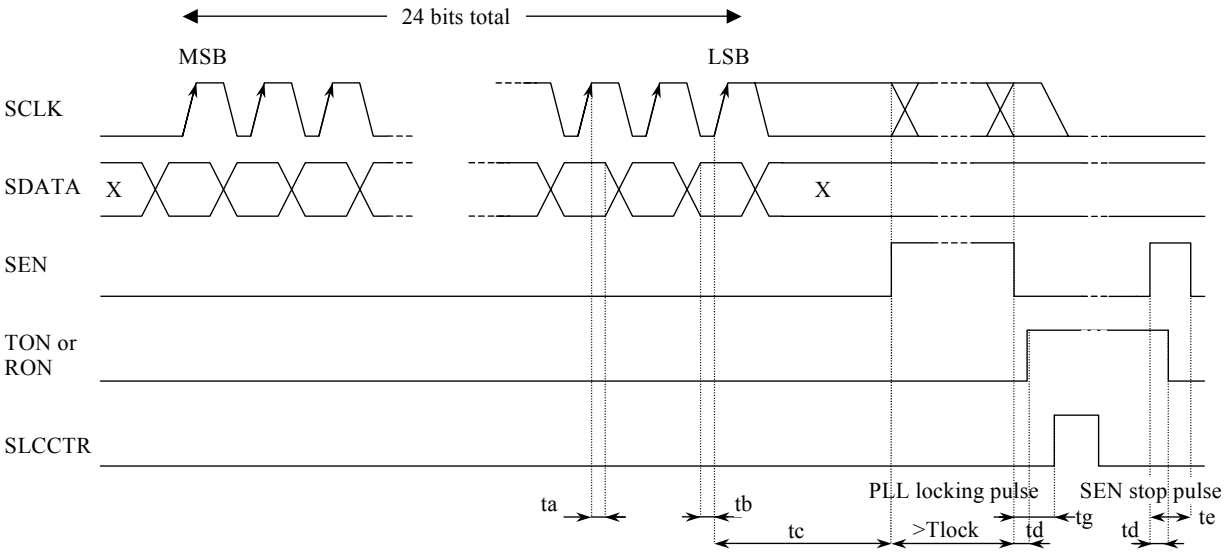


Figure 5 - Mode 2 programming signal timing diagram

Timing diagram in mode 3

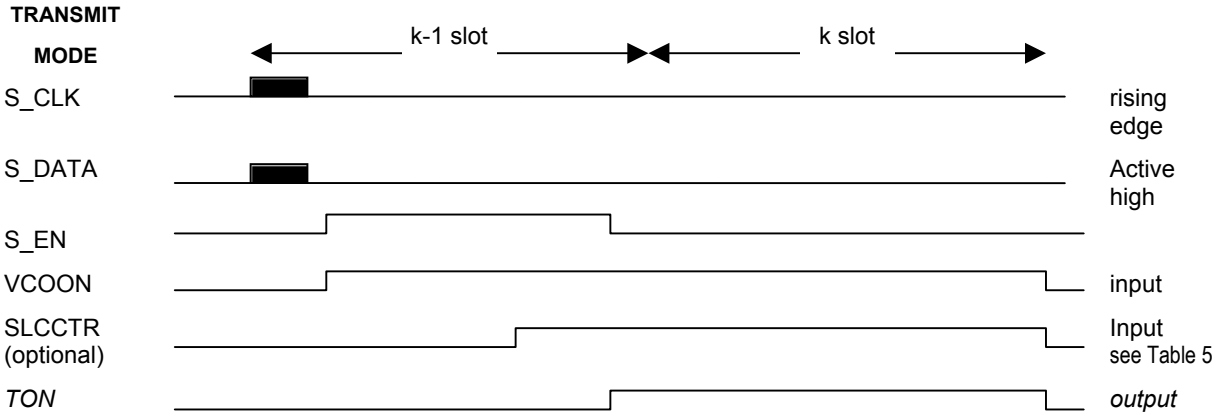


Figure 6 - Mode 3 transmit timing diagram (with the ABC baseband family)

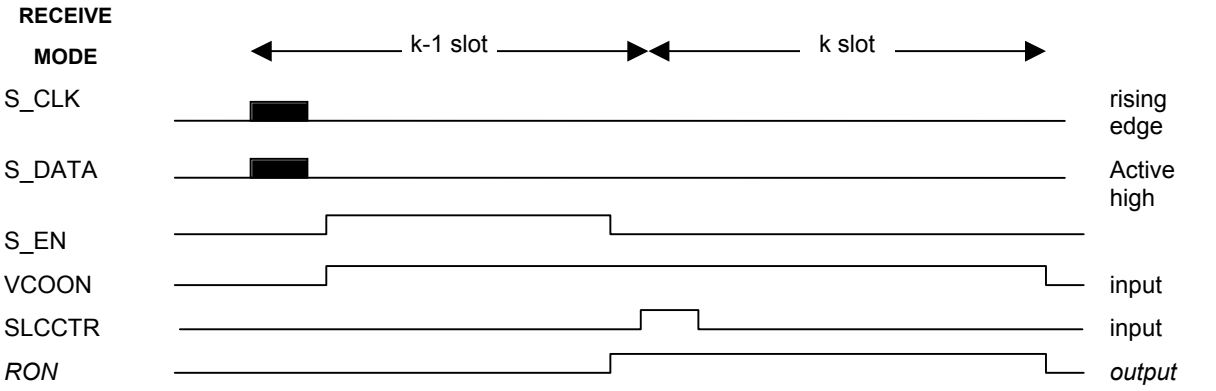


Figure 7 - Mode 3 receive timing diagram (with the ABC baseband family)

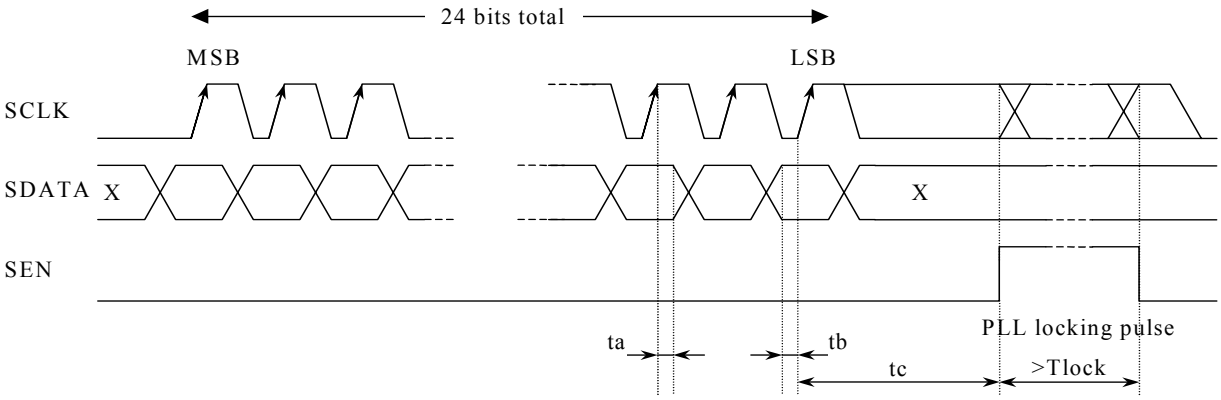


Figure 8 - Mode 3 programming signal timing diagram

Timing diagram in mode 4

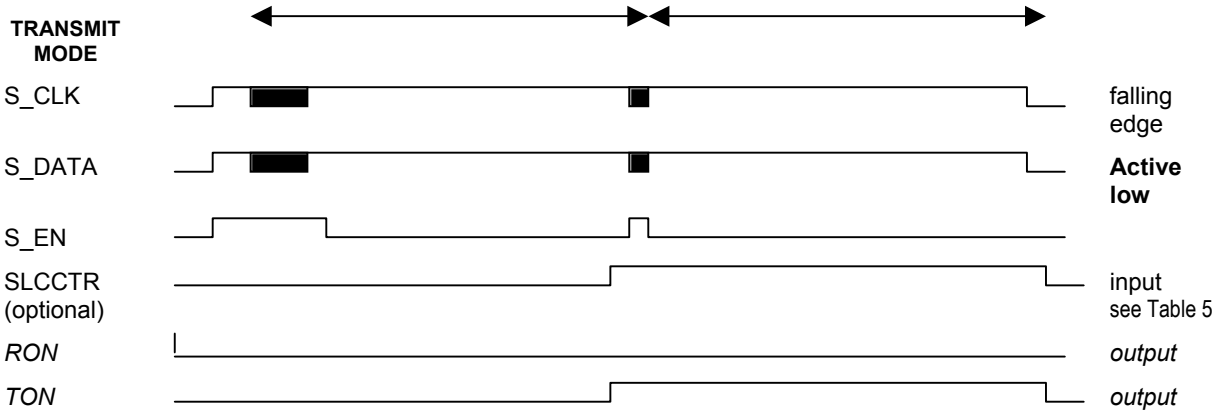


Figure 9 - Mode 4 transmit timing diagram

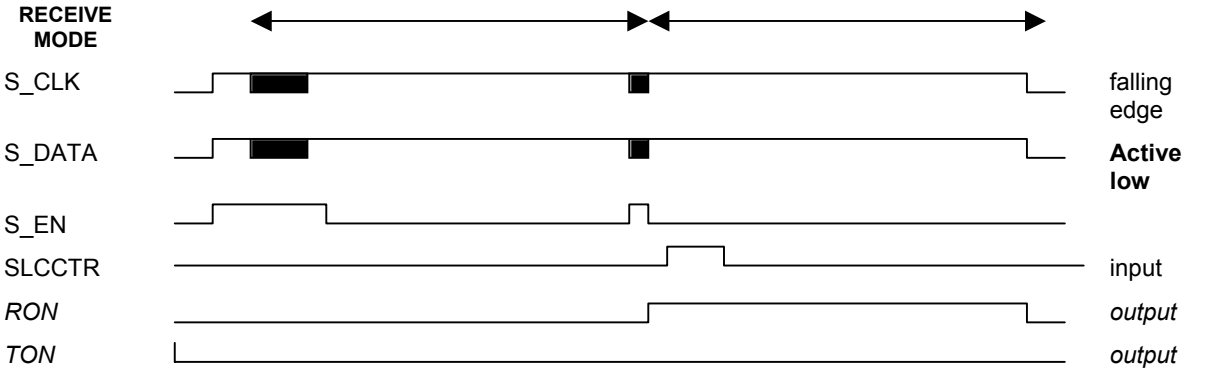


Figure 10 - Mode 4 receive timing diagram

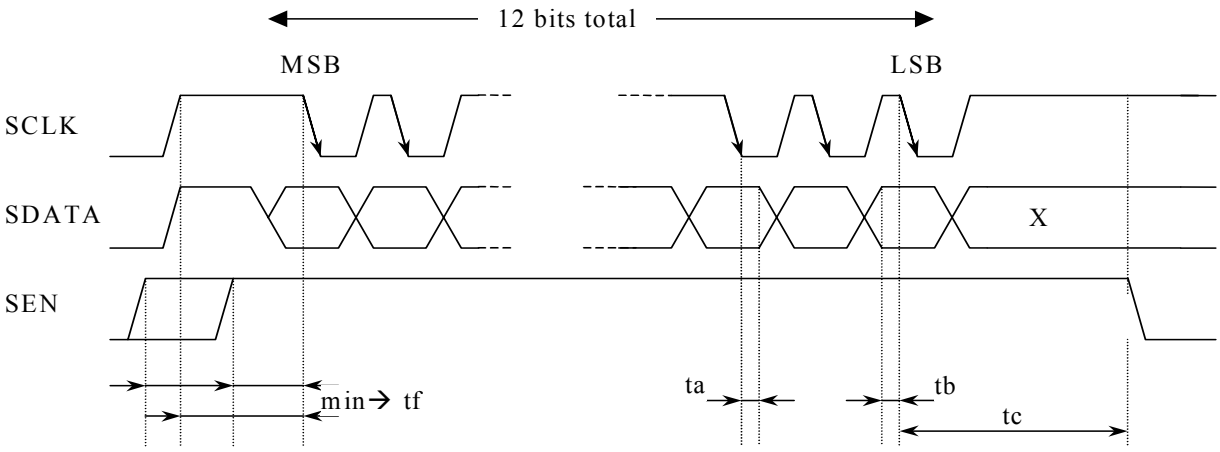


Figure 11 - Mode 4 programming signal timing diagram

SCHEMATIC

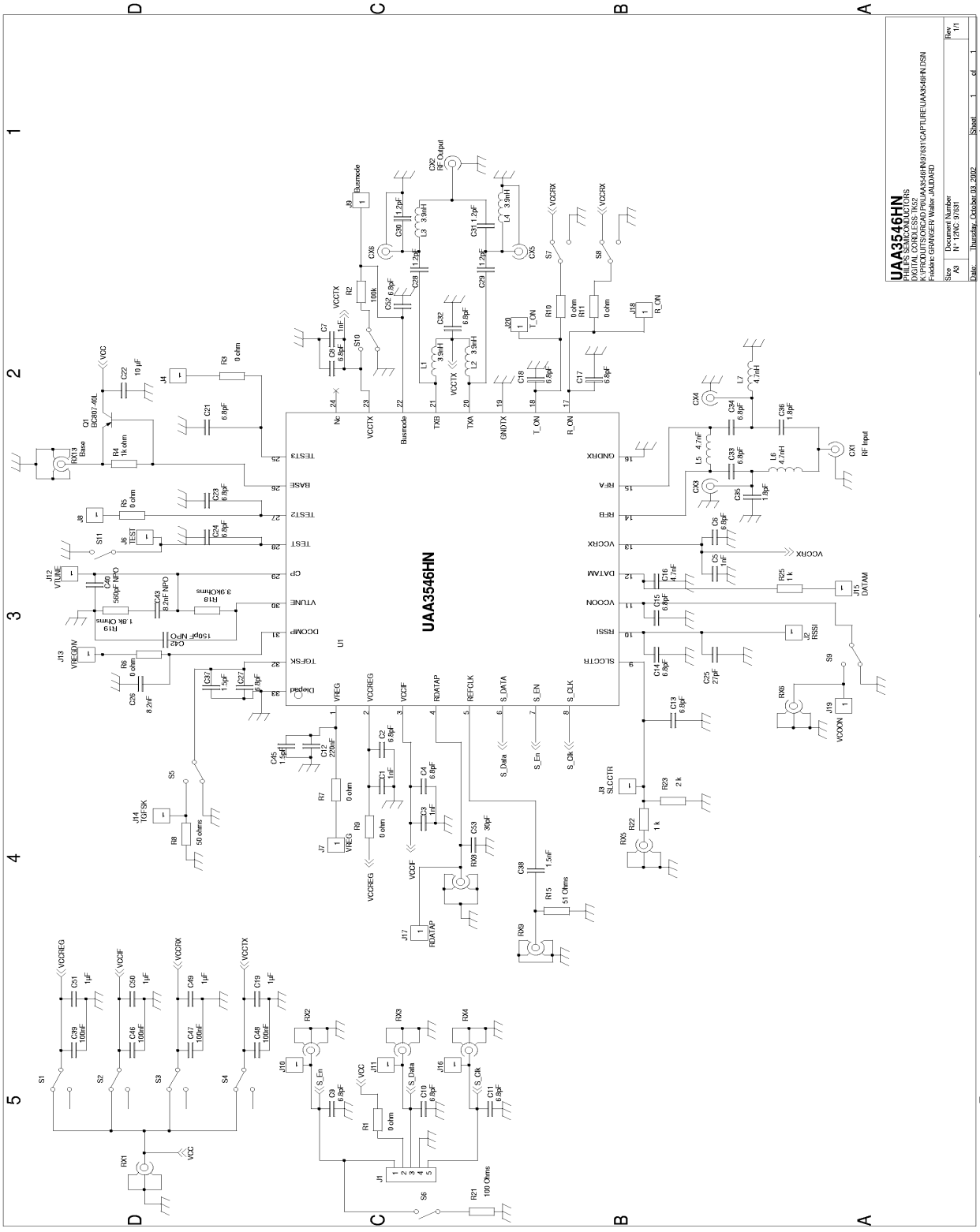


Figure 12 - Characterization board schematic

BOARD LAYOUT

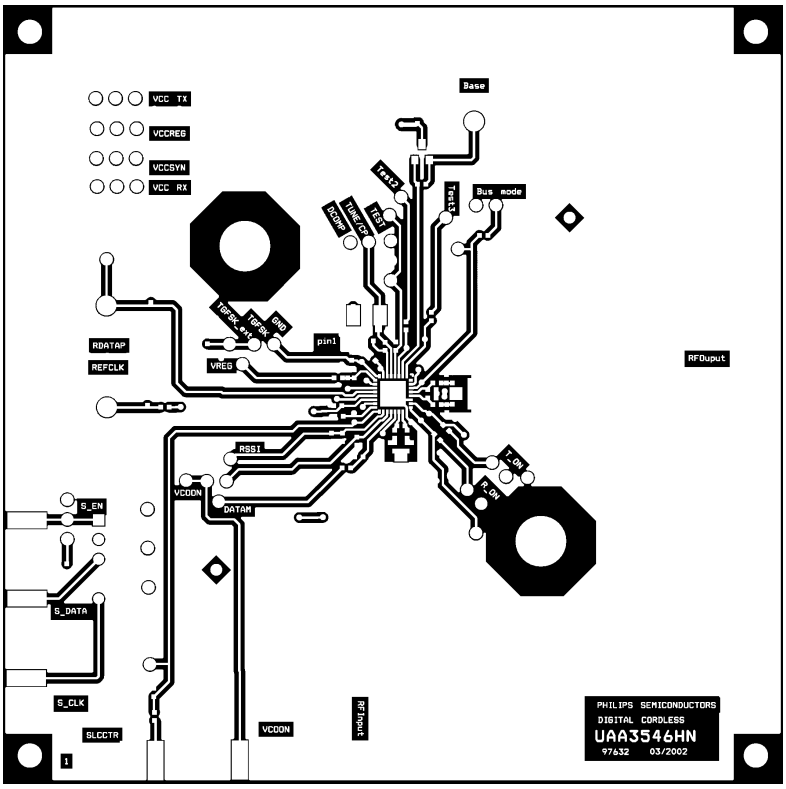


Figure 13 - Top layer (negative)

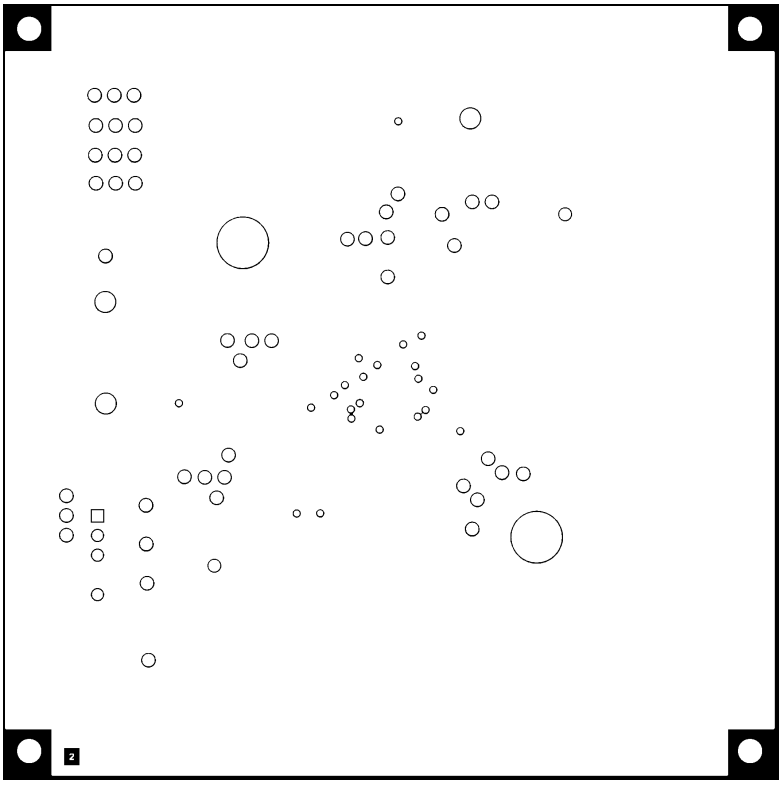


Figure 14 - Internal top layer (negative)

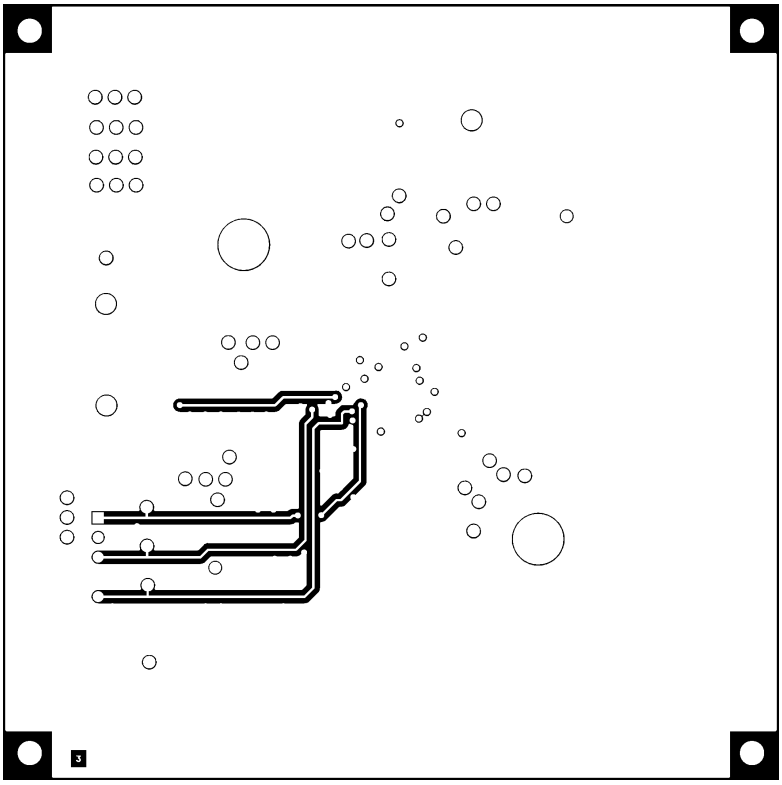


Figure 15 - Internal bottom layer (negative)

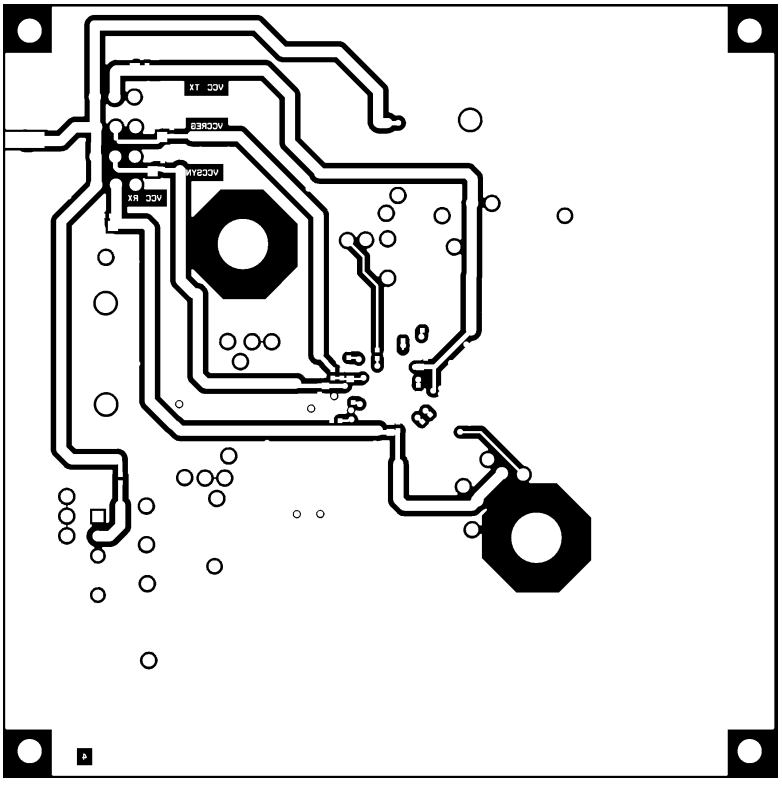


Figure 16 - Bottom layer (negative)

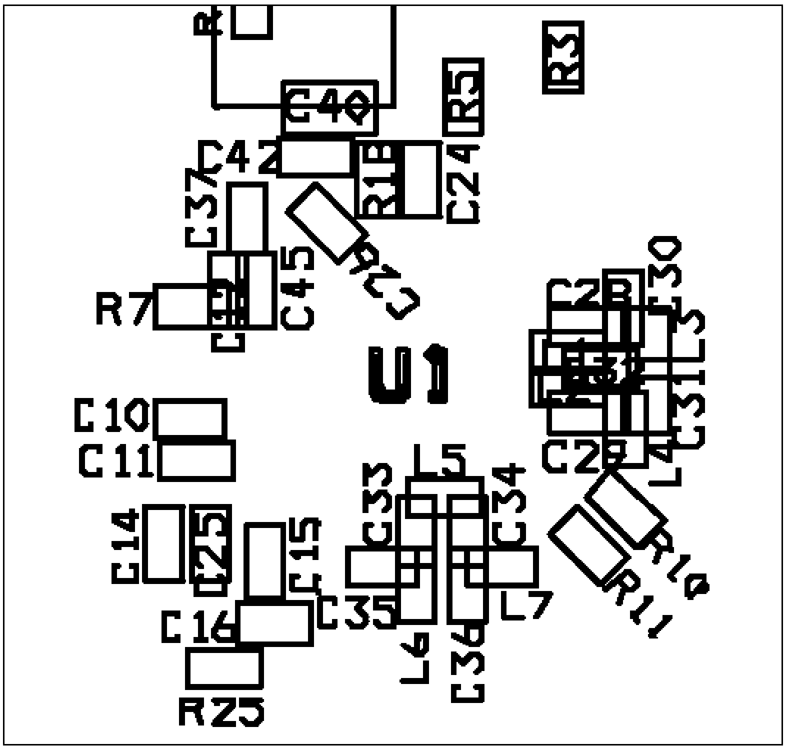


Figure 17 - Top layer components (zoom)

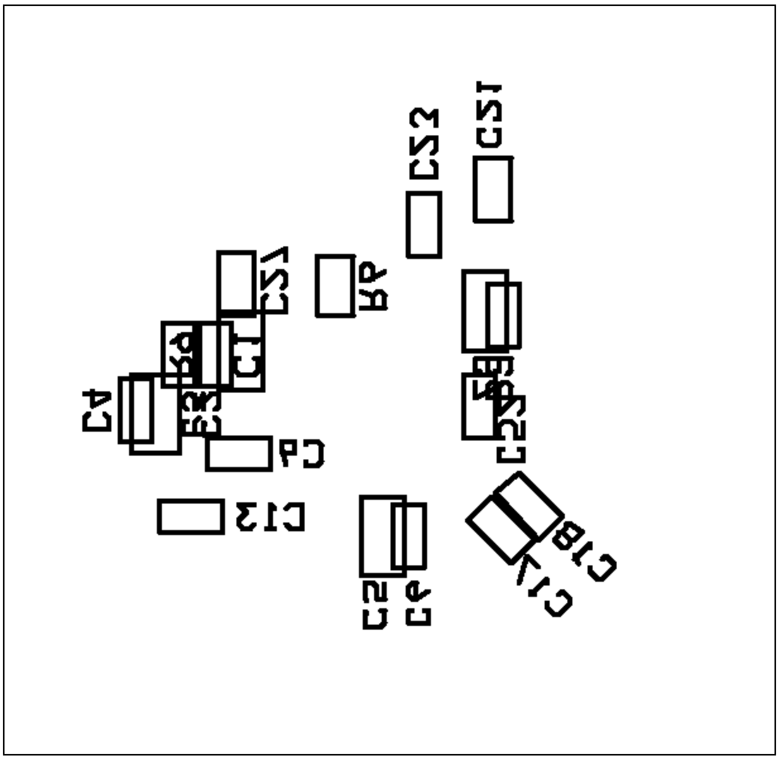


Figure 18 - Bottom layer components (zoom)

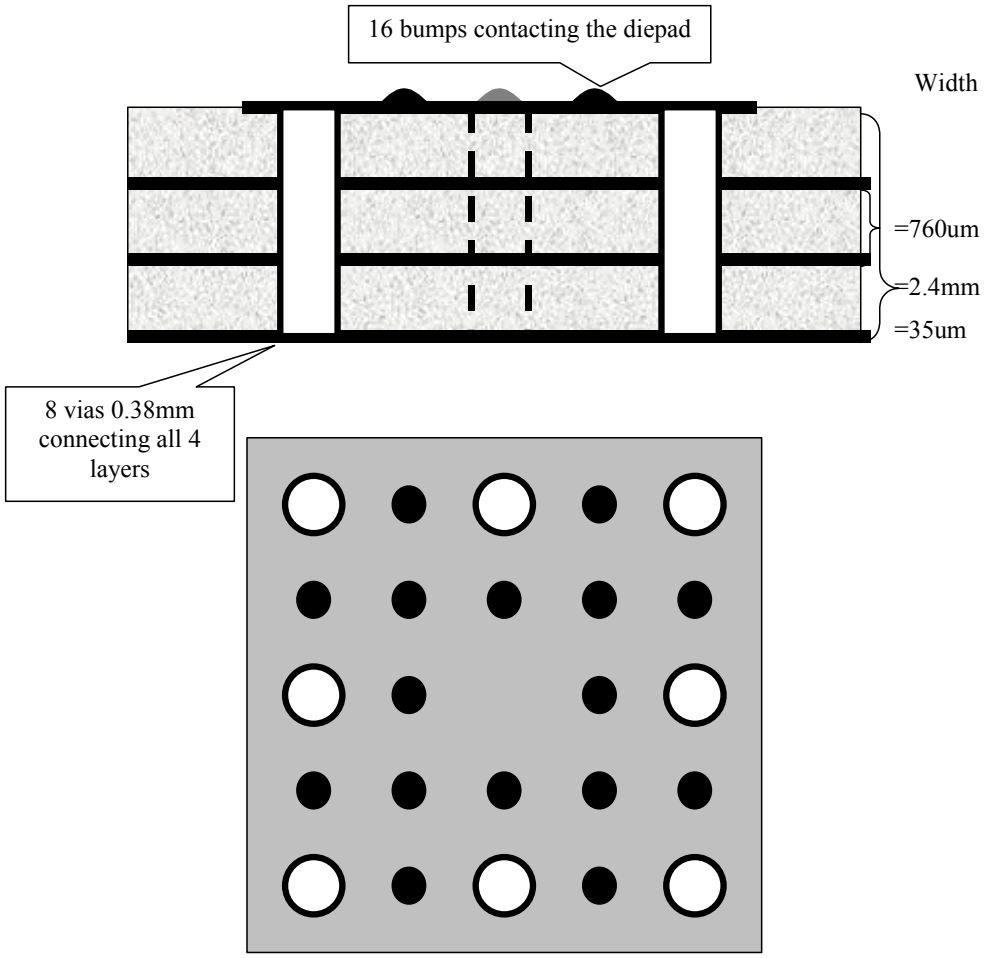


Figure 19 - PCB description under the IC diepad

RX IMPEDANCE

Measured under low level signal at pin outputs; the coupling capacitors and PCB effects are de-embedded.

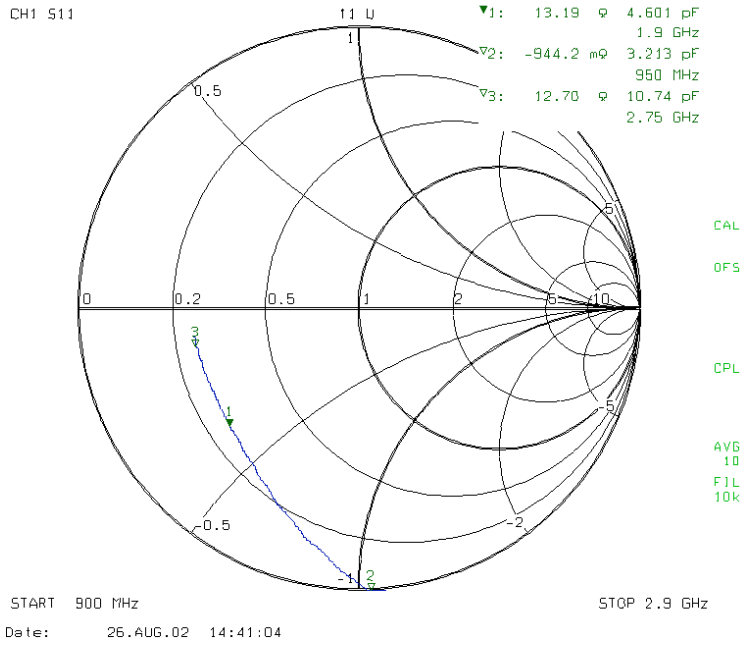


Figure 20 - serial RX half differential input impedance at RFA/RFB

TX IMPEDANCE

Measured under high signal level (+3dBm typ) at pin outputs; the coils to VCC, coupling capacitors and PCB effects are de-embedded.

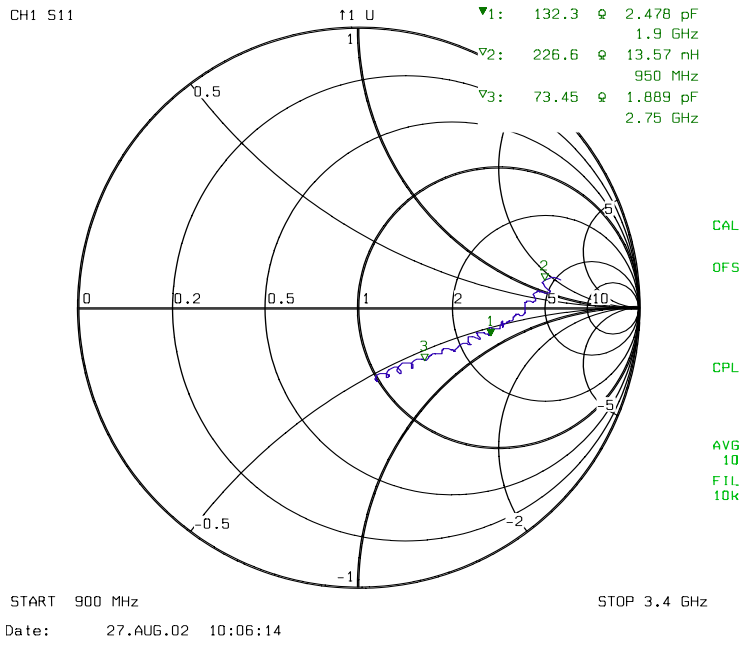


Figure 21 - serial TX half differential output impedance at TXA/TXB

TYPICAL RSSI RESPONSE

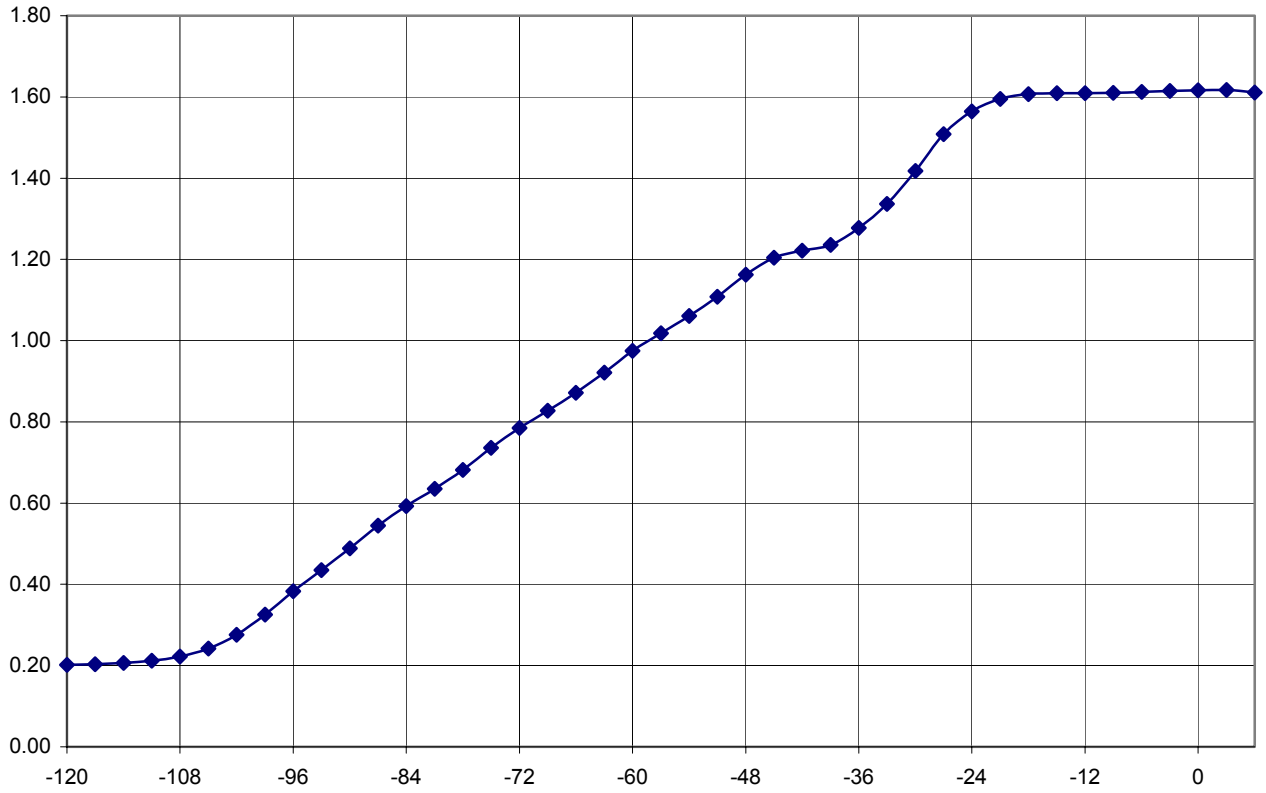
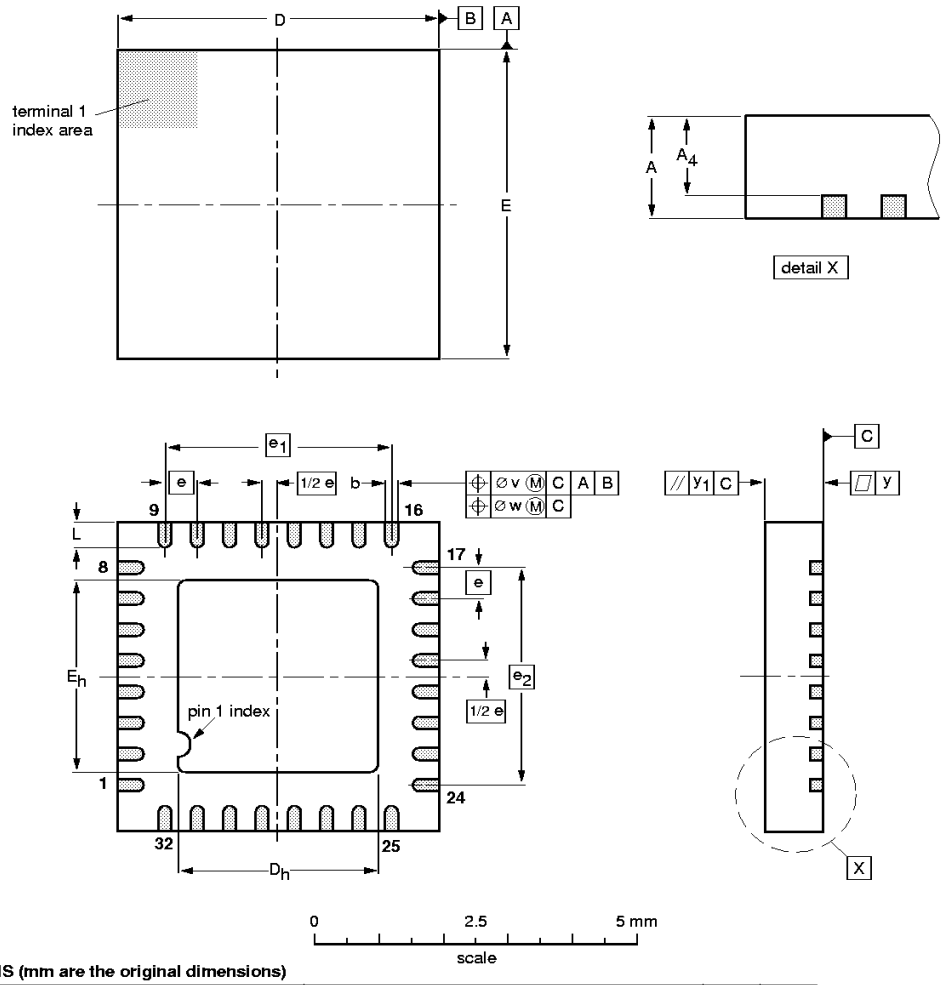


Figure 22 - Typical RSSI response

PACKAGE OUTLINE

HVQFN32: plastic, heatsink very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_4 max.	b	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1.00	0.80	0.35 0.18	5.05 4.95	3.25 2.95	5.05 4.95	3.25 2.95	0.5	3.5	3.5	0.50 0.30	0.2	0.1	0.05	0.1

Note

1. Plastic or metal protrusions of 0.076 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT617-1		MO-220				~~01-06-07~~ 01-08-08

Figure 23 - HVQFN32 package outline

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our “Data Handbook IC26; Integrated Circuit Packages” (document order number 9398 652 90011). There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement. Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems. To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

– larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead.

Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW (1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable (2)	suitable
PLCC (3) , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended (3)(4)	suitable
SSOP, TSSOP, VSO	not recommended (5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”

2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 m; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT	STATUS DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification

The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes

Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.