intersil®

HFA1109

450MHz, Low Power, Current Feedback Video Operational Amplifier

August 2004

Features

- **Wide - 3dB Bandwidth (A_V = +2). 450MHz**
- **Gain Flatness (To 250MHz) 0.8dB**
- **Very Fast Slew Rate (A_V = +2) 1100V/μs**
- **High Input Impedance 1.7MΩ**
- **Differential Gain/Phase . . . . 0.02%/0.02 Degrees**
- **Low Supply Current 10mA**

Applications

- **Professional Video Processing**
- **Video Switchers and Routers**
- **Medical Imaging**
- **PC Multimedia Systems**
- **Video Distribution Amplifiers**
- **Flash Converter Drivers**
- **Radar/IF Processing**

Description

The HFA1109 is a high speed, low power, current feedback amplifier built with Intersil's proprietary complementary bipolar UHF-1 process. This amplifier features a unique combination of power and performance specifically tailored for video applications.

The HFA1109 is a standard pinout op amp. It is a higher performance, drop-in replacement (no feedback resistor change required) for the CLC409.

If a comparably performing op amp with an output disable function (useful for video multiplexing) is required, please refer to the HFA1149 data sheet.

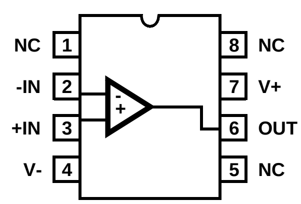
Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1109IB (H1109)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL (Note)	DIP Evaluation Board for High Speed Op Amps		

NOTE: Requires a SOIC-to-DIP adapter. See "Evaluation Board" section inside.

Pinout

HFA1109 (SOIC)
TOP VIEW



FN4019.4

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle

ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 1400V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) . . 2000V
Machine Model (Per EIAJ ED-4701Method C-111) 50V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOIC Package. 170
Maximum Junction Temperature (Die) . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s). . . . . 300^oC
(Lead Tips Only)

Operating Conditions

Temperature Range . . . . -40^oC to 85^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +2, R_F = 250Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	1	5	mV
		A	Full	-	2	8	mV
Average Input Offset Voltage Drift		B	Full	-	10	-	μV/^oC
Input Offset Voltage Common-Mode Rejection Ratio	ΔV_{CM} = ±2V	A	25	47	50	-	dB
	ΔV_{CM} = ±2V	A	Full	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV_{PS} = ±1.25V	A	25	50	53	-	dB
	ΔV_{PS} = ±1.25V	A	Full	47	51	-	dB
Non-Inverting Input Bias Current		A	25	-	4	10	μA
		A	Full	-	5	15	μA
Non-Inverting Input Bias Current Drift		B	Full	-	30	-	nA/^oC
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.25V	A	25	-	0.5	1	μA/V
	ΔV_{PS} = ±1.25V	A	Full	-	0.5	3	μA/V
Inverting Input Bias Current		A	25	-	2	10	μA
		A	Full	-	3	15	μA
Inverting Input Bias Current Drift		B	Full	-	40	-	nA/^oC
Inverting Input Bias Current Common-Mode Sensitivity	ΔV_{CM} = ±2V	A	25	-	3	6	μA/V
	ΔV_{CM} = ±2V	A	Full	-	3	8	μA/V
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.25V	A	25	-	1.6	5	μA/V
	ΔV_{PS} = ±1.25V	A	Full	-	1.6	8	μA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±2V	A	25, 85	0.8	1.7	-	MΩ
	ΔV_{CM} = ±2V	A	-40	0.5	1.4	-	MΩ
Inverting Input Resistance		B	25	-	60	-	Ω
Input Capacitance		B	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	Full	±2	±2.5	-	V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +2, R_F = 250Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Input Noise Voltage Density (Note 4)	f = 100kHz	B	25	-	4	-	nV/√Hz
Non-Inverting Input Noise Current Density (Note 4)	f = 100kHz	B	25	-	2.4	-	pA/√Hz
Inverting Input Noise Current Density (Note 4)	f = 100kHz	B	25	-	40	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (Note 4)		B	25	-	500	-	kΩ
Minimum Stable Gain		B	Full	-	1	-	V/V
AC CHARACTERISTICS							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 4)	A_V = -1, R_F = 200Ω	B	25	300	375	-	MHz
		B	Full	290	360	-	MHz
	A_V = +1, +R_S = 550Ω (PDIP), +R_S = 700Ω (SOIC)	B	25	280	330	-	MHz
		B	Full	260	320	-	MHz
	A_V = +2	B	25	390	450	-	MHz
		B	Full	350	410	-	MHz
Gain Peaking	A_V = +2, V_{OUT} = 0.2V_{P-P}	B	25	-	0	0.2	dB
		B	Full	-	0	0.5	dB
Gain Flatness (A_V = +2, V_{OUT} = 0.2V_{P-P}, Note 4)	To 125MHz	B	25	-1.0	-0.45	-	dB
		B	Full	-1.1	-0.45	-	dB
	To 200MHz	B	25	-1.6	-0.75	-	dB
		B	Full	-1.7	-0.75	-	dB
	To 250MHz	B	25	-1.9	-0.85	-	dB
		B	Full	-2.2	-0.85	-	dB
Gain Flatness (A_V = +1, +R_S = 550Ω (PDIP), +R_S = 700Ω (SOIC), V_{OUT} = 0.2V_{P-P}, Note 4)	To 125MHz	B	25	±0.3	±0.1	-	dB
		B	Full	±0.4	±0.1	-	dB
	To 200MHz	B	25	±0.8	±0.35	-	dB
		B	Full	±0.9	±0.35	-	dB
	To 250MHz	B	25	±1.3	±0.6	-	dB
		B	Full	±1.4	±0.6	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing, Unloaded (Note 4)	A_V = -1, R_L = ∞	A	25	±3	±3.2	-	V
		A	Full	±2.8	±3	-	V
Output Current (Note 4)	A_V = -1, R_L = 75Ω	A	25, 85	±33	±36	-	mA
		A	-40	±30	±33	-	mA
Output Short Circuit Current	A_V = -1	B	25	-	120	-	mA
Closed Loop Output Resistance (Note 4)	DC, A_V = +1	B	25	-	0.05	-	Ω
Second Harmonic Distortion (V_{OUT} = 2V_{P-P}, Note 4)	20MHz	B	25	-	-55	-	dBc
	60MHz	B	25	-	-57	-	dBc
Third Harmonic Distortion (V_{OUT} = 2V_{P-P}, Note 4)	20MHz	B	25	-	-68	-	dBc
	60MHz	B	25	-	-60	-	dBc
Reverse Isolation (S_{12})	30MHz	B	25	-	-65	-	dB

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +2, R_F = 250Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
TRANSIENT CHARACTERISTICS							
Rise and Fall Times	V_{OUT} = 0.5V_{P-P}	B	25	-	1.1	1.3	ns
		B	Full	-	1.1	1.4	ns
Overshoot	V_{OUT} = 0.5V_{P-P}	B	25	-	0	2	%
		B	Full	-	0.5	5	%
Slew Rate	A_V = -1, R_F = 200Ω V_{OUT} = 5V_{P-P}	B	25	2300	2600	-	V/µs
		B	Full	2200	2500	-	V/µs
	A_V = +1, V_{OUT} = 4V_{P-P}, +R_S = 550Ω (PDIP), +R_S = 700Ω (SOIC)	B	25	475	550	-	V/µs
		B	Full	430	500	-	V/µs
	A_V = +2, V_{OUT} = 5V_{P-P}	B	25	940	1100	-	V/µs
		B	Full	800	950	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step, Note 4)	To 0.1%	B	25	-	19	-	ns
	To 0.05%	B	25	-	23	-	ns
	To 0.01%	B	25	-	36	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	5	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	0.06	%
		B	Full	-	0.03	0.09	%
	R_L = 75Ω	B	25	-	0.04	0.09	%
		B	Full	-	0.05	0.12	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	0.06	Degrees
		B	Full	-	0.02	0.06	Degrees
	R_L = 75Ω	B	25	-	0.05	0.09	Degrees
		B	Full	-	0.06	0.13	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current (Note 4)		A	25	-	9.6	10	mA
		A	Full	-	10	11	mA

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1109 design is optimized for a 250Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

TABLE 1. OPTIMUM FEEDBACK RESISTOR

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	200	400
+1	250 (+R_S = 550Ω) PDIP 250 (+R_S = 700Ω) SOIC	350
+2	250	450
+5	100	160
+10	90	70

Table 1 lists recommended R_F values, and the expected bandwidth, for various closed loop gains. For a gain of +1, a resistor (+R_S) in series with +IN is required to reduce gain peaking and increase stability

PC Board Layout

The frequency response of this amplifier depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!** Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. Thus it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth. By decreasing R_S as C_L increases, the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases.

Evaluation Board

The performance of the HFA1105 may be evaluated using the HFA11XX Evaluation Board and a SOIC to DIP adaptor like the Aries Electronics Part Number 14-350000-10. The layout and schematic of the board are shown in Figure 1.

Please contact your local sales office for information. When evaluating this amplifier, the two 510Ω gain setting resistors on the evaluation board should be changed to 250Ω.

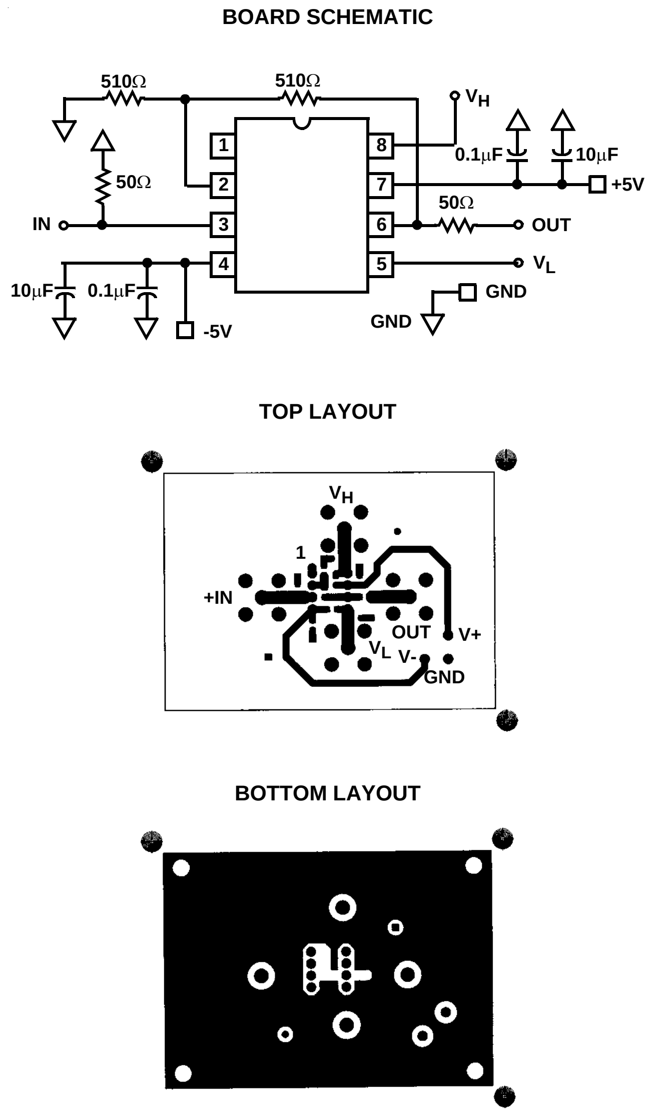


FIGURE 1. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25^{o}C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified

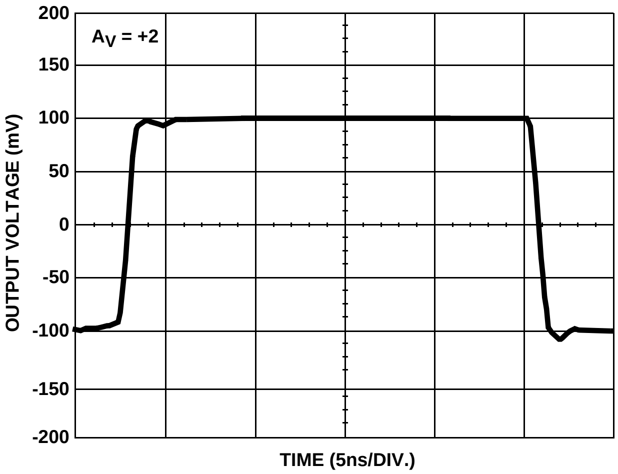


FIGURE 2. SMALL SIGNAL PULSE RESPONSE

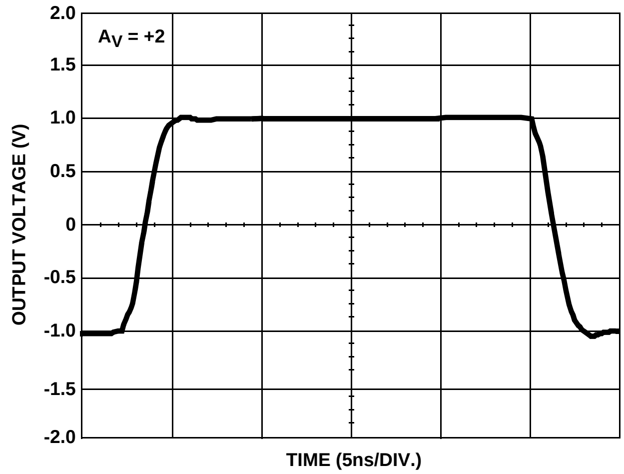


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

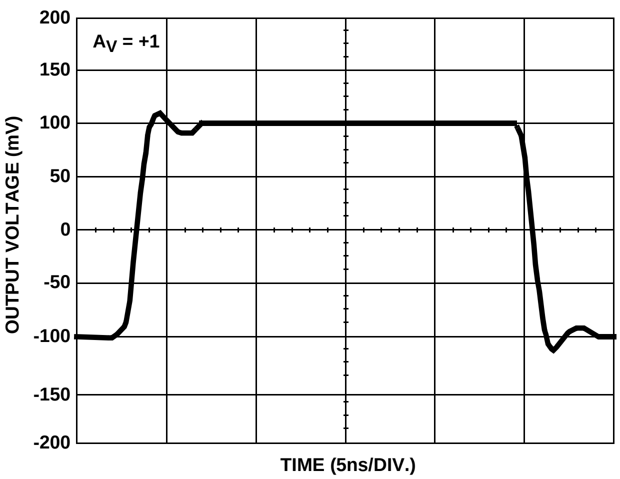


FIGURE 4. SMALL SIGNAL PULSE RESPONSE

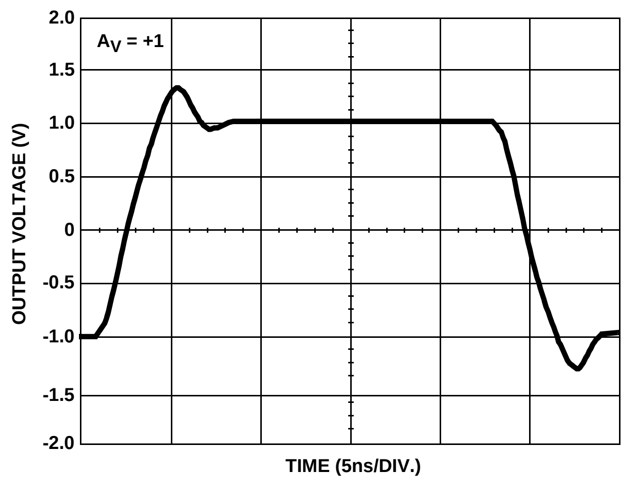


FIGURE 5. LARGE SIGNAL PULSE RESPONSE

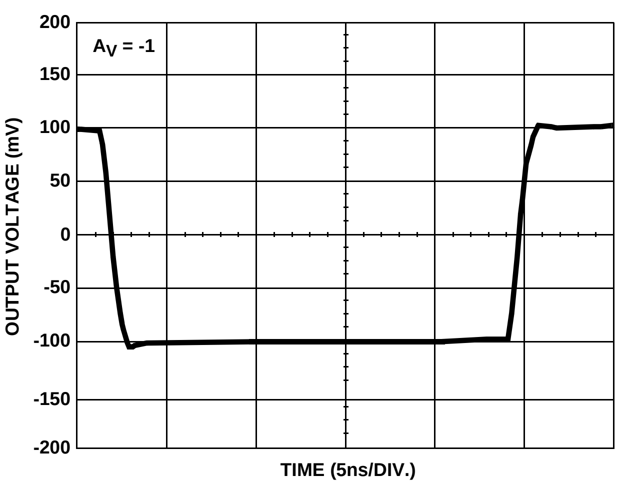


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

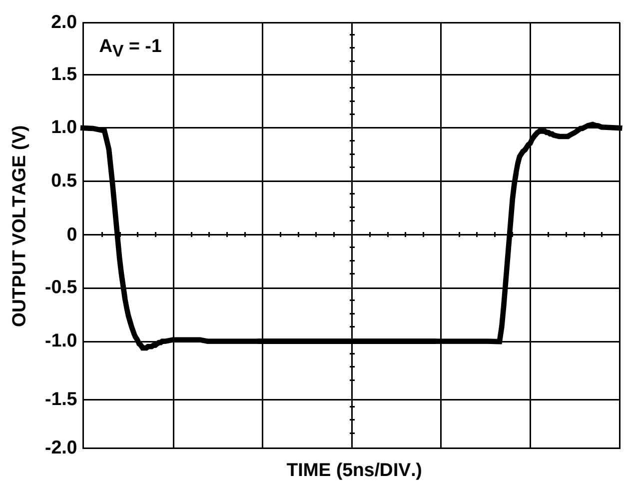


FIGURE 7. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves
$V_{SUPPLY} = \pm 5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

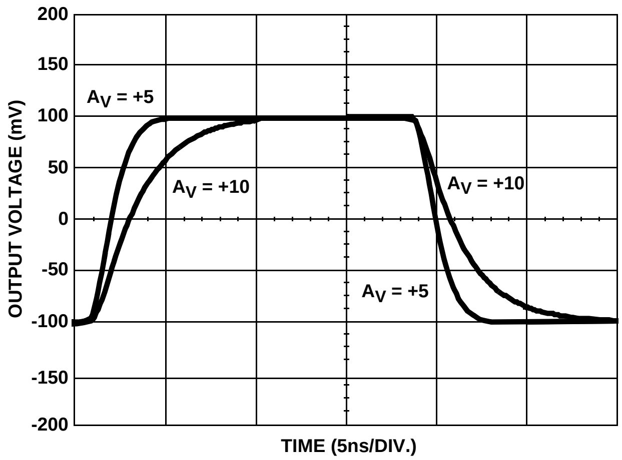


FIGURE 8. SMALL SIGNAL PULSE RESPONSE

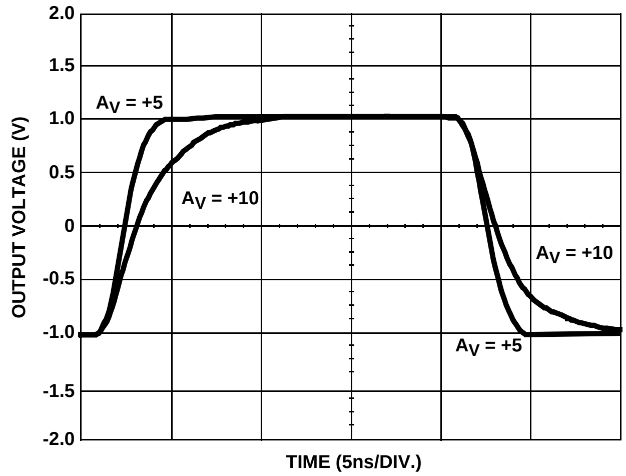


FIGURE 9. LARGE SIGNAL PULSE RESPONSE

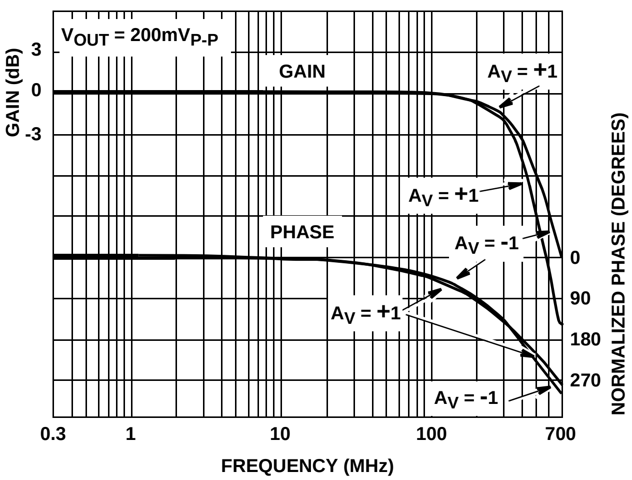


FIGURE 10. FREQUENCY RESPONSE

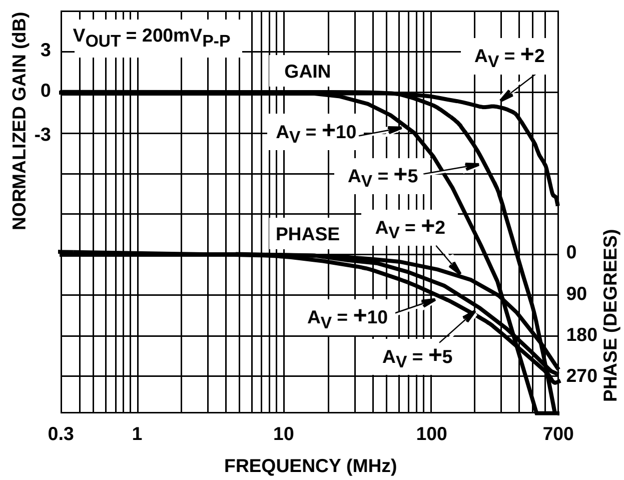


FIGURE 11. FREQUENCY RESPONSE

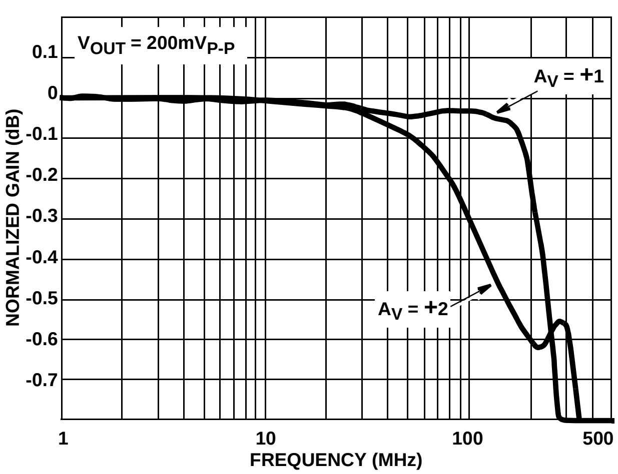


FIGURE 12. GAIN FLATNESS

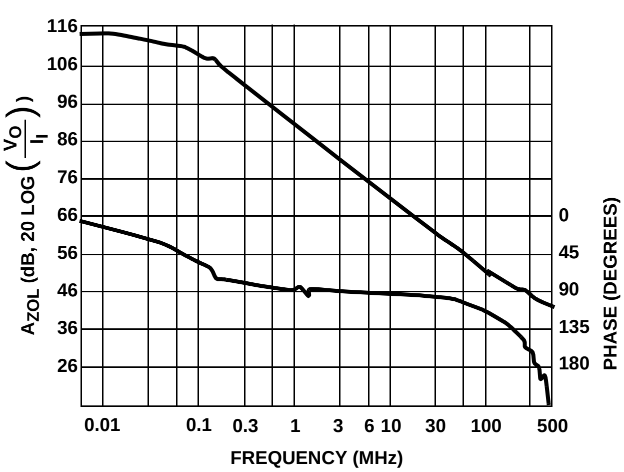


FIGURE 13. OPEN LOOP TRANSIMPEDANCE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

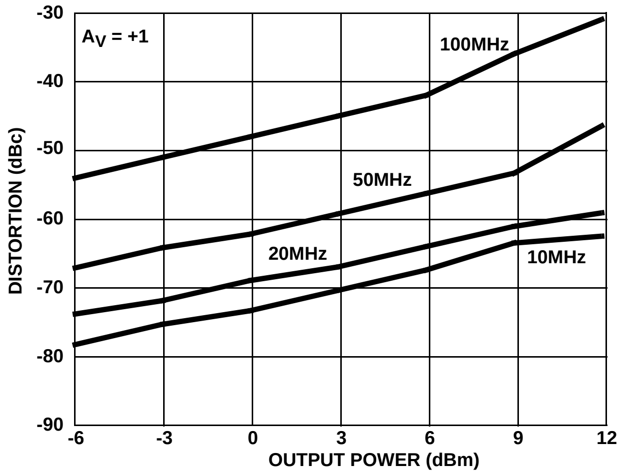


FIGURE 14. 2nd HARMONIC DISTORTION vs P_{OUT}

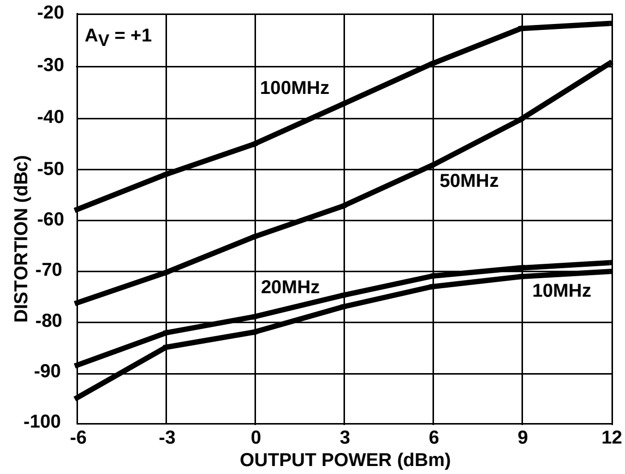


FIGURE 15. 3rd HARMONIC DISTORTION vs P_{OUT}

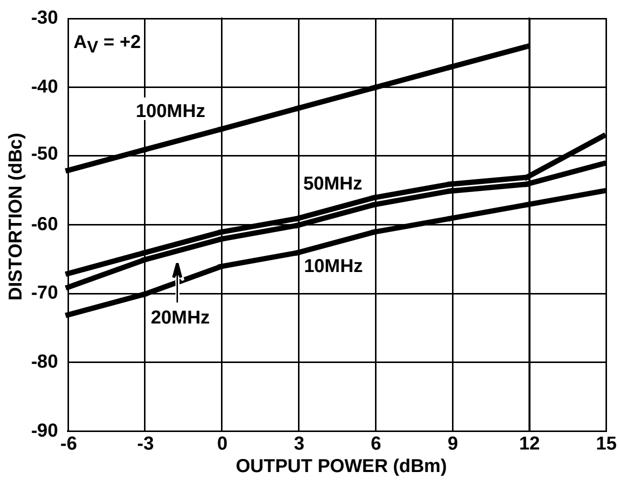


FIGURE 16. 2nd HARMONIC DISTORTION vs P_{OUT}

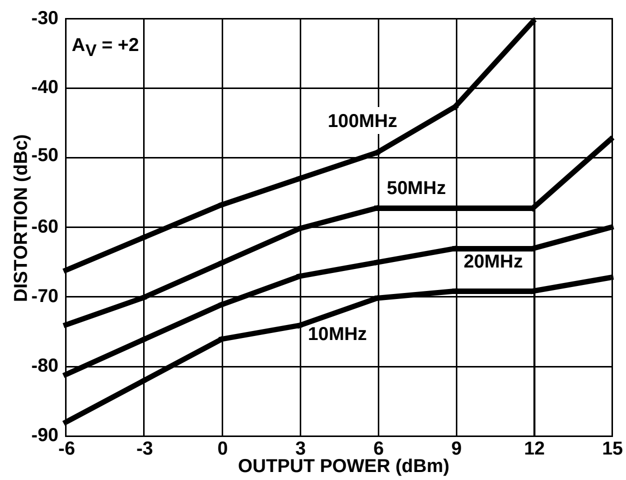


FIGURE 17. 3rd HARMONIC DISTORTION vs P_{OUT}

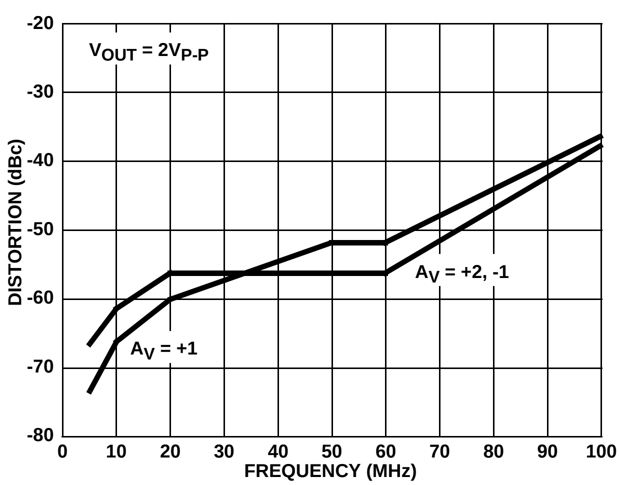


FIGURE 18. 2nd HARMONIC DISTORTION vs FREQUENCY

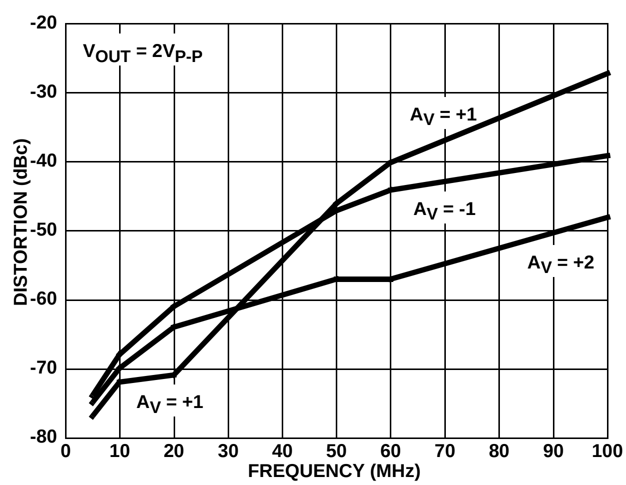


FIGURE 19. 3rd HARMONIC DISTORTION vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

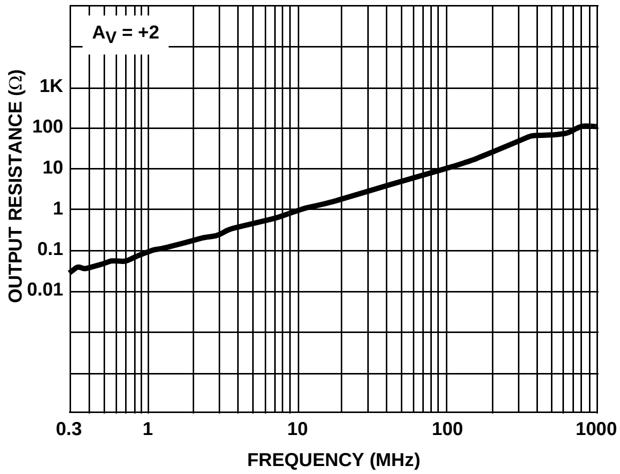


FIGURE 20. CLOSED LOOP OUTPUT RESISTANCE

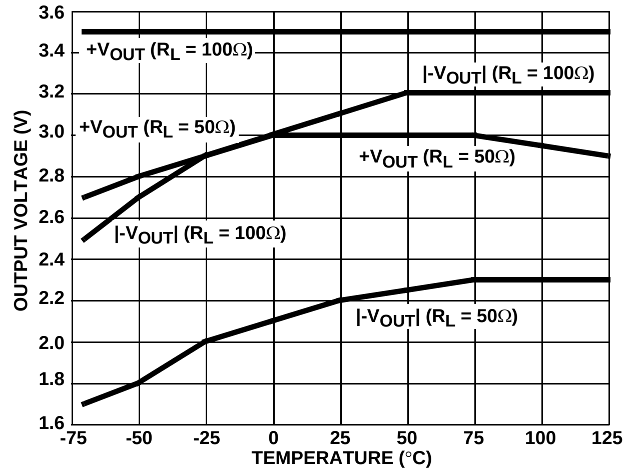


FIGURE 21. OUTPUT VOLTAGE vs TEMPERATURE

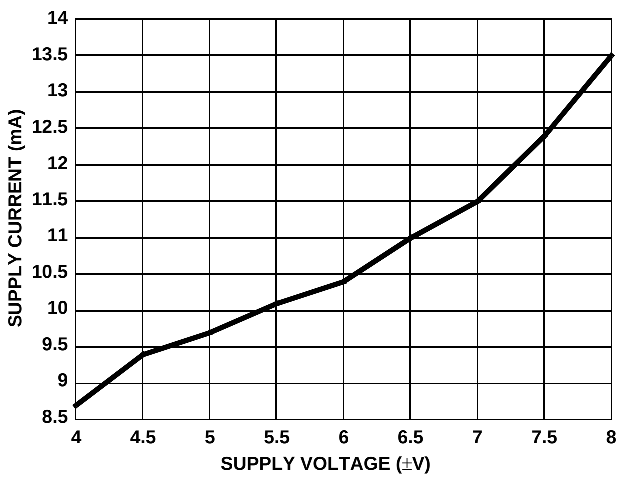


FIGURE 22. SUPPLY CURRENT vs SUPPLY VOLTAGE

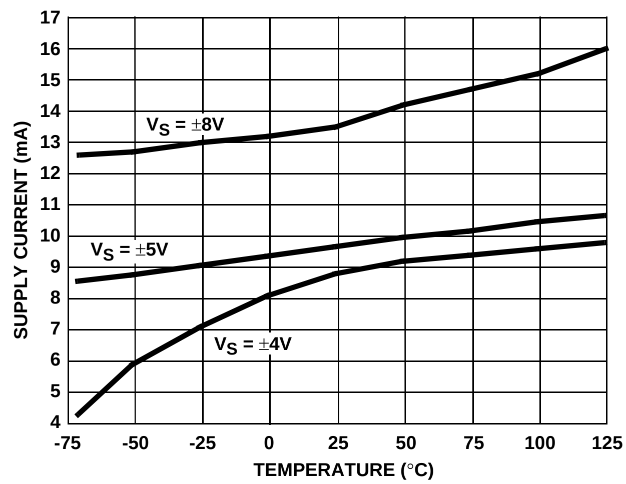


FIGURE 23. SUPPLY CURRENT vs TEMPERATURE

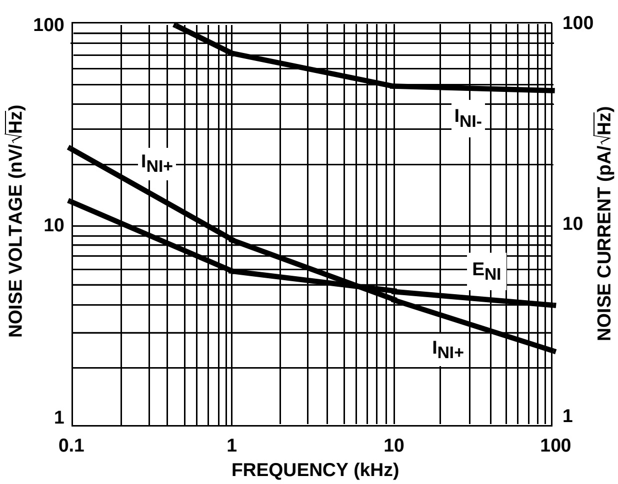


FIGURE 24. INPUT NOISE CHARACTERISTICS

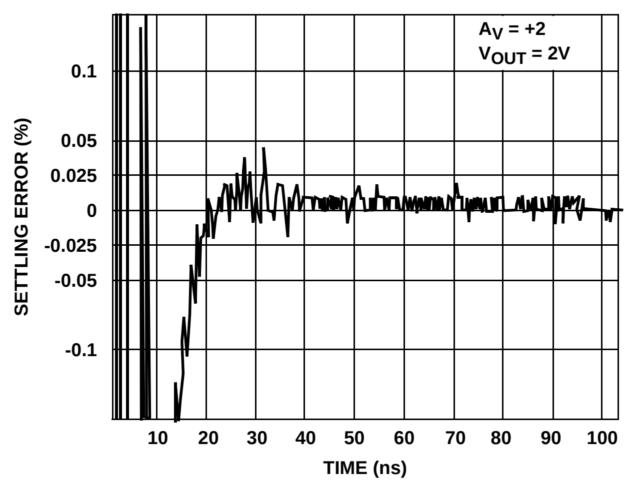


FIGURE 25. SETTLING RESPONSE

Die Characteristics

DIE DIMENSIONS:

59 mils x 80 mils x 19 mils
1500μm x 2020μm x 483μm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

GLASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

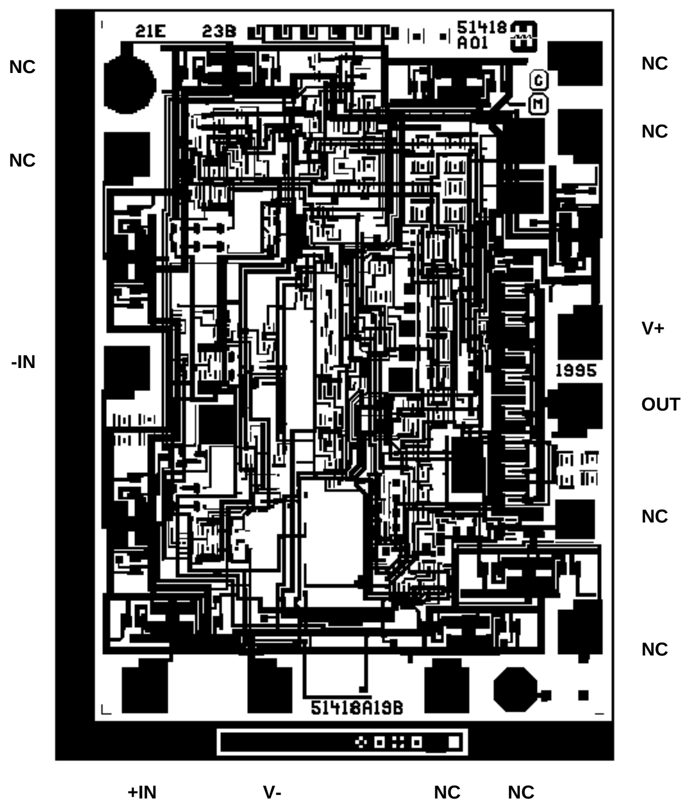
130

SUBSTRATE POTENTIAL (Powered Up):

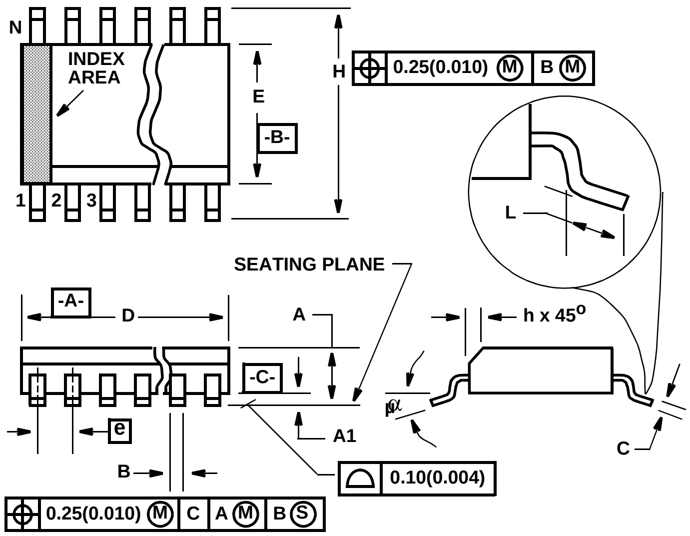
Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1109



Small Outline Plastic Packages (SOIC)



M8.15 **(JEDEC MS-012-AA ISSUE C)**
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.