8M x 32 DDR SDRAM

(Rev 0.7 May/2006)

Features

- Fast clock rate: 300/275/250/200/166 MHz
- Differential Clock CK & CK# input
- 4 Bi-directional DQS. Data transactions on both edges of DQS (1DQS / Byte)
- DLL aligns DQ and DQS transitions
- Edge aligned data & DQS output
- Center aligned data & DQS input
- 4 banks operation
- Programmable mode and extended mode registers
  - CAS# Latency: 3, 4
  - Burst length: 2, 4, 8
  - Burst Type: Sequential & Interleave
- Full page burst length for sequential type only
- Start address of full page burst should be even
- All inputs except DQ's & DM are at the positive edge of the system clock
- No Write-Interrupted by Read function
- 4 individual DM control for write masking only
- Auto Refresh and Self Refresh
- 4096 refresh cycles / 32ms
- Power supplies :

  V_{DD} = 2.5V ± 5%

  V_{DDQ} = 2.5V ± 5%
- Interface : SSTL_2 I/O compatible
- Standard 144-ball FBGA package
- Pb-free package is available

Overview

The EM6AA320 DDR SDRAM is a high-speed CMOS double data rate synchronous DRAM containing 256 Mbits. It is internally configured as a quad 2M x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK).

Data outputs occur at both rising edges of CK and CK#. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of a BankActivate command, which is then followed by a Read or Write command.

The EM6AA320 provides programmable Read or Write burst lengths of 2, 4, 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The refresh functions, either Auto or Self Refresh are easy to use.

In addition, EM6AA320 features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance.

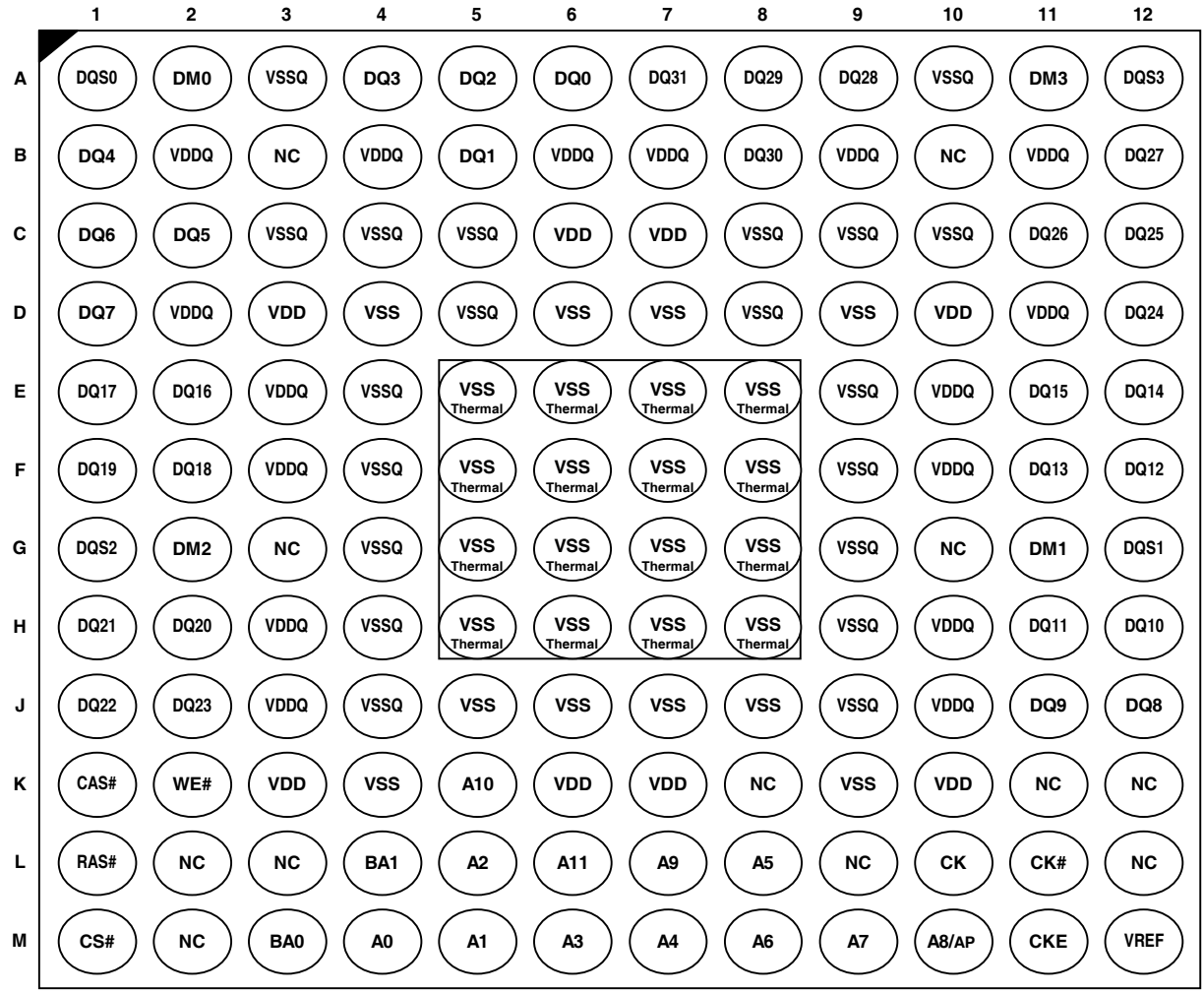
These devices are well suited for applications requiring high memory bandwidth, result in a device particularly well suited to high performance main memory and graphics applications.

Ordering Information

Part Number	Frequency	Power Supply	Package
EM6AA320BI-3.3MS(*)	300MHz	V_{DD} 2.5V V_{DDQ} 2.5V	FBGA
EM6AA320BI-3.6MS(*)	275MHz		FBGA
EM6AA320BI-4MS/4MSG(*)	250MHz		FBGA
EM6AA320BI-5MS/5MSG(*)	200MHz		FBGA
EM6AA320BI-6MS/6MSG(*)	166MHz		FBGA

Note (*) : S indicates stacked die package
G indicates Pb-free package

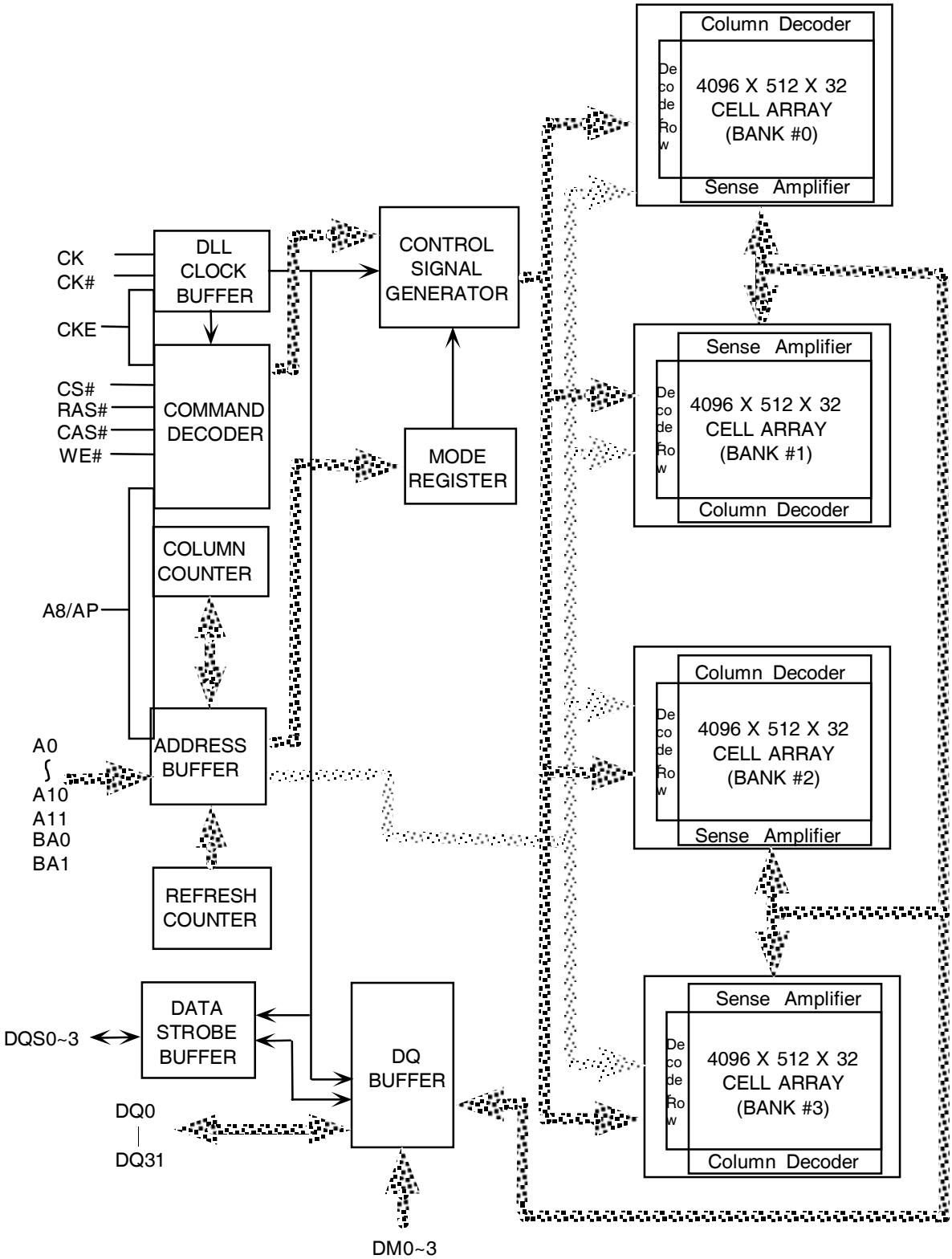
Pin Assignment (FBGA 144Ball Top View)



Pin Assignment by Name (FBGA 144Ball)

Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location
A0	M4	DQ6	C1	DQ24	D12	CK	L10	VDDQ	B6	VSS	E5	VSS	J7	VSSQ	G4
A1	M5	DQ7	D1	DQ25	C12	CK#	L11	VDDQ	B7	VSS	E6	VSS	J8	VSSQ	G9
A2	L5	DQ8	J12	DQ26	C11	CKE	M11	VDDQ	B9	VSS	E7	VSS	K4	VSSQ	H4
A3	M6	DQ9	J11	DQ27	B12	CS#	M1	VDDQ	B11	VSS	E8	VSS	K9	VSSQ	H9
A4	M7	DQ10	H12	DQ28	A9	RAS#	L1	VDDQ	D2	VSS	F5	VSSQ	A3	VSSQ	J4
A5	L8	DQ11	H11	DQ29	A8	CAS#	K1	VDDQ	D11	VSS	F6	VSSQ	A10	VSSQ	J9
A6	M8	DQ12	F12	DQ30	B8	WE#	K2	VDDQ	E3	VSS	F7	VSSQ	C3	NC	B3
A7	M9	DQ13	F11	DQ31	A7	VREF	M12	VDDQ	E10	VSS	F8	VSSQ	C4	NC	B10
A8/AP	M10	DQ14	E12	DQS0	A1	VDD	C6	VDDQ	F3	VSS	G5	VSSQ	C5	NC	G3
A9	L7	DQ15	E11	DQS1	G12	VDD	C7	VDDQ	F10	VSS	G6	VSSQ	C8	NC	G10
A10	K5	DQ16	E2	DQS2	G1	VDD	D3	VDDQ	H3	VSS	G7	VSSQ	C9	NC	K8
A11	L6	DQ17	E1	DQS3	A12	VDD	D10	VDDQ	H10	VSS	G8	VSSQ	C10	NC	K11
DQ0	A6	DQ18	F2	DM0	A2	VDD	K3	VDDQ	J3	VSS	H5	VSSQ	D5	NC	K12
DQ1	B5	DQ19	F1	DM1	G11	VDD	K6	VDDQ	J10	VSS	H6	VSSQ	D8	NC	L2
DQ2	A5	DQ20	H2	DM2	G2	VDD	K7	VSS	D4	VSS	H7	VSSQ	E4	NC	L3
DQ3	A4	DQ21	H1	DM3	A11	VDD	K10	VSS	D6	VSS	H8	VSSQ	E9	NC	L9
DQ4	B1	DQ22	J1	BA0	M3	VDDQ	B2	VSS	D7	VSS	J5	VSSQ	F4	NC	L12
DQ5	C2	DQ23	J2	BA1	L4	VDDQ	B4	VSS	D9	VSS	J6	VSSQ	F9	NC	M2

Block Diagram



Pin Descriptions

Table 1. Pin Details of EM6AA320

Symbol	Type	Description
CK, CK#	Input	**Differential Clock:** CK, CK# are driven by the system clock. All SDRAM input commands are sampled on the positive edge of CK. Both CK and CK# increment the internal burst counter and controls the output registers.
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0, BA1	Input	**Bank Select:** BA0 and BA1 defines to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied. They also define which Mode Register or Extended Mode Register is loaded during a Mode Register Set command.
A0-A11	Input	**Address Inputs:** A0-A11 are sampled during the Bank Activate command (row address A0-A11) and Read/Write command (column address A0-A7, and A9 with A8 defining Auto Precharge) to select one location out of the memory array in the respective bank. During a Precharge command, A8 is sampled to determine if all banks are to be precharged (A8 = HIGH). The address inputs also provide the op-code during a Mode Register Set or Extended Mode Register Set command.
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH" either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BS is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CK. When RAS# is held "HIGH" and CS# is asserted "LOW" the column access is started by asserting CAS# "LOW" Then, the Read or Write command is selected by asserting WE# "HIGH " or "LOW".
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CK. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
DQS0-DQS3	Input / Output	**Bidirectional Data Strobe:** The DQSx signals are mapped to the following data bytes: DQS0 to DQ0-DQ7, DQS1 to DQ8-DQ15, DQS2 to DQ16-DQ23, DQS3 to DQ24-DQ31.
DM0 - DM3	Input	**Data Input Mask:** DM0-DM3 are byte specific. Input data is masked when DM is sampled HIGH during a write cycle. DM3 masks DQ31-DQ24, DM2 masks DQ23-DQ16, DM1 masks DQ15-DQ8, and DM0 masks DQ7-DQ0.
DQ0 - DQ31	Input / Output	**Data I/O:** The DQ0-DQ31 input and output data are synchronized with the positive edges of CK and CK#. The I/Os are byte-maskable during Writes.
V_{DD}	Supply	**Power Supply:** Power for the input buffers and core logic.

V_{SS}	Supply	**Ground:** Ground for the input buffers and core logic.
V_{DDQ}	Supply	**DQ Power:** Provide isolated power to DQs for improved noise immunity.
V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
V_{REF}	Supply	**Reference Voltage for Inputs:** +0.5 x V_{DDQ}
NC	-	**No Connect:** These pins should be left unconnected.

Note: The timing reference point for the differential clocking is the cross point of the CK and CK#. For any applications using the single ended clocking, apply V_{REF} to CK# pin.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CK . Table 2 shows the truth table for the operation commands.

Table 2. Truth Table (Note (1), (2))

Command	State	CKEn-1	CKEn	DM	BA1	BA0	A8	A11-A9, A7-0	CS#	RAS#	CAS#	WE#
BankActivate	Idle(3)	H	X	X	V	V	Row Address		L	L	H	H
BankPrecharge	Any	H	X	X	V	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	V	V	V	L	Column Address A0~A7, A9	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	V	V	V	H		L	H	L	L
Read	Active(3)	H	X	X	V	V	L		L	H	L	H
Read and Autoprecharge	Active(3)	H	X	X	V	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	L	L	OP code		L	L	L	L
Extended Mode Register Set	Idle	H	X	X	L	H			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	X	L	H	H	H
Device Deselect	Any	H	X	X	X	X	X	X	H	X	X	X
Burst Stop	Active(4)	H	X	X	X	X	X	X	L	H	H	L
AutoRefresh	Idle	H	H	X	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	X	H	X	X	X
									L	H	H	H
Power Down Mode Entry	Idle/Active(5)	H	L	X	X	X	X	X	H	X	X	X
									L	H	H	H
Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	X	H	X	X	X
									L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X	X

Note: 1. V = Valid data, X = Don't Care, L = Low level, H = High level
2. CKE_n signal is input level when commands are provided.
CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BA0, BA1signals.
4. Read burst stop with BST command for all burst types.
5. Power Down Mode can not enter in the burst operation.
When this command is asserted in the burst cycle, device state is clock suspend mode.

Mode Register Set (MRS)

The mode register is divided into various fields depending on functionality.

- Burst Length Field (A2, A1, A0)
  This field specifies the data length of column access and selects the Burst Length.
- Addressing Mode Select Field (A3)
  The Addressing Mode can be Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 2, 4 and 8. Full page burst length is only for Sequential mode.
- CAS# Latency Field (A6, A5, A4)
  This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS# Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field.
  $t_{CAC}(min) \leqq$ CAS# Latency X t_{CK}
- Test Mode field :A7; DLL Reset Mode field : A8
  These two bits must be programmed to "00" in normal operation.
- (BA0, BA1)

Mode Resistor Bitmap

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	Mode	RFU must be set to "0"			DLL	TM	CAS Latency			BT	Burst Lenght		

BA0	Register Mode
0	MRS
1	EMRS

A8	A7	Mode
0	0	Normal
1	0	Reset DLL
0	1	Test Mode

A3	Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	1	0	Reserved
0	1	1	3 clocks
1	0	0	4 clocks
All other Reserved			

A2	A1	A0	Burst Length
0	0	1	2
0	1	0	4
0	1	1	8
1	1	1	Full Page (Sequential)
All other Reserved			

Burst Definition, Addressing Sequence of Sequential and Interleave Mode

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
2	X	X	0	0, 1	0, 1
	X	X	1	1, 0	1, 0
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Extended Mode Register Set (EMRS)

The Extended Mode Register Set stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore must be written after power up for proper operation. The extended mode register is written by asserting low on CS#, RAS#, CAS#, and WE#. The state of A0, A2 ~ A5, A7 ~ A11and BA1 is written in the mode register in the same cycle as CS#, RAS#, CAS#, and WE# going low. The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. A1 and A6 are used for setting driver strength to normal, weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. Refer to the table for specific codes.

Extended Mode Resistor Bitmap

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	RFU must be set to “0”					DS1	RFU must be set to “0”				DS0	DLL

BA0	Mode
0	MRS
1	EMRS

A6	A1	Drive Strength	Strength	Comment
0	0	Full	100%	
0	1	SSTL-2 weak	60%	
1	0	RFU	RFU	Do not use
1	1	Matched impedance	30%	Output driver matches impedance

A0	DLL
0	Enable
1	Disable

Power up Sequence

Power up must be performed in the following sequence.

1) Apply power to V_{DD} before or at the same time as V_{DDQ}, V_{TT} and V_{REF} when all input signals are held "NOP" state and maintain CKE “LOW”.
2) Start clock and maintain stable condition for minimum 200us.
3) Issue a “NOP” command and keep CKE “HIGH”
4) Issue a “Precharge All” command.
5) Issue EMRS – enable DLL.
6) Issue MRS – reset DLL. (An additional 200 clock cycles are required to lock the DLL).
7) Precharge all banks of the device.
8) Issue two or more Auto Refresh commands.
9) Issue MRS – with A8 to low to initialize the mode register.

Absolute Maximum Rating

Symbol	Item	Rating		Unit	Note
		Non Pb-free package	Pb-free package		
V_{IN}, V_{OUT}	Input, Output Voltage	- 0.3 ~ V_{DDQ}+0.3		V	
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.3 ~ 3.6		V	
T_A	Ambient Temperature	0~70		°C	
T_{STG}	Storage Temperature	- 55~150		°C	
T_{SOLDER}	Soldering Temperature (10s)	240	260	°C	
P_D	Power Dissipation	2.0		W	
I_{OUT}	Short Circuit Output Current	50		mA	

Recommended D.C. Operating Conditions (SSTL_2 In/Out, T_A = 0 ~ 70 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD}	Power Supply Voltage	2.375	2.5	2.625	V	1
V_{DDQ}	Power Supply Voltage(for I/O)	2.375	2.5	2.625	V	1
V_{REF}	Input Reference Voltage	0.49 x V_{DDQ}	-	0.51 x V_{DDQ}	V	
V_{TT}	Termination Voltage	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	
$V_{IH(DC)}$	Input High Voltage	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	
$V_{IL(DC)}$	Input Low Voltage	Vssq - 0.3	-	V_{REF}- 0.15	V	
V_{OH}	Output High Voltage	V_{tt} + 0.76	-	-	V	I_{OH} = -15.2 mA
V_{OL}	Output Low Voltage	-	-	V_{tt}- 0.76	V	I_{OL} = +15.2 mA
I_{IL}	Input Leakage Current	- 5	-	5	uA	
I_{OL}	Output Leakage Current	- 5	-	5	uA	

Note : 1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.

Capacitance (VDD = 2.5V, f = 1MHz, T_A = 25 °C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0~A11, BA0, BA1)	C_{IN1}	8	10	pF
Input Capacitance (CK, CK#, CKE, CS#, RAS#, CAS#, WE#)	C_{IN2}	6	10	pF
DQ & DQS input/output capacitance	C_{OUT}	6	9	pF
DM0~DM3 input/output capacitance	C_{IN3}	6	9	pF

Note: These parameters are periodically sampled and are not 100% tested.

D.C. Characteristics

(V_{DD} =2.5 ± 5%, T_A = 0~70 °C)

Parameter & Test Condition	Symbol	3.3	3.6	4	5	6	Unit
		Max					
OPERATING CURRENT : One bank; Active-Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0	500	460	350	310	280	mA
OPERATING CURRENT : One bank; Active-Read-Precharge; BL=4; CL=4; tRCDRD=4*tCK; tRC=tRC(min); tCK=tCK(min); Iout=0mA; Address and control inputs changing once per clock cycle	IDD1	600	540	480	440	400	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; tCK=tCK(min); CKE=LOW	IDD2P	120	120	100	80	80	mA
IDLE STANDLY CURRENT : CKE = HIGH; CS#=HIGH(DESELECT); All banks idle; tCK=tCK(min); Address and control inputs changing once per clock cycle; VIN=VREF for DQ, DQS and DM	IDD2N	210	200	175	170	170	mA
ACTIVE POWER-DOWN STANDBY CURRENT : one bank active; power-down mode; CKE=LOW; tCK=tCK(min)	IDD3P	120	120	100	80	80	mA
ACTIVE STANDBY CURRENT : CS#=HIGH;CKE=HIGH; one bank active ; tRC=tRC(max);tCK=tCK(min);Address and control inputs changing once per clock cycle; DQ,DQS,and DM inputs changing twice per clock cycle	IDD3N	300	280	260	240	240	mA
OPERATING CURRENT BURST READ : BL=2; READS; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); Iout=0mA;50% of data changing on every transfer	IDD4R	640	610	580	550	520	mA
OPERATING CURRENT BURST Write : BL=2; WRITES; Continuous Burst ;one bank active; address and control inputs changing once per clock cycle; tCK=tCK(min); DQ,DQS,and DM changing twice per clock cycle; 50% of data changing on every transfer	IDD4W	550	525	500	480	460	mA
AUTO REFRESH CURRENT : tRC=tRFC(min); tCK=tCK(min)	IDD5	750	720	650	610	580	mA
SELF REFRESH CURRENT: Sell Refresh Mode ; CKE<=0.2V;tCK=tCK(min)	IDD6	8	8	5	5	5	mA
BURST OPERATING CURRENT 4 bank operation: Four bank interleaving READs; BL=4;with Auto Precharge; tRC=tRC(min); tCK=tCK(min); Address and control inputschang only during Active, READ , or WRITE command	IDD7	1100	1050	1000	950	900	mA

Note:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage of the device.
2. All voltages are referenced to VSS.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of tCK and tRC. Input signals are changed one time during tCK.
4. Power-up sequence is described in previous page.

Decoupling Capacitance Guide Line

Symbol	Parameter	Value	Unit
C_{DC1}	Decouping Capacitance between V_{DD} and V_{SS}	0.1+0.01	uF
C_{DC2}	Decouping Capacitance between V_{DDQ} and V_{SSQ}	0.1+0.01	uF

AC Input Operating Conditions

(V_{DD} = 2.5 ± 5%, T_A = 0~70 °C)

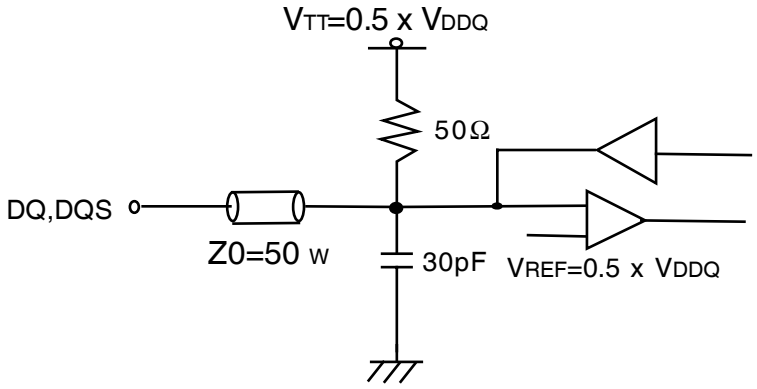
Symbol	Parameter	Min	Max	Unit	Note
V_{IH}	Input High Voltage; DQ	V_{REF}+0.4	-	V	
V_{IL}	Input Low Voltage; DQ	-	V_{REF}-0.4	V	
V_{ID}	Clock Input Differential Voltage; Ck & CK#	0.8	V_{DDQ}+0.6	V	
V_{IX}	Clock Input Crossing Point Voltage; Ck & CK#	0.5xV_{DDQ}-0.2	0.5xV_{DDQ}+0.2	V	

AC Operating Test Conditions

(V_{DD} = 2.5 ± 5%, T_A = 0~70 °C)

Reference Level of Output Signals (V_{RFE})	0.5 x V_{DDQ}
CK & CK# signal maximum peak swing	1.5V
Output Load	See Figure. A Test Load
Input Signal Levels	V_{REF}+0.4 V / V_{REF}-0.4 V
Input Signals Slew Rate	1 V/ns
Input timing measurement reference level	V_{REF}
Output timing measurement reference level	V_{TT}
Reference Level of Input Signals	0.5 x V_{DDQ}

Figure A. Test Load



Electrical Characteristics and Recommended A.C. Operating Conditions

(V_{DD} = 2.5 ± 5%, T_A = 0~70 °C)

Symbol	Parameter		3.3		3.6		4		5		6		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CK}	Clock cycle time	CL = 3	-	-	-	-	4	10	5	10	6	12	ns
		CL = 4	3.3	10	3.6	10	4	10	5	10	-	-	
t_{CH}	Clock high level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{CL}	Clock low level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{DQSCK}	DQS-out access time from CK,CK#		-0.6	0.6	-0.6	0.6	-0.7	0.7	-0.7	0.7	-0.7	0.7	ns
t_{AC}	Output access time from CK,CK#		-0.6	0.6	-0.6	0.6	-0.7	0.7	-0.7	0.7	-0.7	0.7	ns
t_{DQSQ}	DQS-DQ Skew		-	0.35	-	0.4	-	0.4	-	0.45	-	0.45	ns
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
t_{RPST}	Read postamble		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{DQSS}	CK to valid DQS-in		0.85	1.15	0.85	1.15	0.85	1.15	0.85	1.15	0.75	1.25	t_{CK}
t_{WPRES}	DQS-in setup time		0	-	0	-	0	-	0	-	0	-	ns
t_{WPREH}	DQS-in hold time		0.35	-	0.35	-	0.35	-	0.35	-	0.25	-	ns
t_{WPST}	DQS write postamble		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{DQSH}	DQS in high level pulse width		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.35	-	t_{CK}
t_{DQSL}	DQS in low level pulse width		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.35	-	t_{CK}
t_{IS}	Address and Control input setup time		0.9	-	0.9	-	0.9	-	1.0	-	1.0	-	ns
t_{IH}	Address and Control input hold time		0.9	-	0.9	-	0.9	-	1.0	-	1.0	-	ns
t_{DS}	DQ & DM setup time to DQS		0.35	-	0.4	-	0.45	-	0.5	-	0.45	-	ns
t_{DH}	DQ & DM hold time to DQS		0.35	-	0.4	-	0.45	-	0.5	-	0.45	-	ns
t_{HP}	Clock half period		tCLMIN or tCHMIN	-	tCLMIN or tCHMIN	-	tCLMIN or tCHMIN	-	tCLMIN or tCHMIN	-	tCLMIN or tCHMIN	-	ns
t_{QH}	Output DQS valid window		tHP - 0.35	-	tHP - 0.4	-	tHP - 0.45	-	tHP - 0.5	-	THP - 0.55	-	ns
t_{RC}	Row cycle time		17	-	16	-	15	-	12	-	10	-	t_{CK}
t_{RFC}	Refresh row cycle time		19	-	18	-	17	-	14	-	12	-	t_{CK}
t_{RAS}	Row active time		12	100K	11	100K	10	100K	8	100K	7	100K	t_{CK}
t_{RCDRD}	RAS# to CAS# Delay in Read		6	-	5	-	5	-	4	-	3	-	t_{CK}
t_{RCDWR}	RAS# to CAS# Delay in Write		4	-	3	-	3	-	2	-	2	-	t_{CK}
t_{RP}	Row precharge time		5	-	3	-	3	-	4	-	4	-	t_{CK}
t_{RRD}	Row active to Row active delay		3	-	3	-	3	-	2	-	2	-	t_{CK}
t_{WR}	Write recovery time		3	-	3	-	3	-	2	-	2	-	t_{CK}
t_{CDLR}	Last data in to Read command		2	-	2	-	2	-	2	-	2	-	t_{CK}
t_{CCD}	Col. Address to Col. Address delay		1	-	1	-	1	-	1	-	1	-	t_{CK}
t_{MRD}	Mode register set cycle time		1	-	1	-	2	-	2	-	2	-	t_{CK}
t_{DAL}	Auto precharge write recovery + Precharge		9	-	9	-	8	-	6	-	6	-	t_{CK}
t_{XSA}	Self refresh exit to read command delay		200	-	200	-	200	-	200	-	200	-	t_{CK}
t_{PDEX}	Power down exit time		tIS + 2tCK	-	tIS + 2tCK	-	tIS + 2tCK	-	tIS + 2tCK	-	tIS + 2tCK	-	ns
t_{REF}	Refresh interval time		-	7.8		7.8	-	7.8		7.8		7.8	us

Timing Waveforms

Figure 1. AC Parameters for Read Timimg (Burst Length = 4)

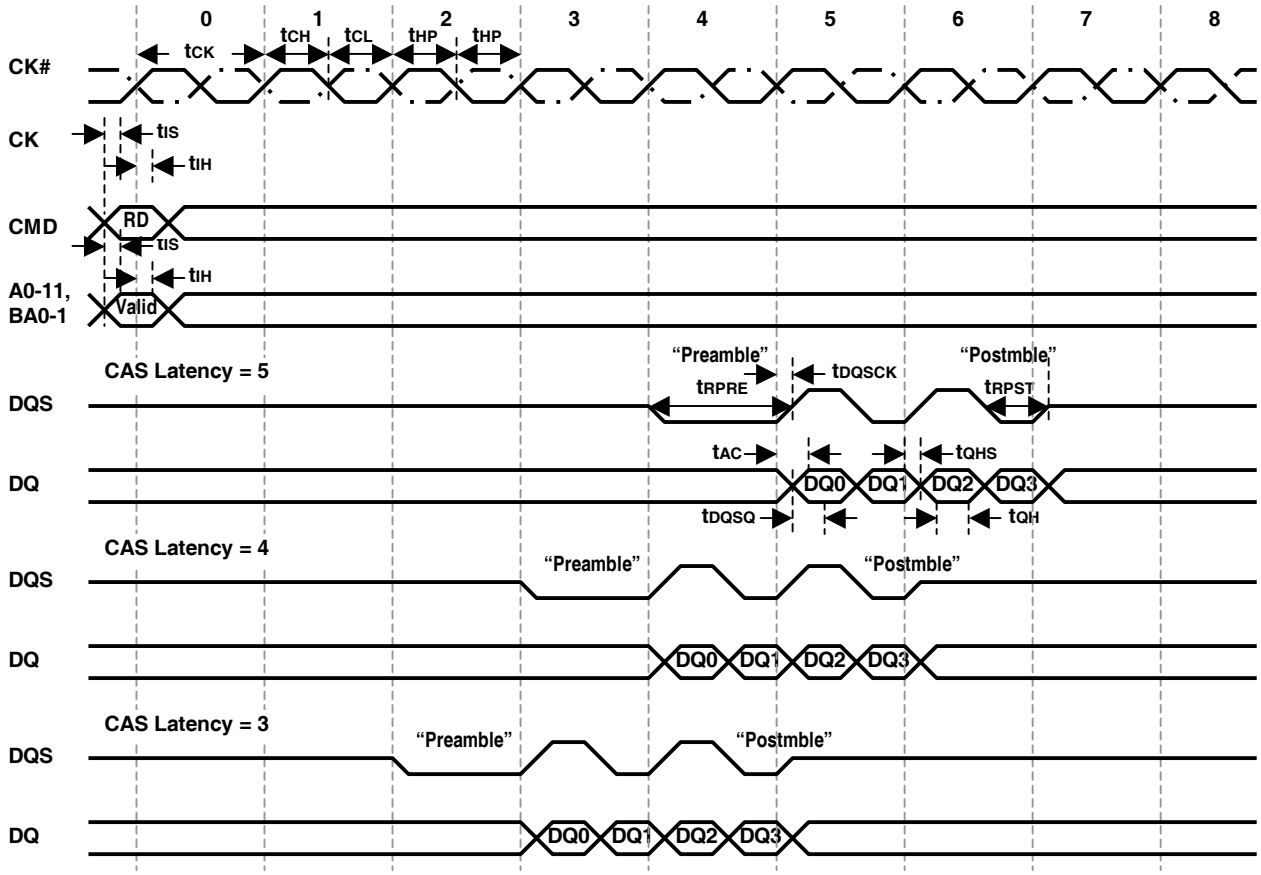


Figure 2. AC Parameters for Write Timing (Burst Length=4)

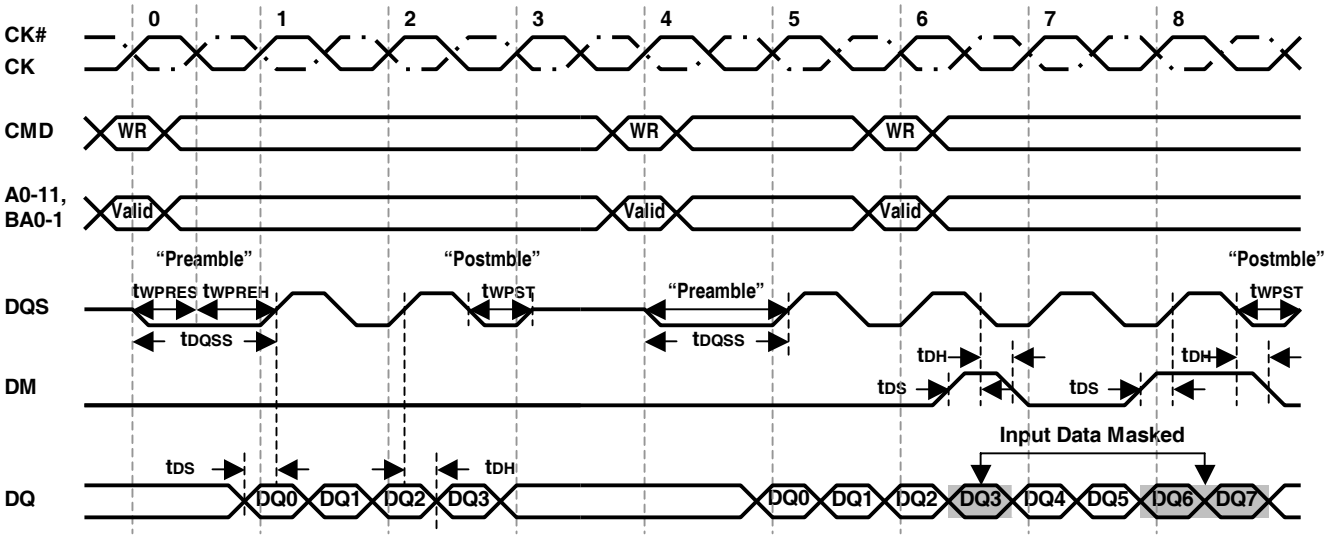


Figure 3. Bank Activate Read or Write Command Timing

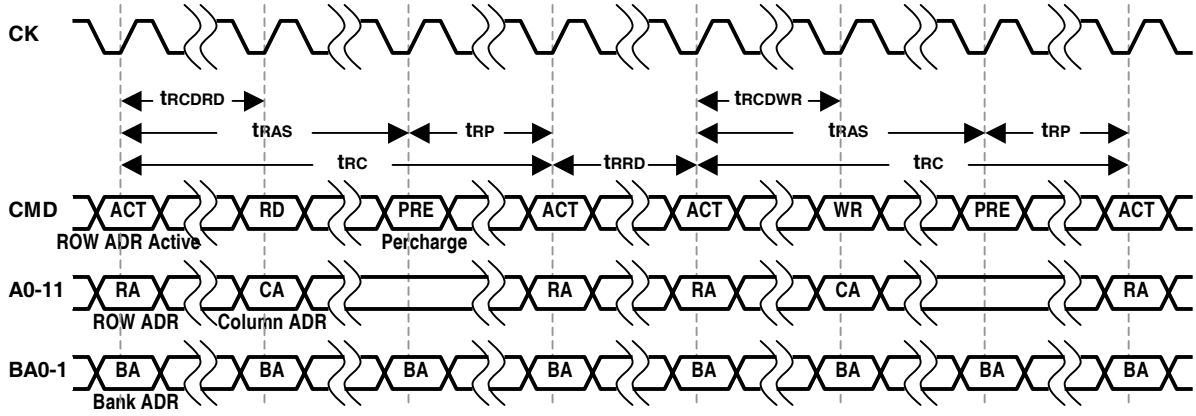


Figure 4. Burst Stop for Read (CAS Letancy = 5, Burst Length = 4)

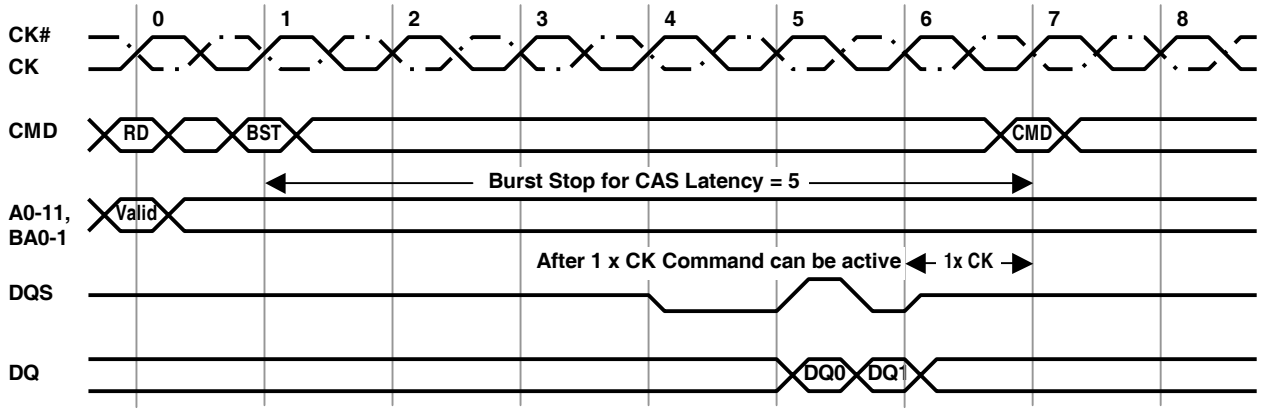


Figure 5. Read with Auto Precharge (CAS Letancy = 5, Burst Length = 4)

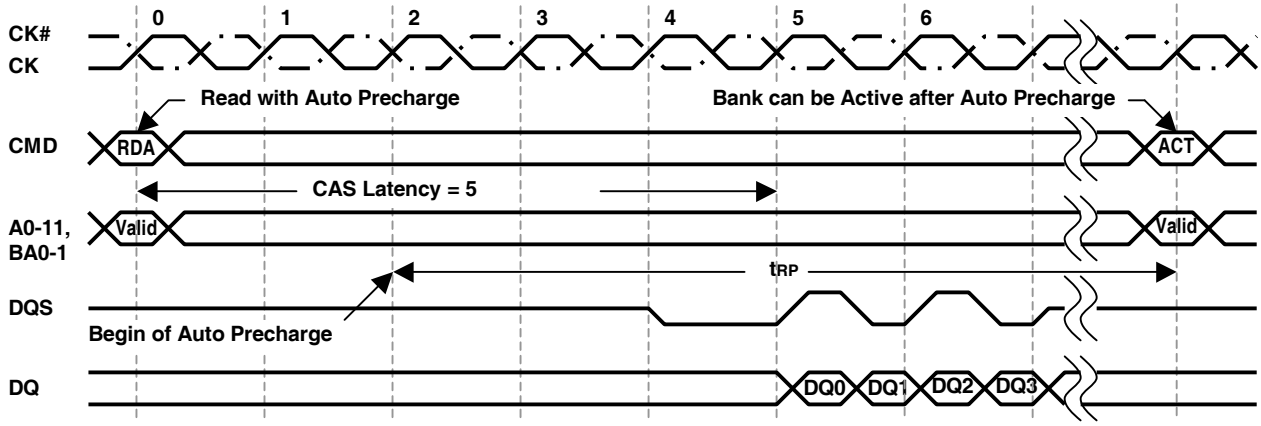


Figure 6. Write with Auto Precharge (Burst Length = 4)

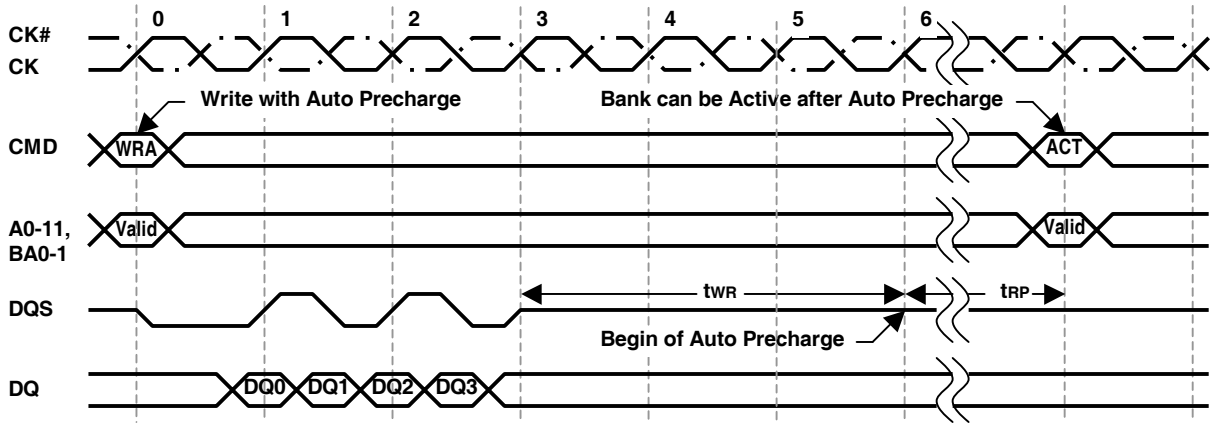


Figure 7. Read Burst Interrupt by Read (CAS Letancy = 5, Burst Length = 4)

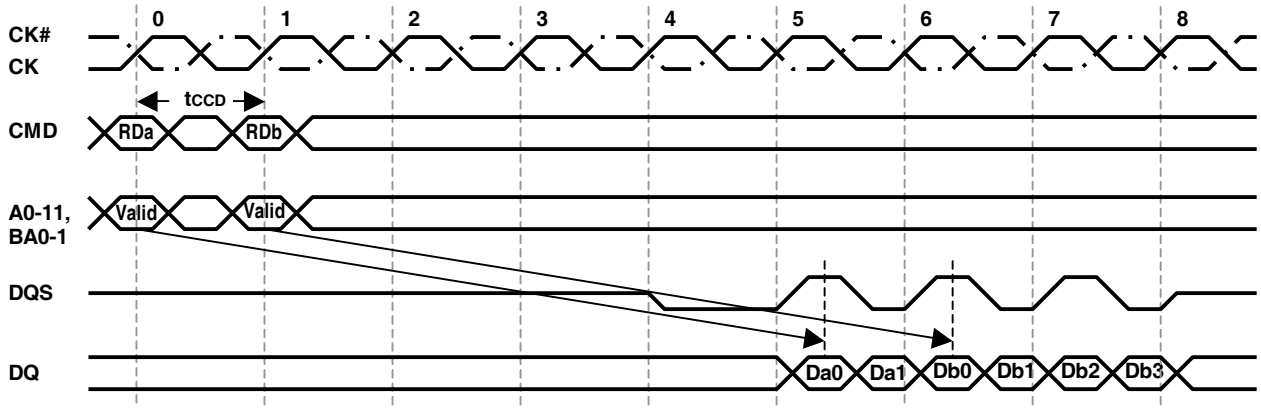


Figure 8. Write Interrupted by Write (Burst Length = 4)

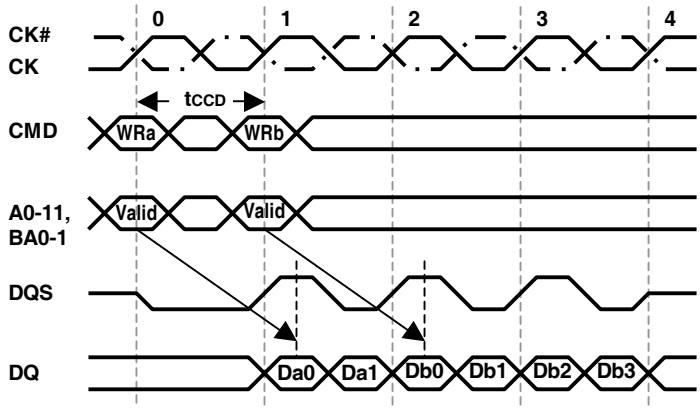


Figure 9. Auto Refresh Timimg

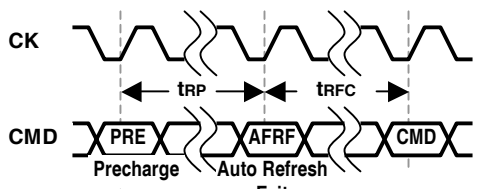


Figure 10. Self Refresh Timimg

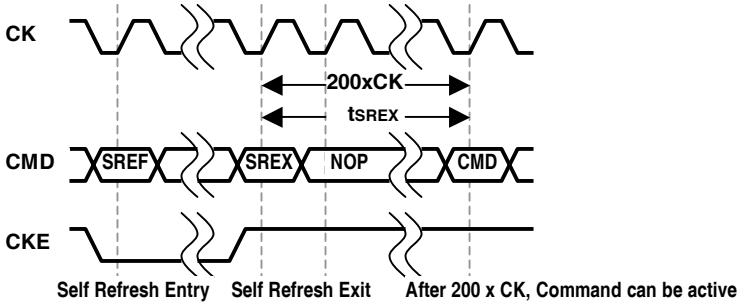


Figure 11. Precharge Command

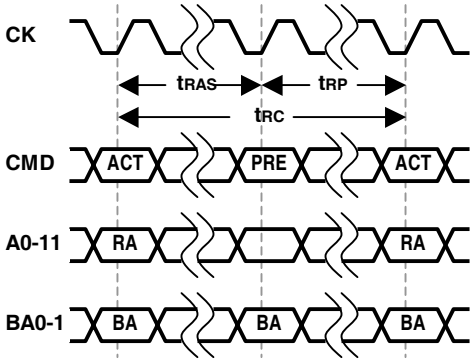


Figure 12. Power Up Sequence

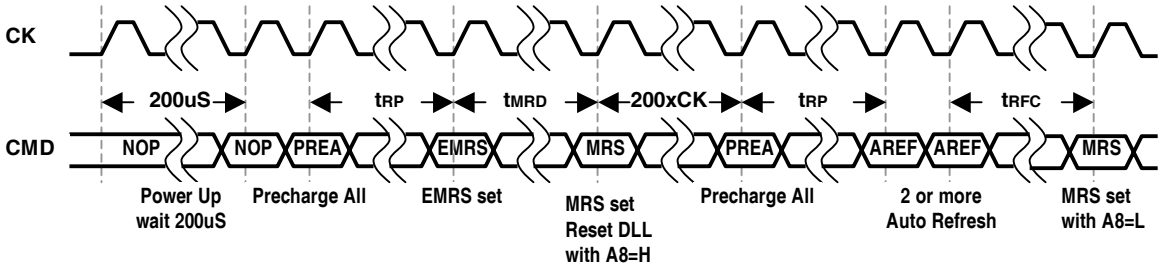


Figure 13. Mode Register Set Timing

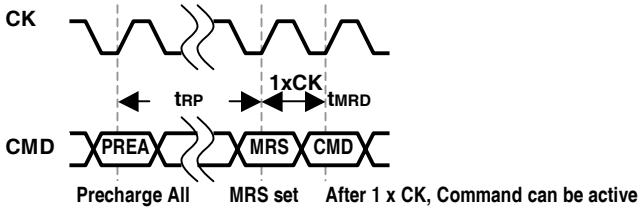
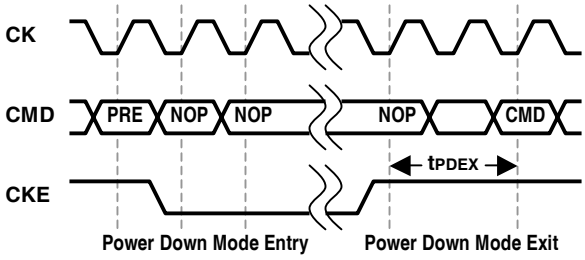
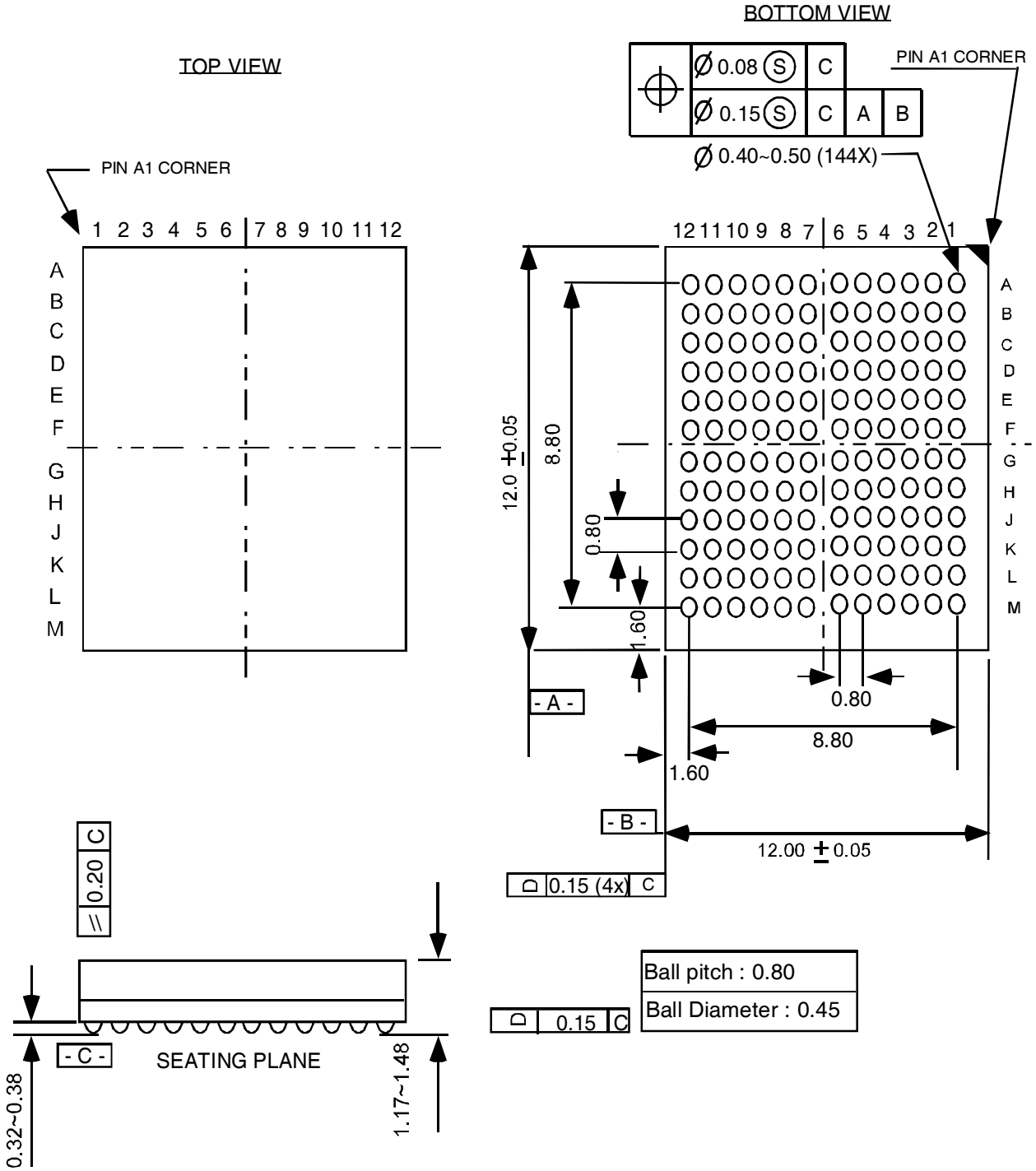


Figure 14. Power Down Mode




TOP VIEW
PIN A1 CORNER
1 2 3 4 5 6 7 8 9 10 11 12
A B C D E F G H J K L M
BOTTOM VIEW
PIN A1 CORNER
Ø 0.08 S C
Ø 0.15 S C A B
Ø 0.40~0.50 (144X)
12 11 10 9 8 7 6 5 4 3 2 1
12.0 ±0.05
8.80
0.80
1.60
0.80
8.80
1.60
12.00 ±0.05
- A -
- B -
0.15 (4x) C
0.20 C
- C -
SEATING PLANE
0.32~0.38
1.17~1.48
0.15 C
Ball pitch : 0.80
Ball Diameter : 0.45