eZ80F915050MOD

eZ80F91 Module

Product Specification

PS019310-0904

PRELIMINARY

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Document Disclaimer

Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Document

Date	Revision Level	Section	Description	Page #
July 2004	10	Formatted to current publication standards		All
		Ethernet PHY and RJ45 Connector section	Part number change to AMD MII.	12
		Bill of Materials for the eZ80F91 Module	Part number change to internal crystal at jumper location Y3.	22

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The eZ80F91 Module

The eZ80F91 Module is a compact, high-performance Ethernet module specially designed for the rapid development and deployment of embedded systems requiring control and Internet/Intranet connectivity.

This expandable module is powered by ZiLOG's latest power-efficient, high-speed, optimized pipeline architecture eZ80F91 microcontroller, a member of ZILOG's family of eZ80Acclaim! Flash Microcontrollers.

The eZ80F91 is a high-speed single-cycle instruction-fetch microcontroller, which can operate with a clock speed of 50MHz. It can operate in Z80-compatible addressing mode (64KB) or full 24-bit addressing mode (16MB).

The rich peripheral set of the eZ80F91 Module makes it suitable for a variety of applications, including industrial control, IrDA connectivity, communication, security, automation, point-of-sale terminals, and embedded networking applications.

Module Features

- Factory-default operating clock frequency at 50MHz
- 10/100 Base-T Ethernet PHY with RJ45 connector
- 512KB fast SRAM
- 256KB on-chip Flash memory
- 1MB off-chip NOR Flash memory
- Battery-backed Real-Time Clock
- I/O connector provides 32 general-purpose 5V-tolerant I/O pinouts
- ZiLOG's industry-leading IrDA transceiver—ZiLOG ZHX1810
- Onboard connector provides I/O bus for external peripheral connections (IRQ, CS, 24 address, 8 data)
- Low-cost connection to carrier board via two 2x30pin headers
- Small footprint 63.5mm x 78.7mm
- 3.3V power supply
- Standard operating temperature range: 0ºC to +70ºC

eZ80F91 Controller Features

- The eZ80F91 device contains 256KB of Flash memory and 8KB of SRAM
- Single-cycle instruction fetch, high-performance, pipelined eZ80® CPU core
- 10/100 Mbps Ethernet MAC with 8KB frame buffer
- Low power features including SLEEP mode, HALT mode, and selective peripheral power-down control
- Two UARTs with independent baud rate generators and support for 9-bit operation
- SPI with independent clock generator
- I^2C with independent clock generator
- Infrared Data Association (IrDA)-compliant infrared encoder/decoder
- New DMA-like eZ80® instructions for efficient block data transfer
- External interface with 4 chip selects, individual wait state generators, and an external WAIT input pin — supports Intel- and Motorola-style buses
- Flexible-priority vectored interrupts (both internal and external) and interrupt controller
- Real-time clock with on-chip 32KHz oscillator, selectable 50/60Hz input, and separate V_{DD} pin for battery backup
- Four 16-bit Counter/Timers with prescalers and direct input/output drive
- Watch-Dog Timer
- 32 bits of general-purpose I/O
- JTAG and ZDI debug interfaces
- 144-pin LQFP package
- 3.0–3.6V supply voltage with 5V tolerant inputs
- Standard operating temperature range: 0ºC to +70ºC

Block Diagram

Figure 1 provides a block diagram of the eZ80F91 Module.

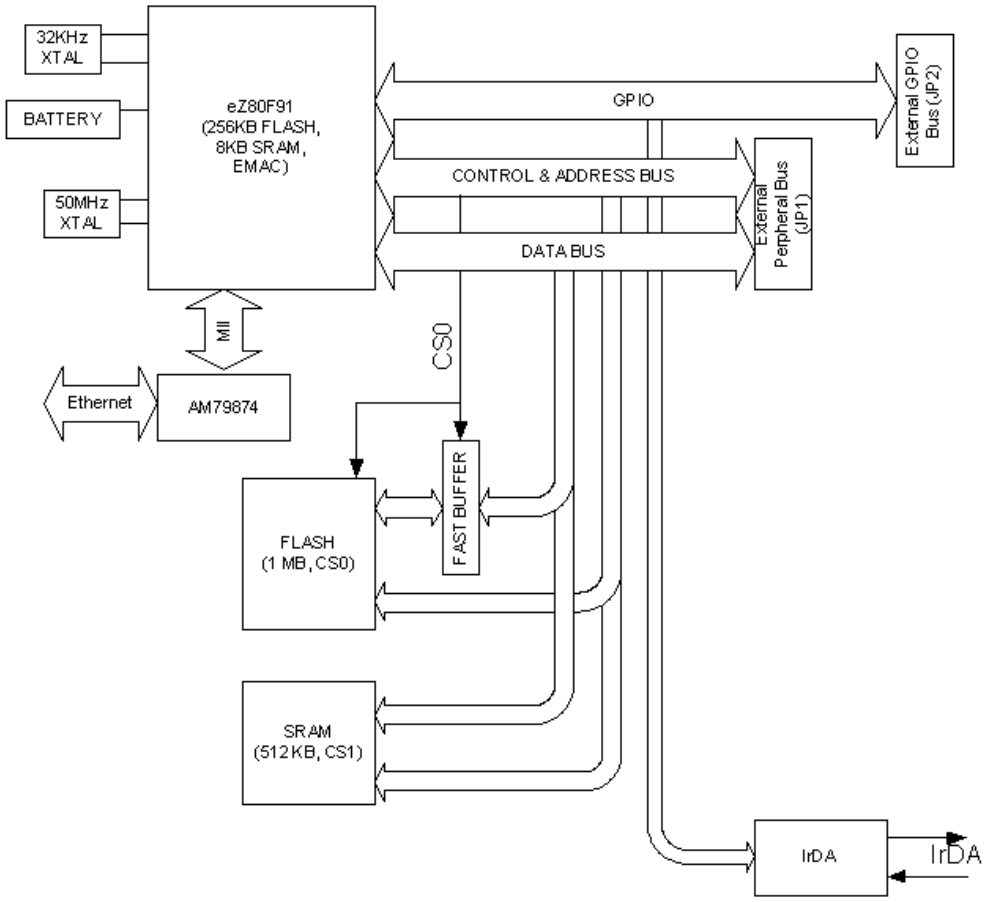

Figure 1. eZ80F91 Module Functional Block Diagram

Pin Description

Peripheral Bus Connector

Figure 2 illustrates the pin layout of the 60-pin Peripheral Bus Connector (JP1) of the eZ80F91 Module. The eZ80® Development Platform, however, features a 50-pin connector. The eZ80F91 Module is designed to interface pin 60 of its JP1 connector to pin 50 of the eZ80® Development Platform's JP1 connector so that pins 1–10 of the eZ80F91 Module overlap the edge of the eZ80® Development Platform. Table 2 identifies the pins and their functions.

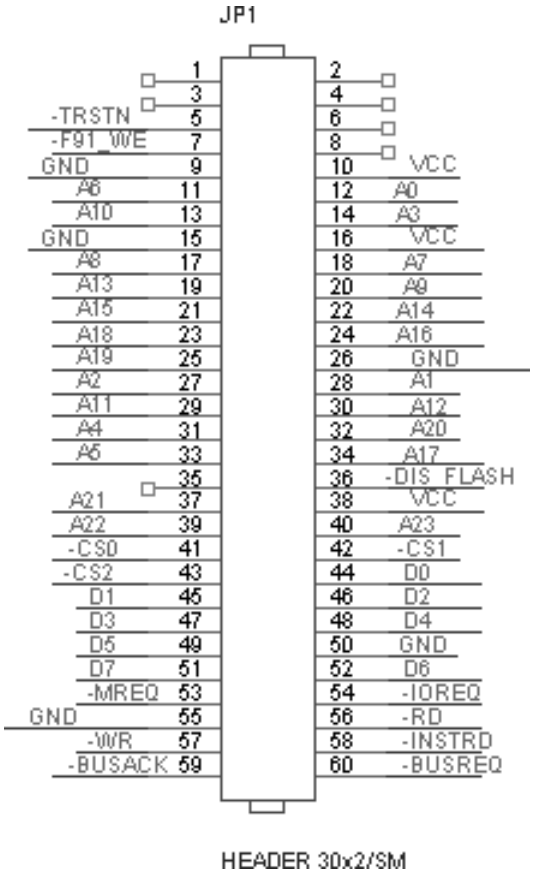

Figure 2. eZ80F91 Module
Peripheral Bus Connector Pin Configuration—JP1

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and B/W, for which BYTE is active Low.

Table 2. eZ80F91 Module Peripheral Bus Connector Pin Identification*

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
1	Reserved			
2	Reserved			
3	Reserved			
4	Reserved			
5	$\overline{TRSTN}$		Input	Reset for On-Chip Instrumentation (OCI).
6	Reserved			
7	$\overline{F91\_WE}$	PU 10KΩ	Input	A Low enables a Write to on-chip Flash memory. If this pin is unconnected, on-chip Flash memory is write-protected.
8	Reserved			
9	GND			V_{SS}/Ground (0V).
10	V_{CC}			3.3V supply input pin.
11	A6		Bidirectional	
12	A0		Bidirectional	
13	A10		Bidirectional	
14	A3		Bidirectional	
15	GND			V_{SS}/Ground (0V).
16	V_{CC}			3.3V supply input pin.
17	A8		Bidirectional	
18	A7		Bidirectional	
19	A13		Bidirectional	
20	A9		Bidirectional	
21	A15		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80F91 Module Peripheral Bus Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
22	A14		Bidirectional	
23	A18		Bidirectional	
24	A16		Bidirectional	
25	A19		Bidirectional	
26	GND			V_{SS}/Ground (0V).
27	A2		Bidirectional	
28	A1		Bidirectional	
29	A11		Bidirectional	
30	A12		Bidirectional	
31	A4		Bidirectional	
32	A20		Bidirectional	
33	A5		Bidirectional	
34	A17		Bidirectional	
35	Reserved			
36	$\overline{\text{DIS\_Flash}}$	PU 10KΩ	Input	A Low disables onboard Flash memory. Flash is enabled if DIS_Flash is not connected; CMOS Input 3.3V (5V tolerant).
37	A21		Bidirectional	
38	V_{CC}			3.3V supply input pin.
39	A22		Bidirectional	
40	A23		Bidirectional	
41	$\overline{\text{CS0}}$		Output	
42	$\overline{\text{CS1}}$		Output	
43	$\overline{\text{CS2}}$		Output	
44	D0	PU 4kΩ	Bidirectional	
45	D1	PU 4kΩ	Bidirectional	

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80F91 Module Peripheral Bus Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
46	D2	PU 4kΩ	Bidirectional	
47	D3	PU 4kΩ	Bidirectional	
48	D4	PU 4kΩ	Bidirectional	
49	D5	PU 4kΩ	Bidirectional	
50	GND			V_{SS}/Ground (0V).
51	D7	PU 4kΩ	Bidirectional	
52	D6		Bidirectional	
53	$\overline{\text{MREQ}}$		Bidirectional	
54	$\overline{\text{IORQ}}$		Bidirectional	
55	GND			V_{SS}/Ground (0V).
56	$\overline{\text{RD}}$		Bidirectional	
57	$\overline{\text{WR}}$		Bidirectional	
58	$\overline{\text{INSTRD}}$		Output	
59	$\overline{\text{BUSACK}}$		Output	
60	$\overline{\text{BUSREQ}}$	PU 2kΩ	Input	

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

I/O Connector

Figure 3 illustrates the pin layout of the 60-pin I/O Connector (JP2) of the eZ80F91 Module. The eZ80® Development Platform, however, features a 50-pin connector. The eZ80F91 Module is designed to interface pin 60 of its JP2 connector to pin 50 of the eZ80® Development Platform's JP2 connector so that pins 1–10 of the eZ80F91 Module overlap the edge of the eZ80® Development Platform. Table 3 identifies the pins and their functions.

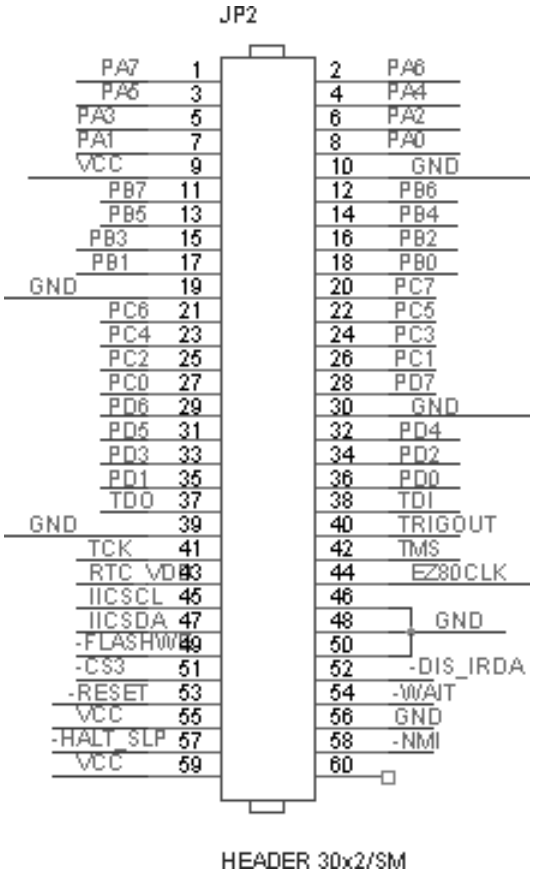

Figure 3. eZ80F91 Module
I/O Connector Pin Configuration—JP2

Table 3. eZ80F91 Module I/O Connector Pin Identification*

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
1	PA7		Bidirectional	
2	PA6		Bidirectional	
3	PA5		Bidirectional	
4	PA4		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 3. eZ80F91 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
5	PA3		Bidirectional	
6	PA2		Bidirectional	
7	PA1		Bidirectional	
8	PA0		Bidirectional	
9	V_{CC}			3.3V supply input pin.
10	GND			V_{SS}/Ground (0V).
11	PB7		Bidirectional	
12	PB6		Bidirectional	
13	PB5		Bidirectional	
14	PB4		Bidirectional	
15	PB3		Bidirectional	
16	PB2		Bidirectional	
17	PB1		Bidirectional	
18	PB0		Bidirectional	
19	GND			V_{SS}/Ground (0V).
20	PC7		Bidirectional	
21	PC6		Bidirectional	
22	PC5		Bidirectional	
23	PC4		Bidirectional	
24	PC3		Bidirectional	
25	PC2		Bidirectional	
26	PC1		Bidirectional	
27	PC0		Bidirectional	
28	PD7		Bidirectional	
29	PD6		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 3. eZ80F91 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
30	GND			V_{SS}/Ground (0V).
31	PD5		Bidirectional	
32	PD4	PD 4kΩ	Bidirectional	
33	PD3		Bidirectional	
34	PD2		Bidirectional	
35	PD1		Bidirectional	
36	PD0		Bidirectional	
37	TDO		Output	JTAG Data Output pin.
38	TDI/ZDA		Input	JTAG Data Input pin.
39	GND			V_{SS}/Ground (0V).
40	TRIGOUT		Output	Active High trigger event indicator.
41	TCK/ZCL	PU 10KΩ	Input	JTAG Input. High on reset enables ZDI mode; Low on reset enables OCI debug.
42	TMS	PU 10KΩ	Input	JTAG Test Mode Select Input.
43	RTC_V_{DD}			RTC supply. For proper operation of the eZ80F91 Module, this pin must be connected to the same power source that powers the module (as is done on the ZiLOG development platform).
44	EZ80CLK		Output	Synchronous CPU clock output.
45	I^2CSCL	PU 4kΩ	Bidirectional	I^2C Bus Clock.
46	GND			V_{SS}/Ground (0V).
47	I^2CSDA	PU 4kΩ	Bidirectional	I^2C Data Clock.
48	GND		Power	V_{SS}/Ground (0V).
49	$\overline{\text{FlashWE}}$	PU 10KΩ	Input	A Low enables a Write to external Flash memory boot block area. If this pin is unconnected, the Flash memory boot block area is write-protected.
50	GND			V_{SS}/Ground (0V).

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 3. eZ80F91 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
51	$\overline{CS3}$		Output	Used on the eZ80190, eZ80L92, eZ80F92, eZ80F93 devices and connected to the CS8900 EMAC.
52	$\overline{DIS\_IRDA}$	PU 10KΩ	Input	A Low disables the onboard IRDA transceiver to use PC0/PC1 UART pins externally.
53	$\overline{RESET}$	PU 2kΩ	Bidirectional	Reset Output from module or push-button reset.
54	$\overline{WAIT}$	PU 2kΩ	Input	Driving the $\overline{WAIT}$ pin Low forces the CPU to provide additional clock cycles for an external peripheral or external memory to complete its Read or Write operation.
55	V_{CC}			3.3V supply input pin.
56	GND			V_{SS}/Ground (0V).
57	$\overline{HALT\_SLP}$		Output, Active Low	A Low on this pin indicates that the CPU enters either HALT or SLEEP mode because of execution of either a HALT or SLP instruction.
58	$\overline{NMI}$	PU 10KΩ	Schmitt Trigger Input, Active Low	The $\overline{NMI}$ input is a higher priority input than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt trigger to allow RC rise times. This external NMI signal is combined with an internal NMI signal generated from the WDT block before being connected to the NMI input of the CPU.
59	V_{CC}			3.3V supply input pin.
60	Reserved		NC	Reserved—No Connection.

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Onboard Component Description

Logic-Level I/Os

The I/O connector features 32 general-purpose 3.3V CMOS I/O pins that can be used as outputs or inputs interfacing to external logic. All I/Os are 5V tolerant. Some of the General-Purpose I/O pins support dual mode functions (SPI, Timer I/O, UARTs and bit I/O with edge- or level-triggered interrupt functions on each pin). For more information on eZ80F91 dual modes, please refer to the eZ80F91 Product Specification (PS0192).

Onboard Battery Backup

An onboard Panasonic VL-1220-1VC 3V Lithium battery powers the 32kHz Real-Time Clock when external power is removed. The battery is charged through diode CR1 and resistor R28 when external power is applied to the board.

Ethernet PHY and RJ45 Connector

The eZ80F91 Ethernet Module contains Advanced Micro Devices' Am79C874 Media-Independent Interface (MII) and a HALO RJ45 with integrated magnetics (transformer and common-mode chokes) and two LED indicators.

The MII enables different modes of Ethernet communication, configurable by resistors R19, R21, R23, and R24. The eZ80F91 Ethernet Module is shipped with all four resistors installed. Table 4, which lists the available resistor settings, is excerpted from the Am79C874 data sheet published by AMD.

Table 4. eZ80F91 Ethernet Module MII Resistor Configuration

R24 ANEG	R19 (Tech[2])	R23 (Tech[1])	R21 (Tech[0])	Speed	Full-Duplex	ANEG-EN	Capabilities	ANEG
IN	IN	IN	IN	Yes[1]	Yes[1]	No	All	Disabled
IN	IN	IN	OUT	No	No	No	10HD	Disabled
IN	IN	OUT	IN	No	No	No	100HD	Disabled

Notes:
1. MII Register 0 (Speed and Duplex Bits) must be set by a MAC to achieve a link.
2. When autonegotiation is enabled, these bits can be written but will be ignored by PHY.
3. The advertised abilities of MII Register 4 cannot exceed the abilities of MII Register 1. Autonegotiation should always be enabled.

Table 4. eZ80F91 Ethernet Module MII Resistor Configuration (Continued)

R24 ANEG	R19 (Tech[2])	R23 (Tech[1])	R21 (Tech[0])	Speed	Full-Duplex	ANEG-EN	Capabilities	ANEG
IN	IN	OUT	OUT	No	No	No	100HD	Disabled
IN	OUT	IN	IN	Yes[1]	Yes[1]	No	All	Disabled
IN	OUT	IN	OUT	No	No	No	10FD	Disabled
IN	OUT	OUT	IN	No	No	No	100FD	Disabled
IN	OUT	OUT	OUT	No	No	No	100FD	Disabled
OUT	IN	IN	IN	Yes[2]	Yes[2]	Yes[3]	None	Enabled
OUT	IN	IN	OUT	Yes[2]	Yes[2]	Yes[3]	10HD	Enabled
OUT	IN	OUT	IN	Yes[2]	Yes[2]	Yes[3]	100HD	Enabled
OUT	IN	OUT	OUT	Yes[2]	Yes[2]	Yes[3]	100HD, 10HD	Enabled
OUT	OUT	IN	IN	Yes[2]	Yes[2]	Yes[3]	None	Enabled
OUT	OUT	IN	OUT	Yes[2]	Yes[2]	Yes[3]	10FD/HD	Enabled
OUT	OUT	OUT	IN	Yes[2]	Yes[2]	Yes[3]	100FD/HD	Enabled
OUT	OUT	OUT	OUT	Yes[3]	Yes[2]	Yes[3]	All	Enabled

Notes:
1. MII Register 0 (Speed and Duplex Bits) must be set by a MAC to achieve a link.
2. When autonegotiation is enabled, these bits can be written but will be ignored by PHY.
3. The advertised abilities of MII Register 4 cannot exceed the abilities of MII Register 1. Autonegotiation should always be enabled.

Ethernet LEDs

The Ethernet connection is provided by the HALO RJ45 connector. It contains two green LEDs that are located next to each other on the eZ80F91 Module. When PHY is receiving data, the left LED is on. When the PHY is transmitting data, the right LED is on.

Fast Buffer (U10)

The eZ80F91 Module's fast buffer (see Figure 1 on page 3) exists to prevent bus contention that will occur because of slow turn-off time of the module's external Flash and the fast bus turn-around time of the eZ80F91 (generic feature of the eZ80® family when it is used in native mode).

Below is a short explanation of the problem related to bus contention when using eZ80 family of the microprocessors in native eZ80® mode. Refer to Figure 4 on

page 15 while reading the following discussion. Also see the eZ80F91 Product Specification (PS0192) for further details.

Bus contention occurs when two or more devices drive a common bus. The eZ80F91's CS0 drives the Flash CE. After the access to Flash, CS0 is driven High a maximum of 8.8ns after the next rising edge of the Clock (T6, Figure 4). The Flash turn-off time (T_{OD}) is 25ns, which is the time from OE or CE going High to the Flash output drivers going into High-Z mode. In other words, after the end of the eZ80F91 Read access to Flash, it takes 8.8ns+25ns = 33.8ns before Flash stops driving the data bus. At this point, the eZ80F91 device is already well into the next bus cycle.

Assume that the next cycle is Memory Write. During the Memory Write cycle, Data (output) from the eZ80F91 device is valid not later than T3 = 7.5ns, and the Write pulse is asserted not later than 4.5ns after the falling edge of the Clock (14.5ns from the Rising edge if Clock is 50MHz). It means that during T_{CON} = (33.8ns – 7.5ns) = 26.3ns; two devices drive the common Data Bus—the eZ80F91 device and Flash. In turn, data that is being written during the Write operation might be corrupted. The part used to isolate a slow Flash data bus from a fast eZ80F91 bus has 5.5ns turn-off time, which reduces 25ns part of the T_{CON} to 5.5ns. As a result, bus contention still occurs, but its duration is not 26.3ns, as the following equation shows:

Time of contention = (8.8ns - 7.5ns + 5.5ns) = 6.8ns

Data being written is not corrupted because the Write pulse is not yet asserted.

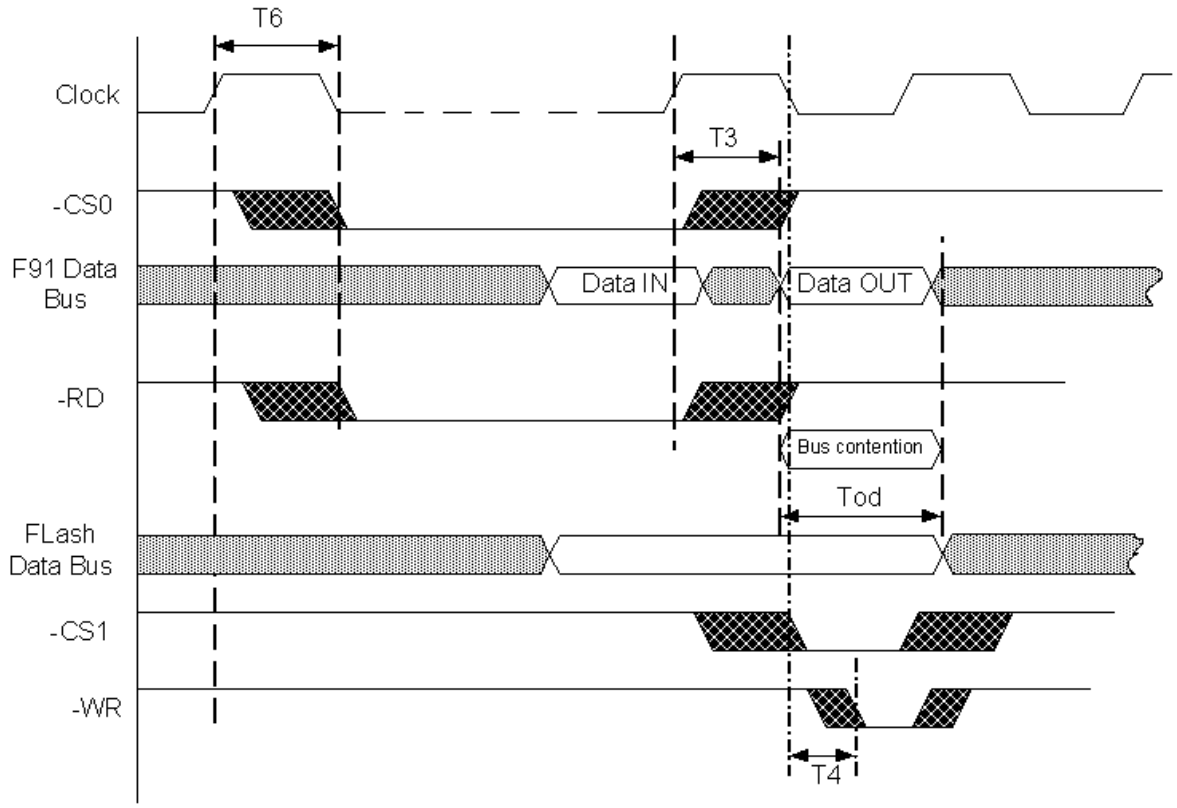

Figure 4. Bus Contention Without the eZ80F91 Module Fast Buffer Feature

Memory

The eZ80F91 Module contains external Flash memory, and the eZ80F91 MCU contains internal Flash memory. To allow Read/Write access to Flash memory on the eZ80F91 Module, there are two signals provided, on connectors JP1 and JP2. A jumper JP3 on the module enables programming of on-chip Flash.

There is also a signal that duplicates the function of this jumper. Table 5 describes the states of the signals and the status of the jumper for different modes.

Table 5. Flash Memory Programming Signals and Jumpers

Signal/Jumper	Function	State/Status
$\overline{\text{DIS\_FLASH}}$	Controls Read/Write access to eZ80F91 Module external Flash memory	When Low, access is enabled
$\overline{\text{FlashWE}}$	Controls Write operations to the boot block of eZ80F91 Module external Flash memory	When Low, Write is enabled
$\overline{\text{JP3}}$	Controls Write access to eZ80F91 MCU on-chip Flash memory	When IN, Write is enabled
$\overline{\text{F91\_WE}}$	Controls Write access to eZ80F91 MCU on-chip Flash memory	When Low, Write is enabled

The eZ80F91 Module's external Flash memory has an access time of 100ns. At least five wait states must be added to the cycle when accessing external Flash at the 50MHz clock speed. eZ80F91 MCU on-chip Flash is faster; its minimum access time is 60ns, which requires only three wait states at 50MHz.

There is 512KB of fast SRAM on the eZ80F91 Module. Access time is 12ns, which requires one wait-state access. The eZ80F91 on-chip SRAM can be used with zero wait states.

IrDA Transceiver

An onboard IrDA transceiver (ZiLOG ZHX1810) is connected to PD0 (TX), PD1 (RX), and PD2 (Shutdown, R_SD). The IrDA transceiver is of the LED type 870nm Class 1.

The receiver supply current is 90–150µA and the transmitter supply current is 260mA when the LED is active.The IrDA transceiver is accessible via the IrDA controller attached to UART0 on the eZ80F91 device. The UART0 console and the IrDA transceiver cannot be used simultaneously.

To use the UART0 for console or to save power, the transceiver can be disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IR_SD) High or by pulling the DIS_IRDA pin on the I/O connector Low. The shutdown is used for power savings. To enable the IrDA transceiver, DIS_IRDA is left floating and PD2 is set to Low.

Reset Generator

The onboard Reset Generator Chip performs reliable Power-On Reset. The chip generates a reset pulse with a duration of 200ms if the power supply drops below

2.93V. This reset pulse ensures that the board always starts in a defined condition. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80F91 Module with a low-impedance output (e.g. a 100-Ohm pushbutton).

Serial Interface Ports

The CPU contains two UARTs with programmable baud rate generators. UART0 is connected to GPIO PD[0:7] on the I/O connector. UART1 is connected to GPIO PC[0:7] on the I/O connector.

Note: Do not connect an RS-232 interface without level shifters. There are no RS232-level shifters on the eZ80F91 Module.

Physical Dimensions

The footprint of the eZ80F91 Module PCB is 63.5mm x 78.7cm. With an RJ-45 Ethernet connector, the overall height is 25mm. See Figure 5.

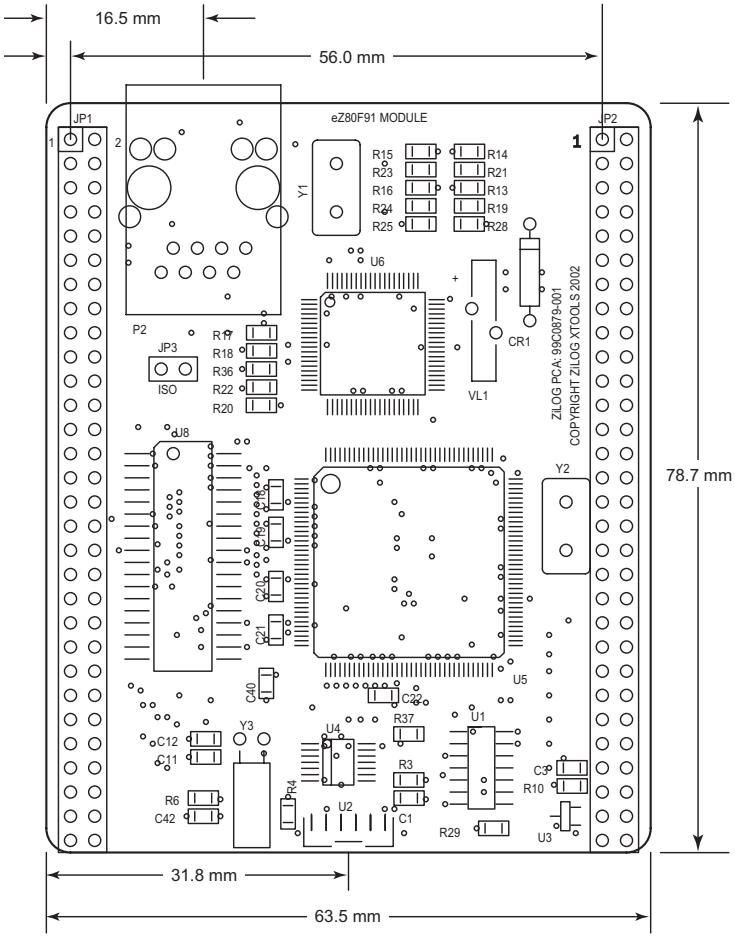

Figure 5. Physical Dimensions of the eZ80F91 Module

Figure 6 illustrates the top layer silkscreen of the eZ80F91 Module.

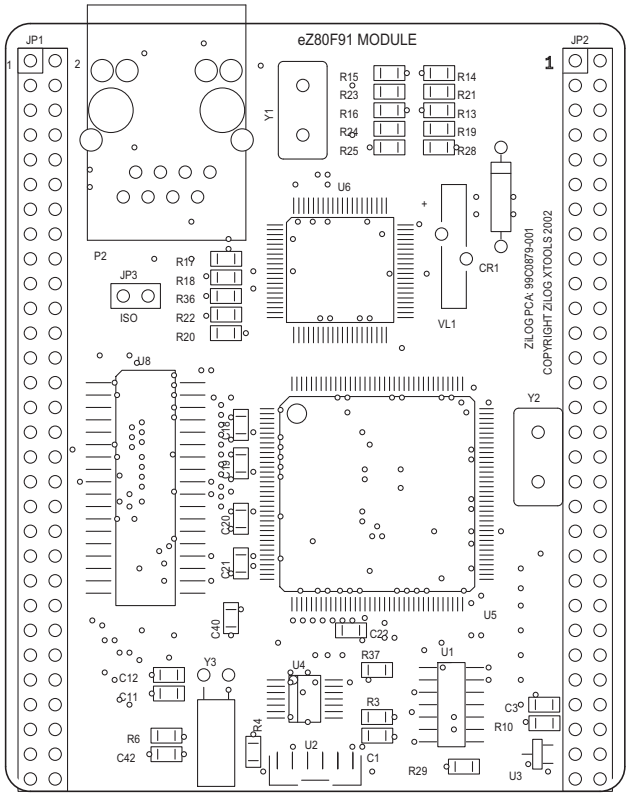

Figure 6. eZ80F91 Module—Top Layer

Figure 7 illustrates the bottom layer silkscreen of the eZ80F91 Module.

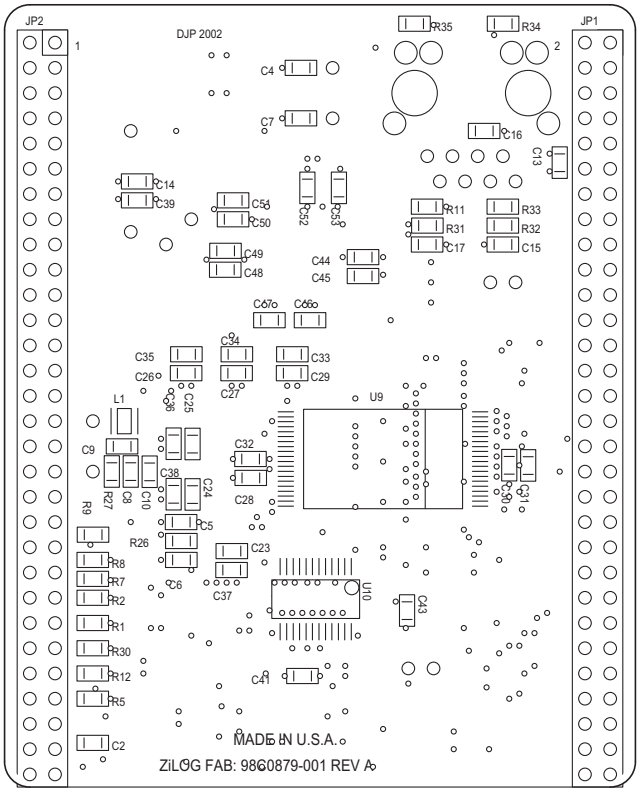

Figure 7. eZ80F91 Module—Bottom Layer

Absolute Maximum Ratings

Stresses greater than those listed in Table 6 can cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs should be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 6. Absolute Maximum Ratings

Parameter	Min	Max	Units
Standard operating temperature	0	+70	ºC
Storage temperature	–45	+85	ºC
Operating Humidity (RH @ 50ºC)	25%	90%	
Operating Voltage	—	3.6	V

Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
0193	Unique Document Number
10	Revision Number
0904	Month and Year Published

Change Log

Rev	Date	Purpose
01	December 2002	Original issue
02	January 2003	Minor content revision
03	February 2003	Minor content revision
04	June 2003	Minor content revision
05	June 2003	Minor content revision
06	August 2003	Hyperlink correction
07	December 2003	Typo correction
08	December 2003	Correction to BOM
09	March 2004	Correction to schematic
10	September 2004	Corrections to PHY section

Module Bill of Materials

Table 7 lists the installed components of the eZ80F91 Module.

Table 7. Bill of Materials for the eZ80F91 Module

Part Number	Part Name	Qty.	Jumper Location	Manufacturer
98C0879-001	Fab, eZ80F91 Module, Rev. B	1	—	Prime Technologies
35-0180-12	IC, SRAM, 512Kx8, 12ns, 3V, 36-SOJ	1	U8	Alliance Semi. AS7C34096-12JC
35-0016-05	IC, 74LVC04, 3.3V, GATE, 14-SOIC	1	U1	Texas Instruments SN74LVC04AD
35-0720-10	IC, Flash, 1Mx8, 100ns, 3V, 40-TSSOP	1	U9	Micron Technologies MT28F008B3VG-10B
35-0719-00	IC, MAX6328, RESET, SOT-23	1	U3	Maxim Inc. MAX6328UR29-T
ZHX1810	IC, IR Transceiver, Low Profile	1	U2	ZiLOG Inc. ZHX1810MV115THTR
35-0062-01	IC, 74LCX32, LV, QUAD OR, 14-TSSOP	1	U4	Fairchild Semi. 74LCX32MTC
35-0022-01	IC, AM7C874, PHY XCVR, 80QFP	1	U6	AMD AM79C874VC
eZ80F91	IC, eZ80F91, 50MHZ, 144VQFP	1	U5	ZiLOG Inc. eZ80F91
35-0731-00	IC, 74CBTLV3861PWR, 24-TSSOP	1	U10	Texas Instruments SN74CBTLV3861PWR
48-1013-01	Diode, TVS Array, XCVR Prot, 8-SOIC	1	U9	Semtec LCDA15C-6
17-2005-70	CAP, 1000pF, 50V, Ceramic Chip, 0603	15	C13, C14, C31-43	Panasonic ECJ-1VC1H561J
17-2005-66	CAP, 0.1µF, 16V, Ceramic Chip, 0603	28	C2,10, C15-30, C44-53	Kemet Inc. C0603C104K5RAC
17-2005-54	CAP, 0.01µF, 50V, Ceramic Chip, 0603	1	C3	Panasonic ECJ-1VB1C103K
17-2005-83	CAP, 0.33µF, 16V, Ceramic Chip, 0603	1	C1	Panasonic ECJ-1VF1C334Z
17-2005-63	CAP, 560pF, 50V, Ceramic Chip, 0603	1	C6	Panasonic ECJ-1VC1H563K

Table 7. Bill of Materials for the eZ80F91 Module (Continued)

Part Number	Part Name	Qty.	Jumper Location	Manufacturer
17-2001-03	CAP, 12pF, 50V, Ceramic Chip, 0603	4	C9, C11, C12	Panasonic ECJ-1VC1H120J
17-2001-05	CAP, 22PF, 50V, CER CHIP, 0603	2	C4, C7	PANASONIC ECJ-1VC1H220J
17-2001-20	CAP, 270PF, 50V, CER CHIP, 0603	1	C5	PANASONIC ECJ-1VC1H271J
17-2001-01	CAP, 5PF, 50V, CER CHIP, 0603	1	C8	PANASONIC ECJ-1VC1H050C
48-0051-00	DIODE, 1N5817, RCTFR	1	CR1	MOTOROLA 1N5817
16-9005-33	INDUCTOR, 3.3µH, 20%, 1210 SMD	1	L1	PANASONIC ELJ-PA3R3MF
46-3001-03	Resistor, 10KΩ, 1%, 1/16W, 0603 SMT	15	R3, 8, 10, R12-18, R20, 25, 29, 30, 37	Sprague 420CK472X2PD
46-3000-00	Resistor, 0Ω, 1%, 1/16W, 0603 SMT	4	R19, 21, 23, 24	"
46-3000-71	Resistor, 2.21KΩ, 1%, 1/16W, 0603 SMT	2	R5, R6	"
46-3000-35	Resistor, 68Ω, 1%, 1/16W, 0603 SMT	1	R3	"
46-3000-02	RES, 2.2Ω, 1%, 1/16W, 0603 SMT	1	R4	"
46-3000-32	RES, 49.9Ω, 1%, 1/16W, 0603 SMT	4	R11, 31, 32, 33	"
46-3000-63	RES, 1KΩ, 1%, 1/16W, 0603 SMT	1	R22	"
46-3000-56	RES, 499Ω,1%, 1/16W, 0603 SMT	1	R26	"
46-3001-34	RES, 200KΩ, 1%, 1/16W, 0603 SMT	1	R27	"
46-3000-47	RES, 221Ω, 1%, 1/16W, 0603 SMT	1	R28	"
46-3000-51	RES, 332Ω, 1%, 1/16W, 0603 SMT	2	R34, R35	"
46-3001-75	RES, 10MΩ, 1%, 1/16W, 0603 SMT	1	R38	"
23-0000-25	XTAL, 25.0000MHz, SER/RESN, HC49S	1	Y1	CITIZEN HC49US25.000MABJ
23-0000-50	XTAL, 50.0000MHz, SER/RESN, HC49S	1	Y2	CITIZEN HC49US50.000MABJ

Table 7. Bill of Materials for the eZ80F91 Module (Continued)

Part Number	Part Name	Qty.	Jumper Location	Manufacturer
23-0006-00	Internal crystal, 32.768KHz, SER/RESN, TF case	1	Y3	Fox NC-38
21-0907-01	Connector, RJ45, Fast jack,10/100 Base-T	1	P2	Halo Electronics HFJ11-2450E-L11
21-0055-02	Connector, HDR/PIN, .025SQ, double row	2	JP1, JP2 (backside)	Harwin M-20-976-3622

Schematics

Figures 8 through 10 diagram the layout of the eZ80F91 Module. Ethernet circuiting devices are not loaded on the eZ80F91 Module. However, these devices appear in the following schematics for reference purposes.

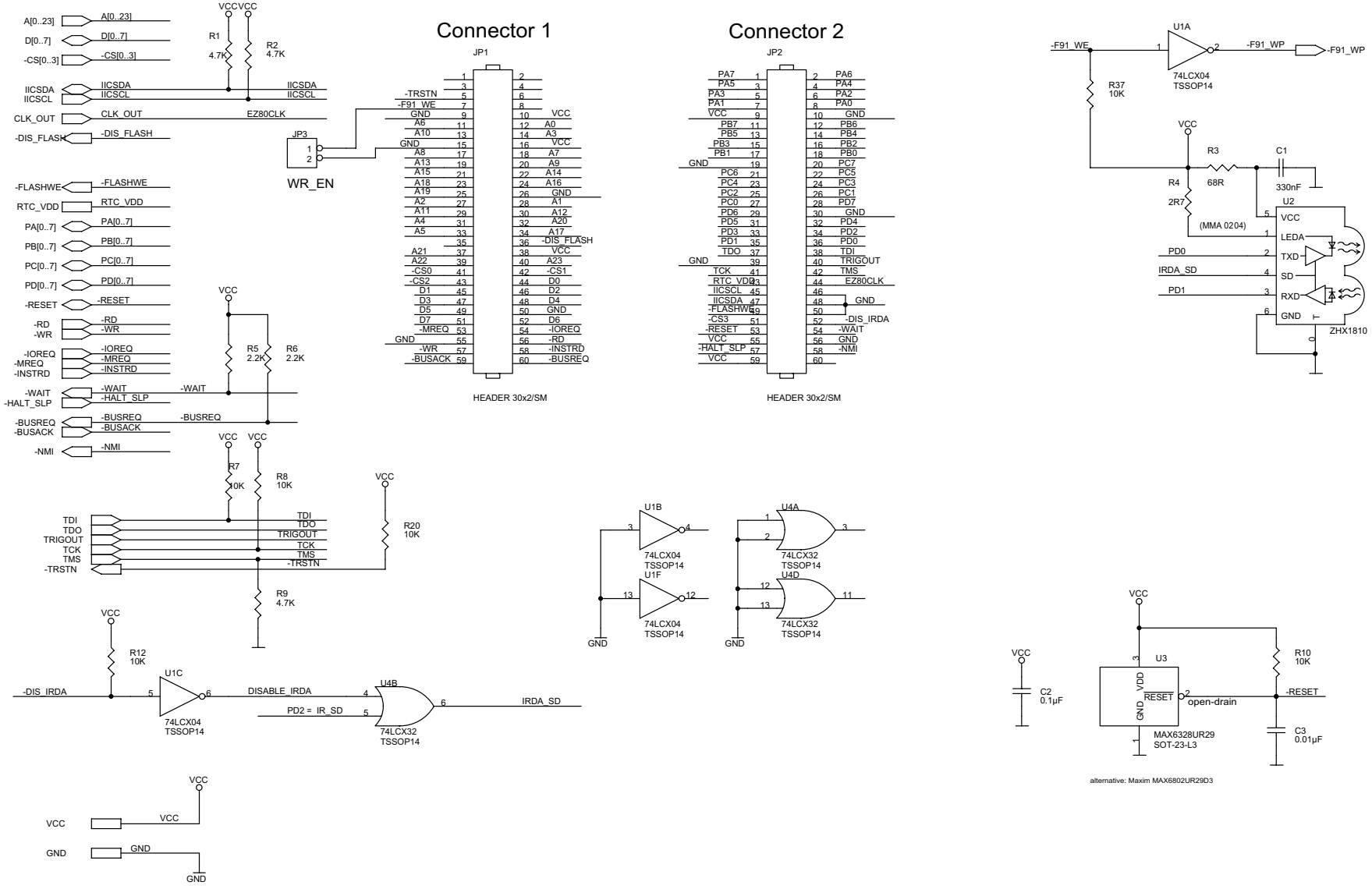

Figure 8. eZ80F91 Module Schematic Diagram, #1 of 3—Connectors and Miscellaneous

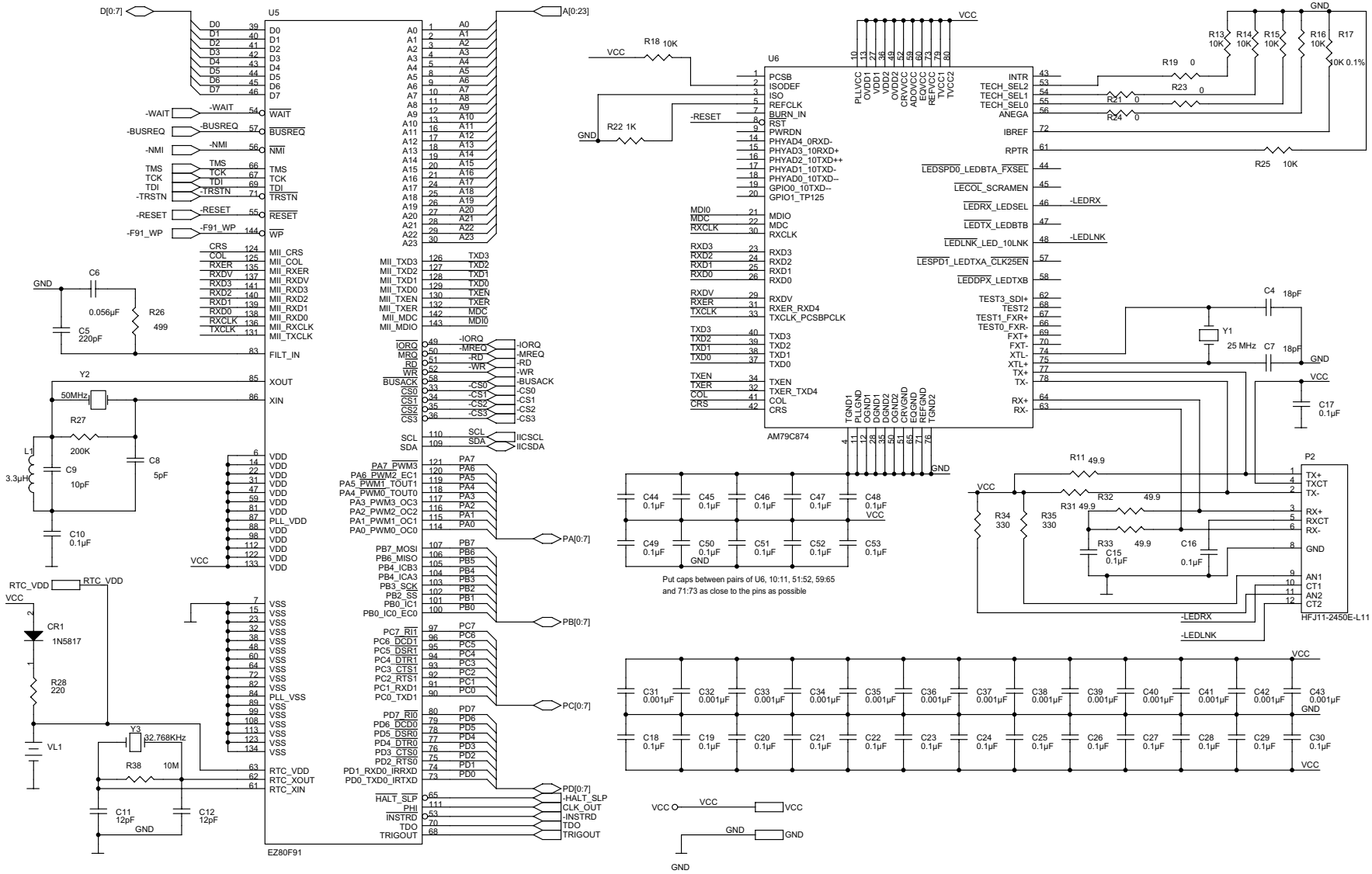

Figure 9. eZ80F91 Module Schematic Diagram, #2 of 3—CPU and PHY

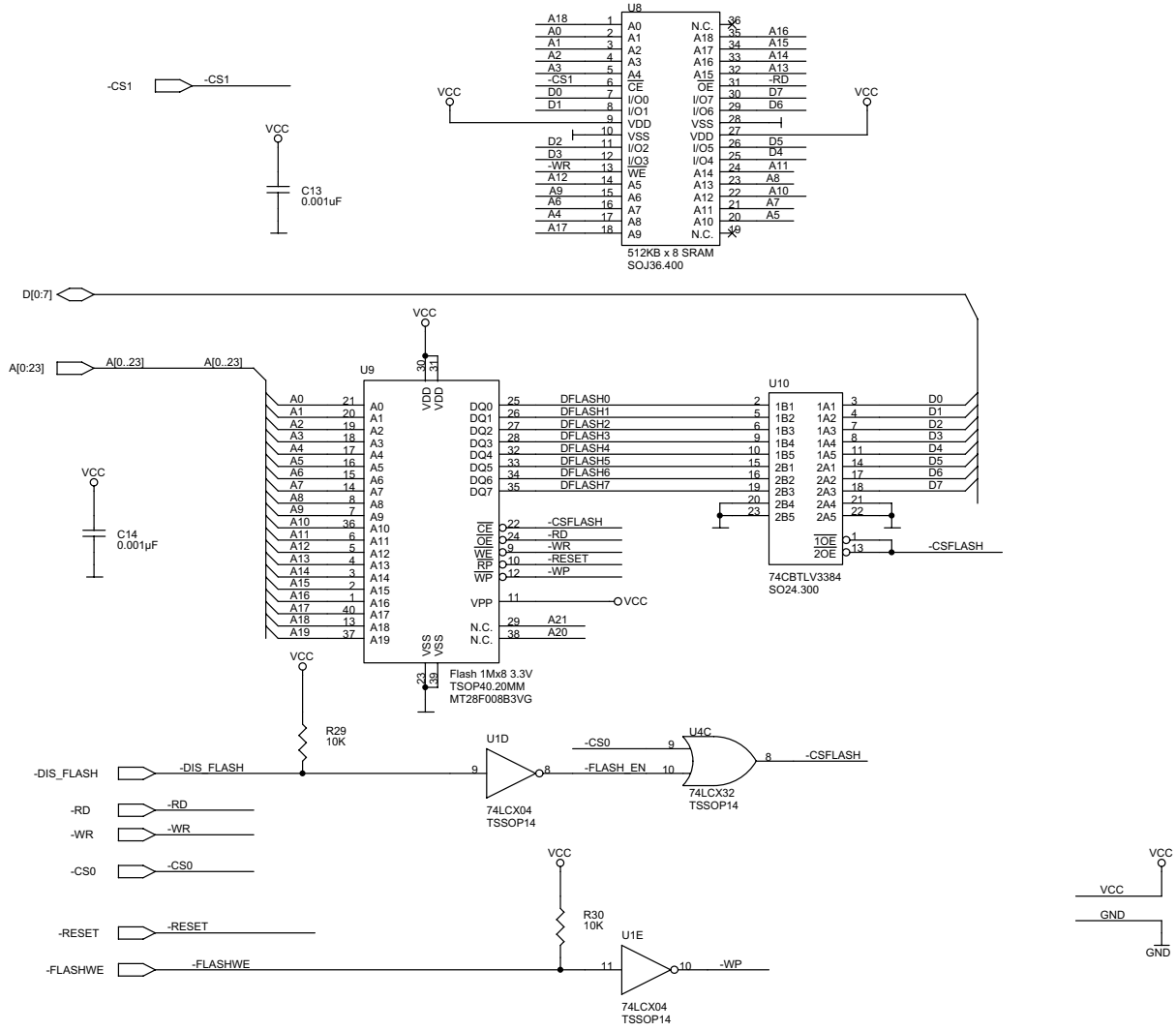

Figure 10. eZ80F91 Module Schematic Diagram, #3 of 3—Module Memory

Customer Feedback Form

The eZ80F91 Module Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	Email

Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
532 Race Street
San Jose, CA 95126
Phone: (408) 558-8500
Fax: (408) 558-8536
ZiLOG Customer Support

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.