



STB130NH02L STP130NH02L

N-CHANNEL 24V - 0.0034 Ω - 120A D²PAK/TO-220 STripFET™ III POWER MOSFET FOR DC-DC CONVERSION

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB130NH02L	24 V	< 0.0044 Ω	90 A ⁽²⁾
STP130NH02L	24 V	< 0.0044 Ω	90 A ⁽²⁾

- TYPICAL R_{DS(on)} = 0.0034 Ω @ 10 V
- TYPICAL R_{DS(on)} = 0.005 Ω @ 5 V
- R_{DS(on)} * Q_g INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING D²PAK (TO-263)
POWER PACKAGE IN TUBE (NO SUFFIX) OR
IN TAPE & REEL (SUFFIX "T4")

DESCRIPTION

The STB_P130NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. It is ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

APPLICATIONS

- SYNCHRONOUS RECTIFICATIONS FOR
TELECOM AND COMPUTER
- OR-ING DIODE

Figure 1: Package

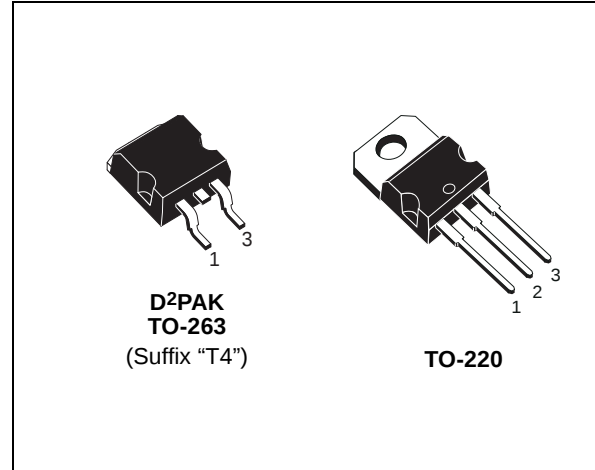


Figure 2: Internal Schematic Diagram

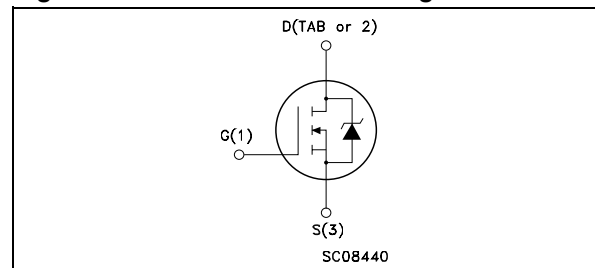


Table 2: Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB130NH02LT4	B130NH02L	TO-263	TAPE & REEL
STP130NH02L	P130NH02L	TO-220	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{spike(1)}	Drain-source Voltage Rating	30	V
V _{DS}	Drain-source Voltage (V _{GS} = 0)	24	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	24	V
V _{GS}	Gate- source Voltage	± 20	V
I _D ⁽²⁾	Drain Current (continuous) at T _C = 25°C	90	A
I _D ⁽²⁾	Drain Current (continuous) at T _C = 100°C	90	A
I _{DM} ⁽³⁾	Drain Current (pulsed)	360	A
P _{tot}	Total Dissipation at T _C = 25°C	150	W
	Derating Factor	1	W/°C
E _{AS} ⁽⁴⁾	Single Pulse Avalanche Energy	900	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Max. Operating Junction Temperature		

STB130NH02L STP130NH02L**Table 4: THERMAL DATA**

Rthj-case	Thermal Resistance Junction-case	Max	1.0	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)**Table 5: OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 25 mA, V _{GS} = 0	24			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = 20 V V _{DS} = 20 V T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

Table 6: ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 45 A V _{GS} = 5 V I _D = 22.5 A		0.0034 0.005	0.0044 0.008	Ω Ω

Table 7: DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (5)	Forward Transconductance	V _{DS} = 10 V I _D = 45 A		55		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 15V f = 1 MHz V _{GS} = 0		4450 1126 141		pF pF pF
R _G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1.6		Ω

ELECTRICAL CHARACTERISTICS (continued)**Table 8: SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 10\text{ V}$ $I_D = 45\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure)		14 224		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=10\text{ V}$ $I_D=90\text{ A}$ $V_{GS}=10\text{ V}$		69 13 9	93	nC nC nC
$Q_{oss}^{(6)}$	Output Charge	$V_{DS} = 16\text{ V}$ $V_{GS} = 0\text{ V}$		27		nC
$Q_{gls}^{(7)}$	Third-quadrant Gate Charge	$V_{DS} < 0\text{ V}$ $V_{GS} = 10\text{ V}$		64		nC

Table 9: SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 10\text{ V}$ $I_D = 45\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		69 40	54	ns ns

Table 10: SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				90 360	A A
$V_{SD}^{(5)}$	Forward On Voltage	$I_{SD} = 45\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 90\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_J = 150^\circ\text{C}$ (see test circuit, Figure 5)		47 58 2.5		ns nC A

(1) Guaranteed when external $R_g=4.7\ \Omega$ and $t_f < t_{fmax}$.

(2) Value limited by wire bonding

(3) Pulse width limited by safe operating area.

(4) Starting $T_J = 25^\circ\text{C}$, $I_D = 45\text{ A}$, $V_{DD} = 10\text{ V}$.(5) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.(6) $Q_{oss} = C_{oss} \cdot \Delta V_{in}$, $C_{oss} = C_{gd} + C_{ds}$. See Appendix A

(7) Gate charge for synchronous operation

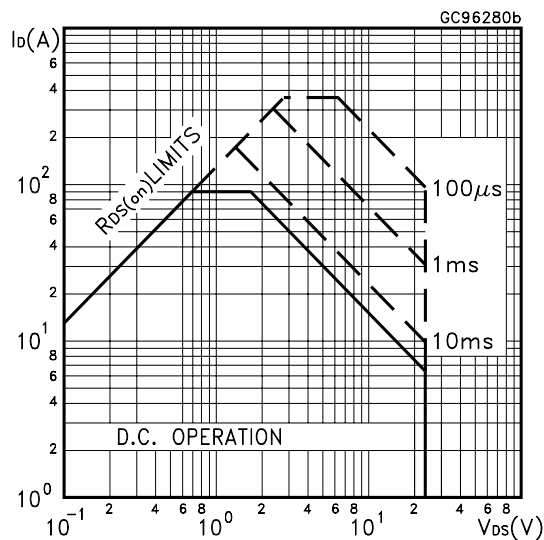
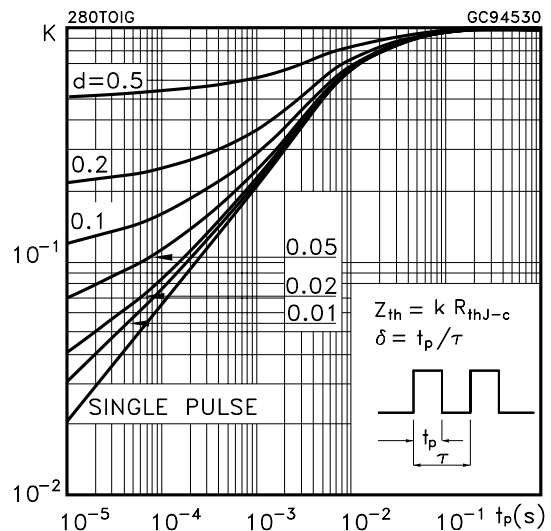
Figure 3: Safe Operating Area**Figure 4: Thermal Impedance**

Figure 5: Output Characteristics

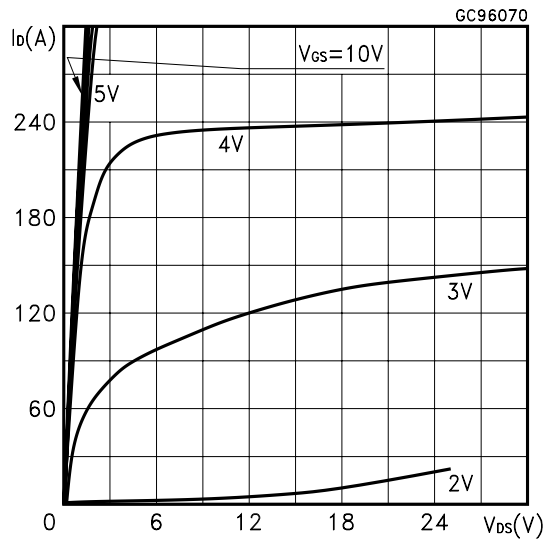


Figure 7: Transconductance

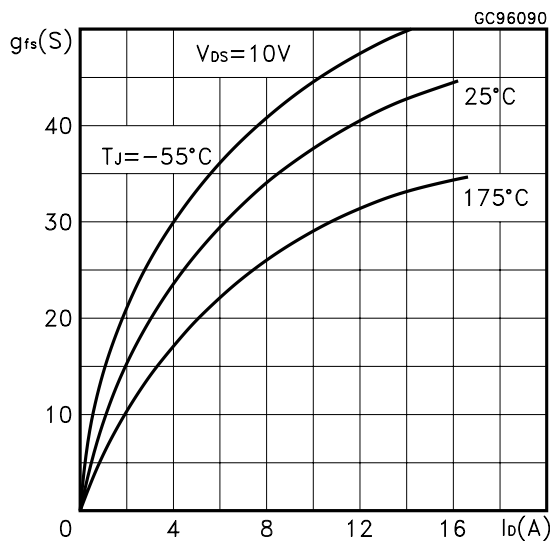


Figure 9: Gate Charge vs Gate-source Voltage

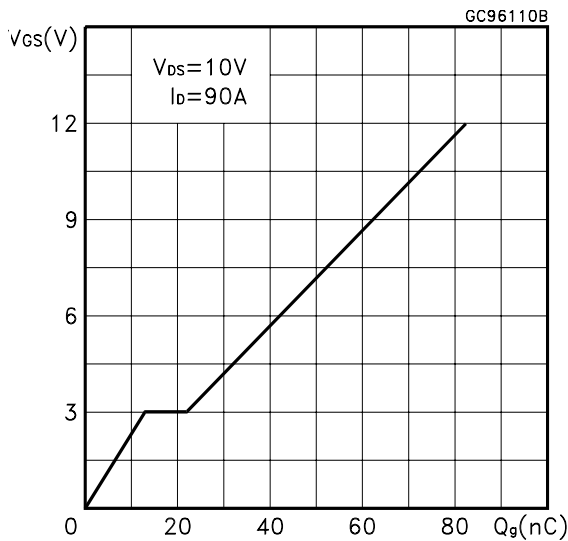


Figure 6: Transfer Characteristics

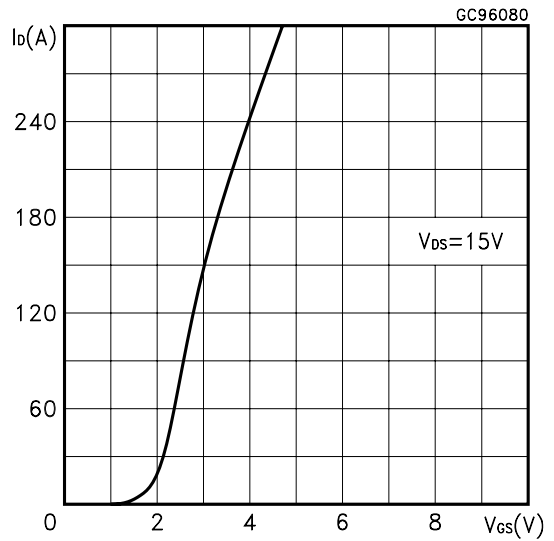


Figure 8: Static Drain-source On Resistance

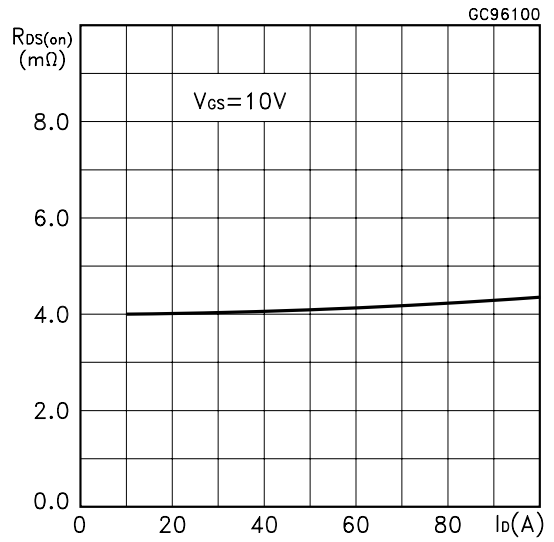


Figure 10: Capacitance Variations

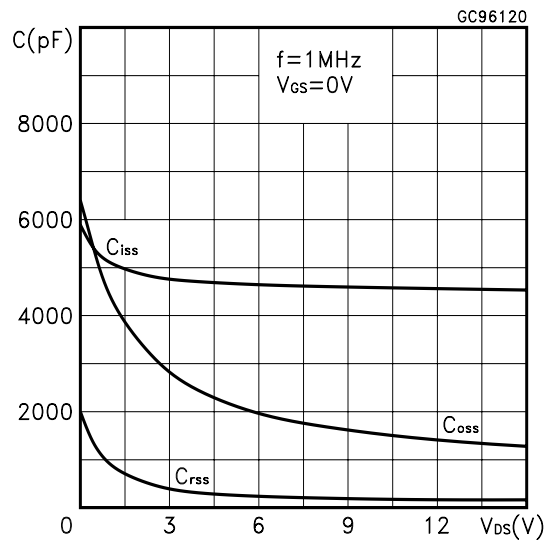


Figure 11: Normalized Gate Threshold Voltage vs Temperature

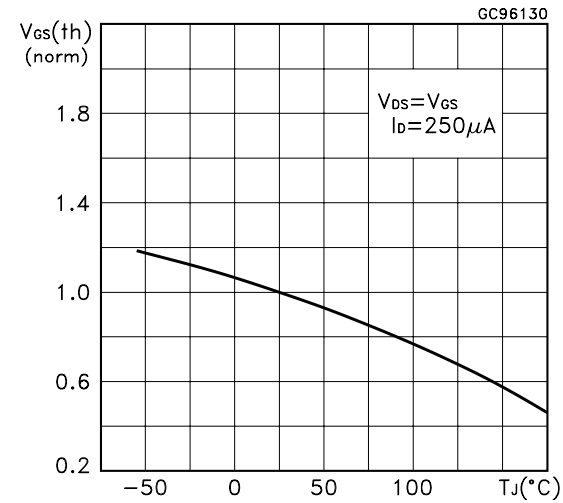


Figure 13: Source-drain Diode Forward Characteristics

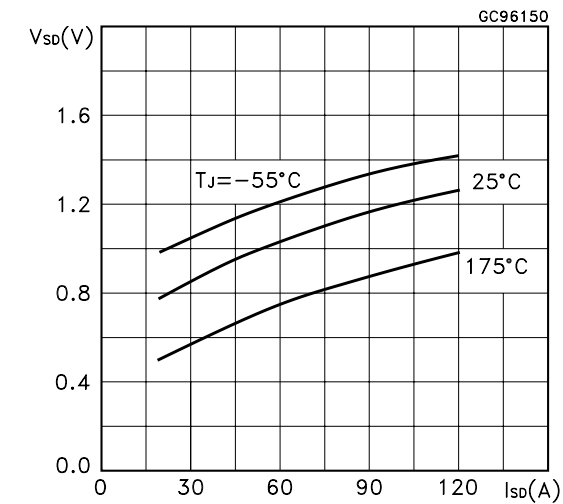


Figure 12: Normalized on Resistance vs Temperature

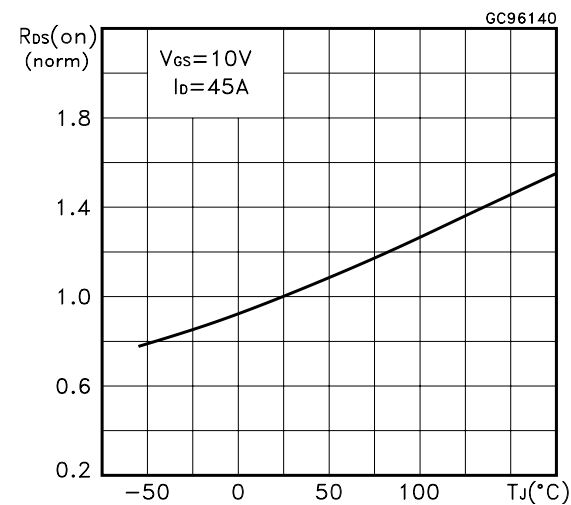


Figure 14: Normalized Breakdown Voltage vs Temperature

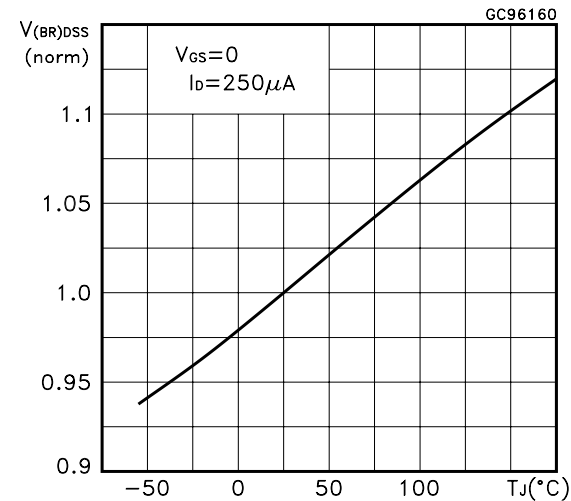


Figure 15: Unclamped Inductive Load Test Circuit

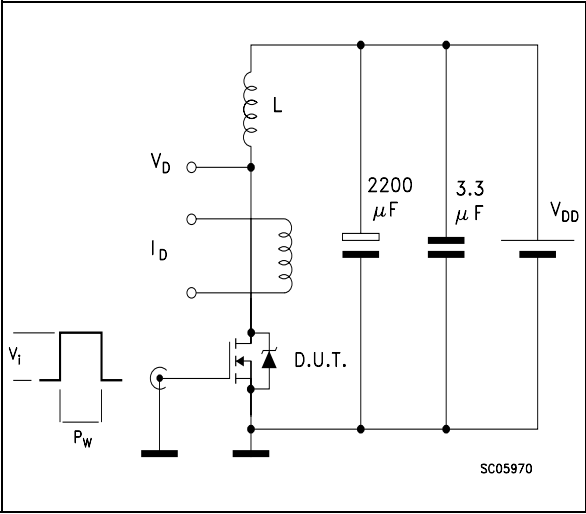


Figure 16: Unclamped Inductive Waveform

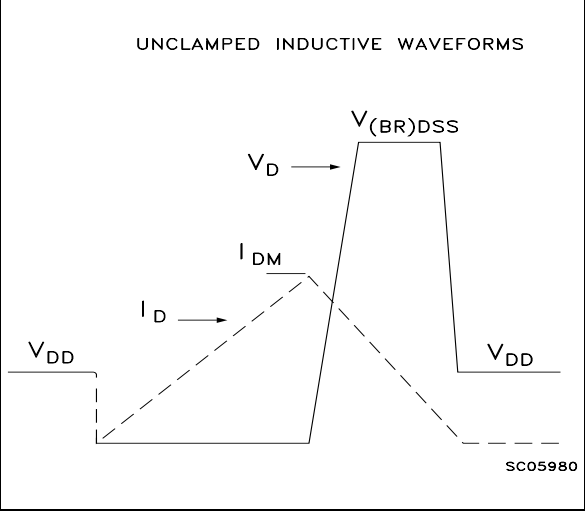


Figure 17: Switching Times Test Circuits For Resistive Load

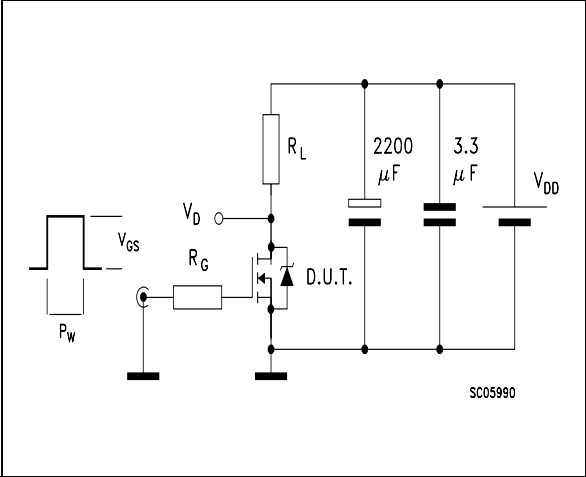


Figure 18: Gate Charge test Circuit

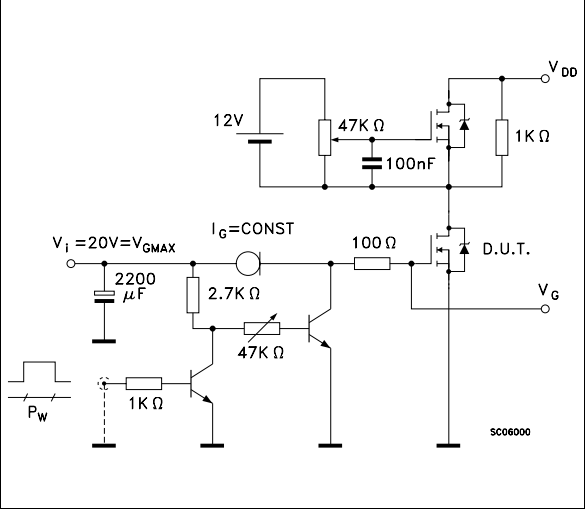
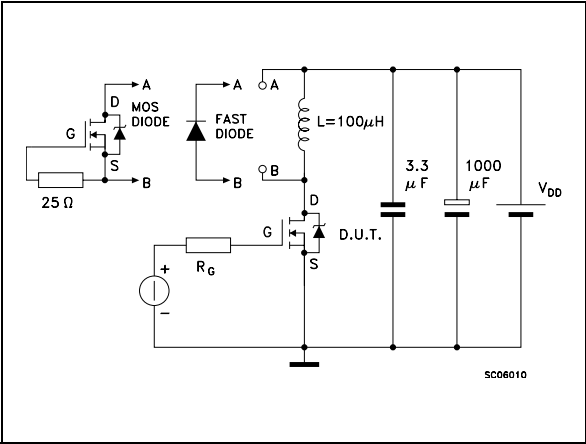
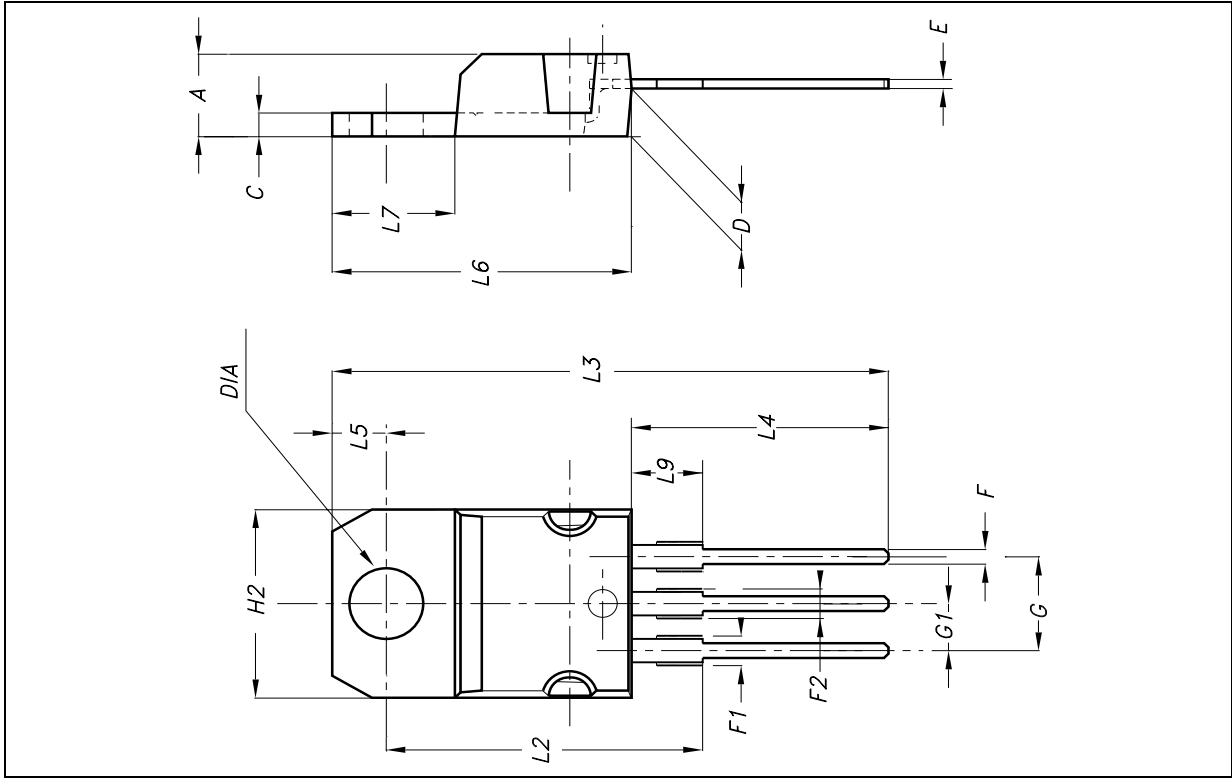


Figure 19: Test Circuit For Inductive Load Switching And Diode Recovery Times



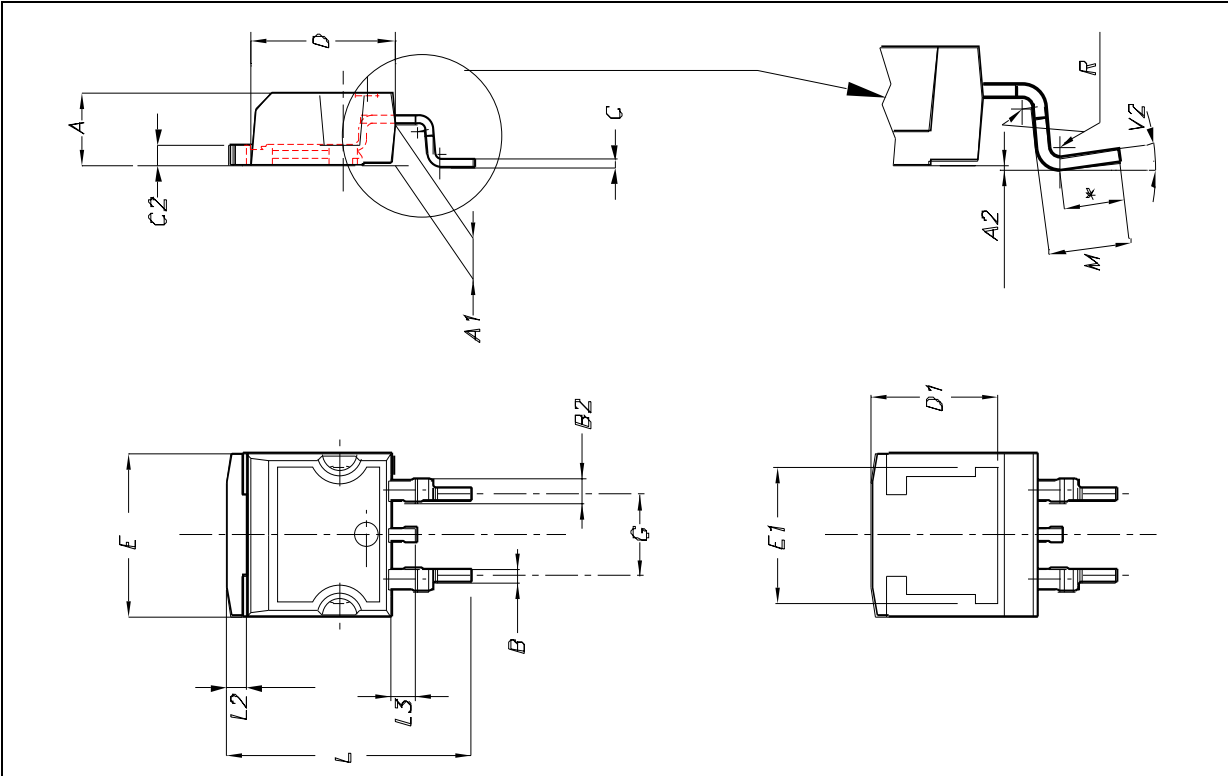
TO-220 MECHANICAL DATA

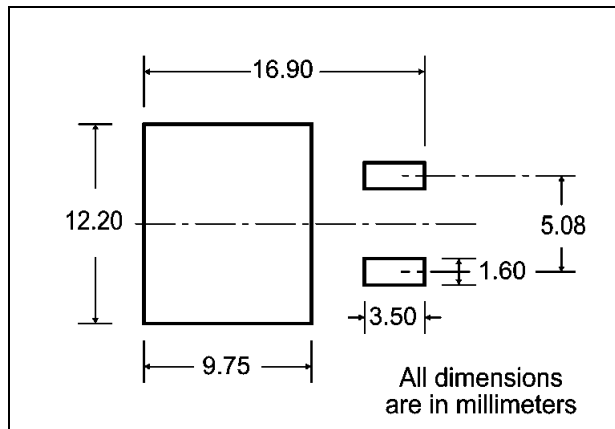
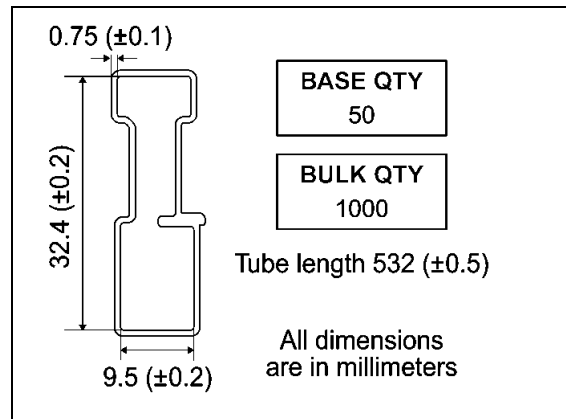
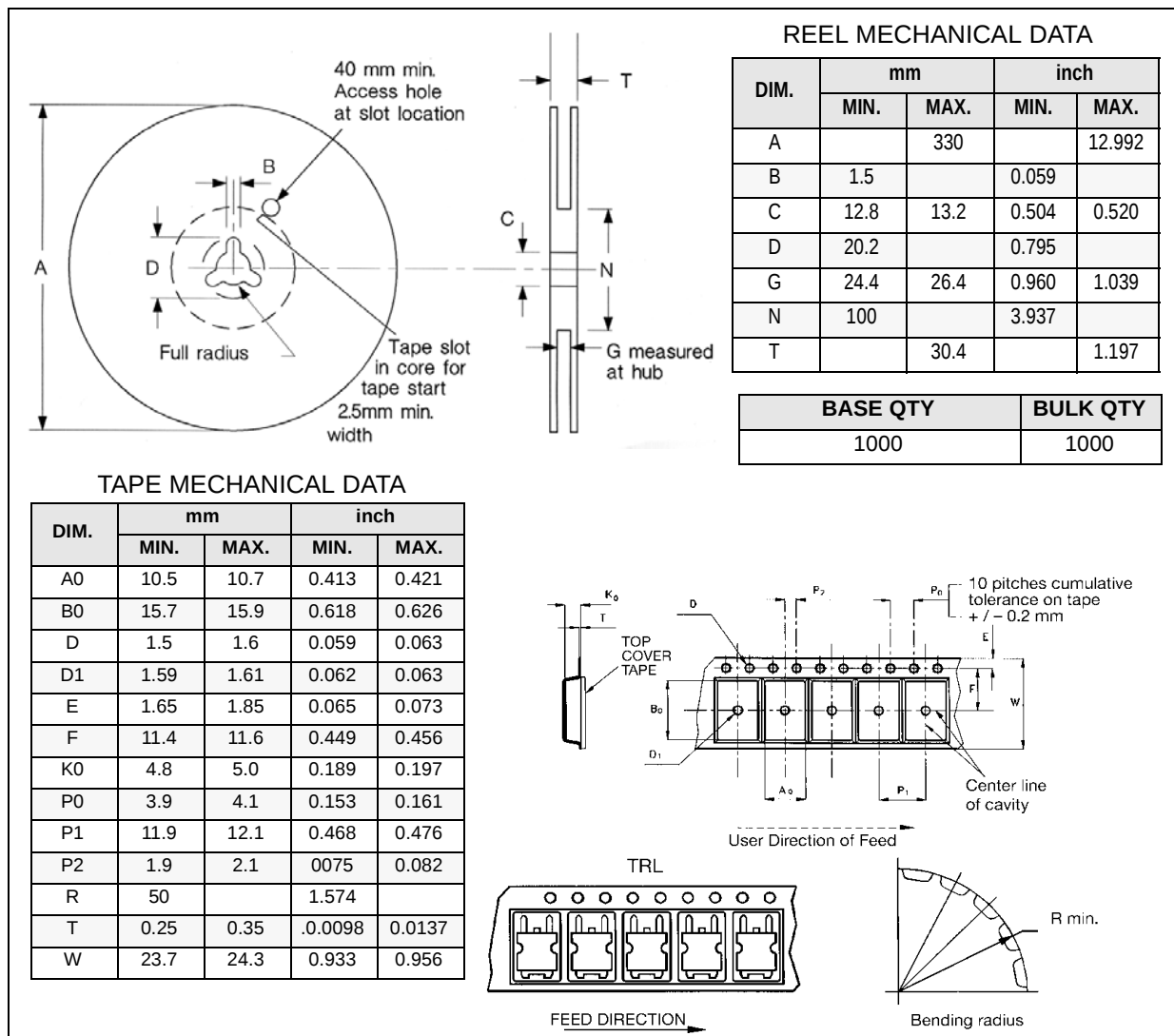
DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.40		2.70	0.094		0.106
H2	10		10.40	0.393		0.409
L2		16.40			0.645	
L3		28.90			1.137	
L4	13		14	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.20		6.60	0.244		0.260
L9	3.50		3.93	0.137		0.154
DIA	3.75		3.85	0.147		0.151



D²PAK MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°

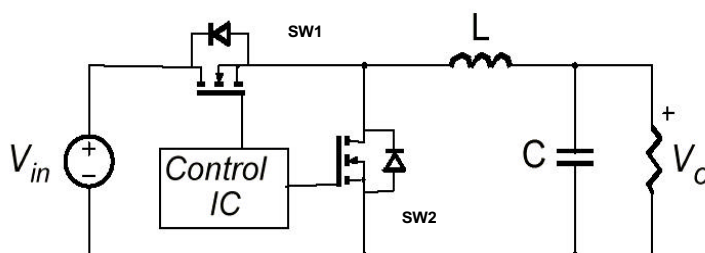


D2PAK FOOTPRINT**TUBE SHIPMENT (no suffix)*****TAPE AND REEL SHIPMENT (suffix "T4")***

* on sales type

APPENDIX A

Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW₁ during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{\text{conduction}}$		$R_{\text{DS(on)SW1}} * I_L^2 * \delta$	$R_{\text{DS(on)SW2}} * I_L^2 * (1 - \delta)$
$P_{\text{switching}}$		$V_{\text{in}} * (Q_{\text{gsth(SW1)}} + Q_{\text{gd(SW1)}}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	$^1 V_{\text{in}} * Q_{\text{rr(SW2)}} * f$
	Conduction	Not Applicable	$V_{\text{r(SW2)}} * I_L * t_{\text{deadtime}} * f$
$P_{\text{gate(Q}_G)}$		$Q_{\text{gs(SW1)}} * V_{\text{gg}} * f$	$Q_{\text{gls(SW2)}} * V_{\text{gg}} * f$
P_{Qoss}		$\frac{V_{\text{in}} * Q_{\text{oss(SW1)}} * f}{2}$	$\frac{V_{\text{in}} * Q_{\text{oss(SW2)}} * f}{2}$

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
PQoss	Output capacitance losses

¹ Dissipated by SW1 during turn-on

Table 11:Revision History

Date	Revision	Description of Changes
April 2005	2.0	ADDED PACKAGE TO-220

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