

# VN330SP-32-E QUAD HIGH SIDE SMART POWER SOLID STATE RELAY

## **General Features**

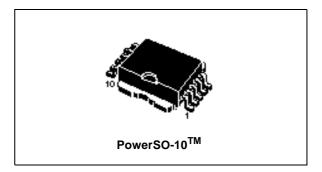
Туре	$V_{demag}(*)$	$R_{DSon}(*)$	I <sub>out</sub> (*)	v <sub>cc</sub>
VN330SP-32-E	V <sub>CC</sub> -55V	<b>0.32</b> Ω(**)	1A	36V

(\*)Per channel.

(\*\*)at TJ = 85 °C

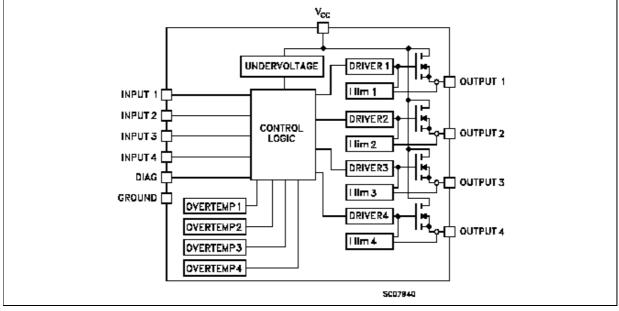
## Features

- OUTPUT CURRENT : 1A PER CHANNEL
- DIGITAL INPUT CLAMPED AT 32V MINIMUM VOLTAGE
- SHORTED LOAD AND OVER-TEMPERATURE PROTECTIONS
- BUILT-IN CURRENT LIMITER
- UNDERVOLTAGE SHUT-DOWN
- OPEN DRAIN DIAGNOSTIC OUTPUT
- FAST DEMAGNETIZATION OF INDUCTIVE LOADS



### Description

The VN330SP-32-E is a monolithic device made using STMicroelectronics VIPower Technology, intended for driving four indipendent resistive or inductive loads with one side connected to ground. Active current limitation avoids dropping the system power supply in case of shorted load. Built-in thermal shut-down protects the chip from overtemperature and short circuit. The open drain diagnostic output indicates over-temperature conditions.



## Block Diagram

Rev 3

1/14

57

	<b>j</b>		
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power supply voltage	45	V
-V <sub>CC</sub>	Reverse supply voltage	-0.3	V
I <sub>OUT</sub>	Output current (continuos)	Internally limited	Α
I <sub>R</sub>	Reverse output current (per channel)	-6	Α
I <sub>IN</sub>	Input current (per channel)	± 10	mA
I <sub>DIAG</sub>	Diag pin current	± 10	mA
$V_{ESD}$	Electrostatic discharge (R = 1.5KW; C = 100pF)	2000	V
E <sub>AS</sub>	E <sub>AS</sub> Single pulse avalanche energy per channel not simultaneously <i>Figure 3.</i>		mJ
P <sub>tot</sub>	Power dissipation at $T_c \le 25^{\circ}C$	Internally limited	W
TJ	Junction operating temperature	Internally limited	°C
T <sub>stg</sub>	Storage Temperature	-55 to 150	°C

 Table 1.
 Absolute Maximum Rating

### Figure 1. Connection Diagram (Top View)

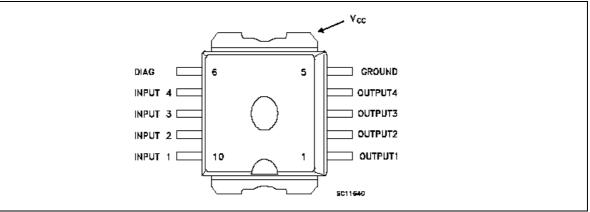
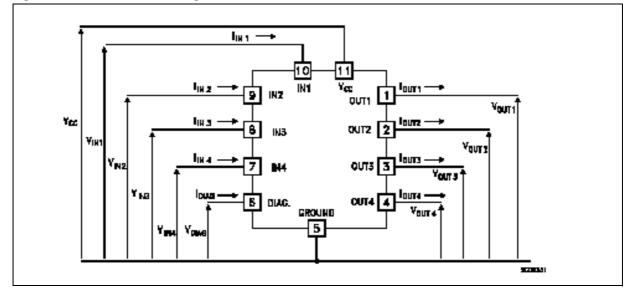


Figure 2. Current and Voltage Conventions



Symbol	Symbol Parameter		Max Value	Unit
R <sub>thJC</sub>	Thermal resistance junction-case (Note:1)	Max	2	°C/W
R <sub>thJA</sub>	Thermal resistance junction-ambient (Note:2)	Max	50	°C/W

#### Table 2. Thermal data

Note: 1.Per channel

Note: 2. When mounted using minimum recommended pad size on FR-4 board

**Electrical Chracteristics** (10V <  $V_{CC}$  < 36V; -25°C <  $T_J$  < 125°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>CC</sub>	Supply voltage		10		36	V
		I <sub>OUT</sub> = 0.5A; T <sub>J</sub> = 125°C			0.4	Ω
R <sub>ON</sub>	On state resistance	I <sub>OUT</sub> = 0.5A; T <sub>J</sub> = 85°C			0.32	Ω
		I <sub>OUT</sub> = 0.5A; T <sub>J</sub> = 25°C			0.2	Ω
l.	Supply surrent	All channels OFF; V <sub>IN</sub> = 30V;			1	mA
IS	Supply current	On state; $T_J = 125^{\circ}C I_{OUT1}I_{OUT4} = 0V$			10	mA
V <sub>demag</sub>	Output voltage at turn-off	I <sub>OUT</sub> = 0.5A; L <sub>LOAD</sub> >= 1mH	V <sub>CC</sub> -65	$V_{CC}$ -55	V <sub>CC</sub> -45	V

#### Table 3. Power Section

#### Table 4.Logical Input

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>IL</sub>	Input low level voltage				2	V
V <sub>IH</sub>	Input high level voltage .	Note:3	3.5			V
V <sub>I(HYST)</sub>	Input hysteresis voltage			0.5		V
Lu.	Input current	V <sub>IN</sub> = 0 to 30V			600	μΑ
I <sub>IN</sub>	input current	$V_{IN} = 0$ to 2V	25			μΑ
I <sub>LGND</sub>	Output current in ground disconnection	$V_{CC} = V_{INn} = GND = DIAG = 24V;$ T <sub>J</sub> = 25°C			25	mA
View	Input clamp voltage	I <sub>IN</sub> = 1mA	32	36		V
V <sub>ICL</sub>	Note:3	I <sub>IN</sub> = -1mA		-0.7		V

Note: 3.The input voltage is internally clamped at 32V minimum, it is possible to connect the input pins to an higher voltage via an external resistor calculate to not exceed 10mA



Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
+	Turn-on delay time of	$I_{OUT} = 0.5A$ , Resistive Load Input rise time < 0.1 $\mu$ s,				
t <sub>d(ON)</sub>	Output current	$T_J = 25^{\circ}C$		30	40	μs
		T <sub>J</sub> = 125°C			60	μs
+	Rise time of Output	$I_{OUT} = 0.5A$ , Resistive Load Input rise time < 0.1 $\mu$ s,				
t <sub>r</sub>	current	$T_J = 25^{\circ}C$		50	100	μs
		T <sub>J</sub> = 125°C			115	μs
1	Turn-off delay time of	$I_{OUT} = 0.5A$ , Resistive Load Input rise time < 0.1 $\mu$ s,				
t <sub>d(OFF)</sub>	Output current	$T_J = 25^{\circ}C$		20	30	μs
		T <sub>J</sub> = 125°C			40	μs
+	Fall time of Output	$I_{OUT} = 0.5A$ , Resistive Load Input rise time < 0.1 $\mu$ s,				
t <sub>f</sub>	current	$T_J = 25^{\circ}C$		8	15	μs
		T <sub>J</sub> = 125°C			20	μs
(di/dt) <sub>on</sub>		I <sub>OUT</sub> = 0.5A,			0.5	A/μs
(u) u) on	Turn-on current slope	$I_{OUT} = I_{LIM}, T_J = 25^{\circ}C$			2	A/μs
(di/dt) <sub>off</sub>	Turn-off current slope	I <sub>OUT</sub> = 0.5A,			2	A/μs
(un un off		$I_{OUT} = I_{LIM}, T_J = 25^{\circ}C$			4	A/μs

Table 5.Switching ( $V_{CC} = 24V$ )

#### Table 6. Protections

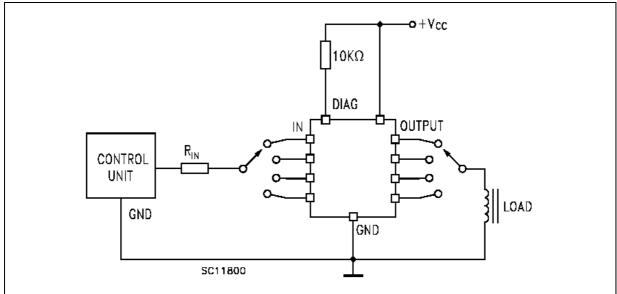
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>DIAG</sub> (*)	Status voltage output low	I <sub>DIAG</sub> = 5mA ( Fault condition )			1	V
V(*)	) Status alamp valtaga	I <sub>DIAG</sub> = 1mA	32	36		V
V <sub>SCL</sub> (*)	Status clamp voltage	I <sub>DIAG</sub> = -1mA		-0.7		V
V <sub>USD</sub>	Undervoltage shut down		5		8	V
I <sub>LIM</sub>	DC Short circuit current	$V_{CC} = 24V; R_{LOAD} < 10m\Omega$	1		2.5	А
I <sub>OVPK</sub>	Peak short circuit current	$V_{CC} = 24V; V_{IN} = 30V; R_{LOAD} < 10m\Omega$			4	А
I <sub>DIAGH</sub>	Leakage on diag pin in high state	V <sub>DIAG</sub> = 24V			100	μΑ
I <sub>LOAD</sub>	Output leakage current	V <sub>CC</sub> = 10 to 36V; V <sub>IN</sub> = V <sub>IL</sub> 4 Channels in Parallel			25	μΑ
t <sub>SC</sub>	Delay time of current limiter				100	μs
T <sub>TSD</sub>	Thermal shut down temperature		150	170		°C
Τ <sub>R</sub>	Thermal reset temperature		135	155		°C

(\*)Status determination > 100ms after the switching edge.

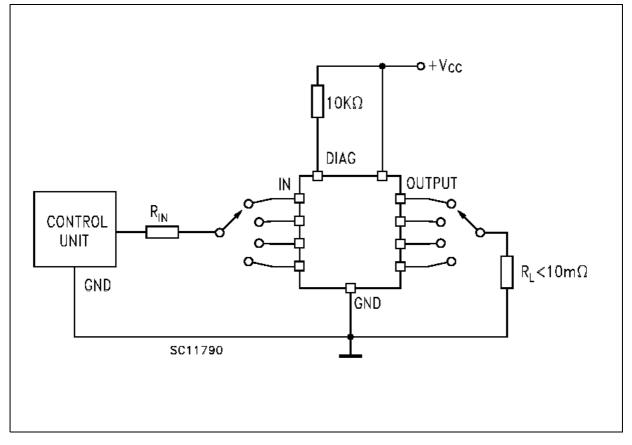
Note: If INPUT pin is floating the corrisponding channel will automatically switch OFF. If GND pin is disconnected, the channel will switch OFF provided V<sub>CC</sub> not exceed 36V.









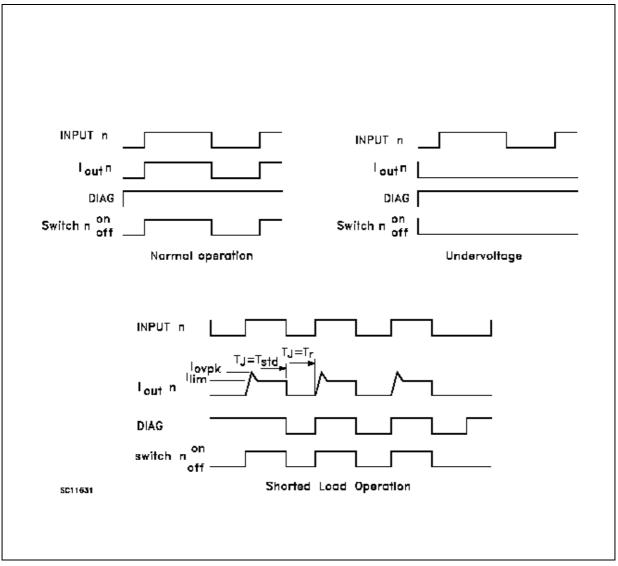




Conditions	INPUTn	OUTPUTn	Diagnostic
Normal operation	L	L H	H H
Overtemperature	L	L	H L
Undervoltage	L	L	H H
Shorted load ( Current limitation )	L	L H	H H

#### Table 7.Truth Table

### Figure 5. Switching Waveforms





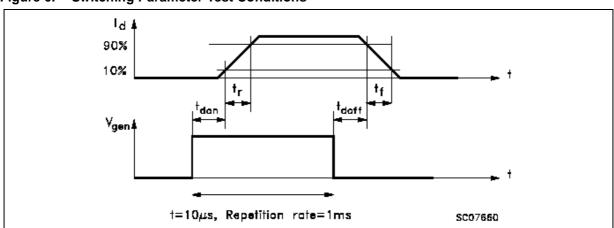
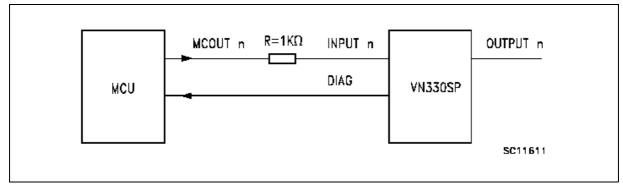


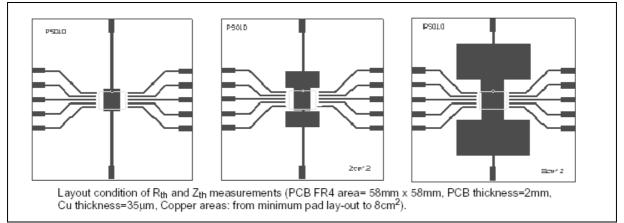
Figure 6. Switching Parameter Test Conditions





## PowerSO-10<sup>™</sup> Thermal Data







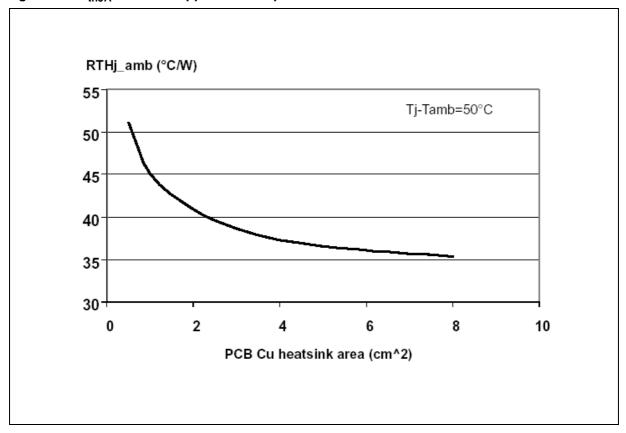


Figure 9.  $R_{thJA}$  Vs. PBC copper area in open box free air condition



### **Mechanical Data**

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



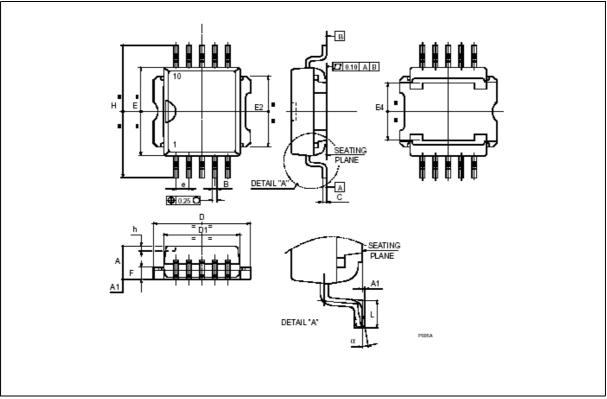
57

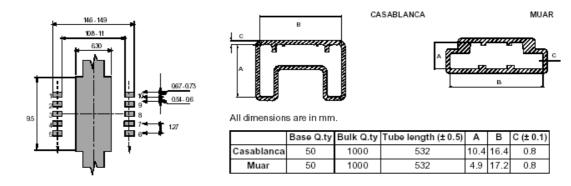
Sumbol		millimeters	
Symbol	Min	Тур	Max
А	3.35		3.65
A (*)	3.4		3.6
A1	0.00		0.10
В	0.40		0.60
B (*)	0.37		0.53
C	0.35		0.55
C (*)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 (*)	7.30		7.50
E4	5.90		6.10
E4 (*)	5.90		6.30
e		1.27	
e F	1.25		1.35
E (*)	1.20		1.40
Ĥ	13.80		14.40
H (*)	13.85		14.35
h		0.50	
L	1.20		1.80
L (*)	0.80		1.10
а	0°		8°
α (*)	2°		8°

## Table 8. PowerSO-10<sup>TM</sup> Mechanical Data

Note: (\*) Muar only POA P013P

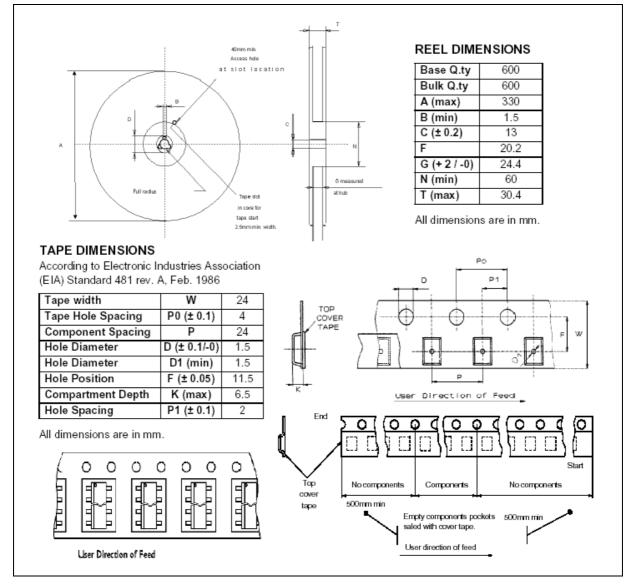






### Figure 11. PowerSO-10<sup>TM</sup> Suggested Pad and Tube Shipment (No Suffix)







#### Table 9.Order Codes

Package	Tube	Tape and Reel
PowerSO-10 <sup>TM</sup>	VN330SP-32-E	VN330SPTR-32-E

### VN330SP-32-E

Table 10.Revision History

Date	Revision	Changes
5-Sep-2005	3	Final release



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

