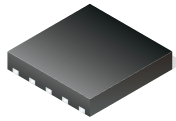


120-V Boot, 4-A Peak, High Frequency High-Side/Low-Side Driver

Check for Samples: UCC27210, UCC27211

FEATURES

- **Drives Two N-Channel MOSFETs in High-Side/Low-Side Configuration with Independent Inputs**
- **Maximum Boot Voltage 120-V DC**
- **4-A Sink, 4-A Source Output Currents**
- **0.9-Ω Pull-Up/Pull-Down Resistance**
- **Input Pins can Tolerate -10 V to 20 V and are Independent of Supply Voltage Range**
- **TTL or Pseudo-CMOS Compatible Input Versions**
- **8-V to 17-V VDD Operating Range, (20 V ABS MAX)**
- **7.2-ns Rise and 5.5-ns Fall Time with 1000-pF Load**
- **Fast Propagation Delay Times (18 ns typical)**
- **2-ns Delay Matching**
- **Symmetrical Under Voltage Lockout for High-Side and Low-Side Driver**
- **All Industry Standard Packages Available (SOIC-8, PowerPAD™ SOIC-8, 4-mm x 4-mm SON-8 and 4-mm x 4-mm SON-10)**
- **Specified from -40 to 140 °C**

APPLICATIONS

- **Power Supplies for Telecom, Datacom, and Merchant**
- **Half-Bridge and Full-Bridge Converters**
- **Push-Pull Converters**
- **High Voltage Synchronous-Buck Converters**
- **Two-Switch Forward Converters**
- **Active-Clamp Forward Converters**
- **Class-D Audio Amplifiers**

DESCRIPTION

The UCC27210 and UCC27211 Drivers are based on the popular UCC27200 and UCC27201 MOSFET drivers, but offer several significant performance improvements. Peak output pull-up and pull-down current has been increased to 4-A source/4-A sink, and pull-up/pull-down resistance have been reduced to 0.9 Ω, thereby allowing for driving large power MOSFETs with minimized switching losses during the transition through the MOSFET's Miller Plateau. The input structure is now able to directly handle -10 VDC, which increases robustness and also allows direct interface to gate-drive transformers without using rectification diodes. The inputs are also independent of supply voltage and have a 20-V maximum rating.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONT.)

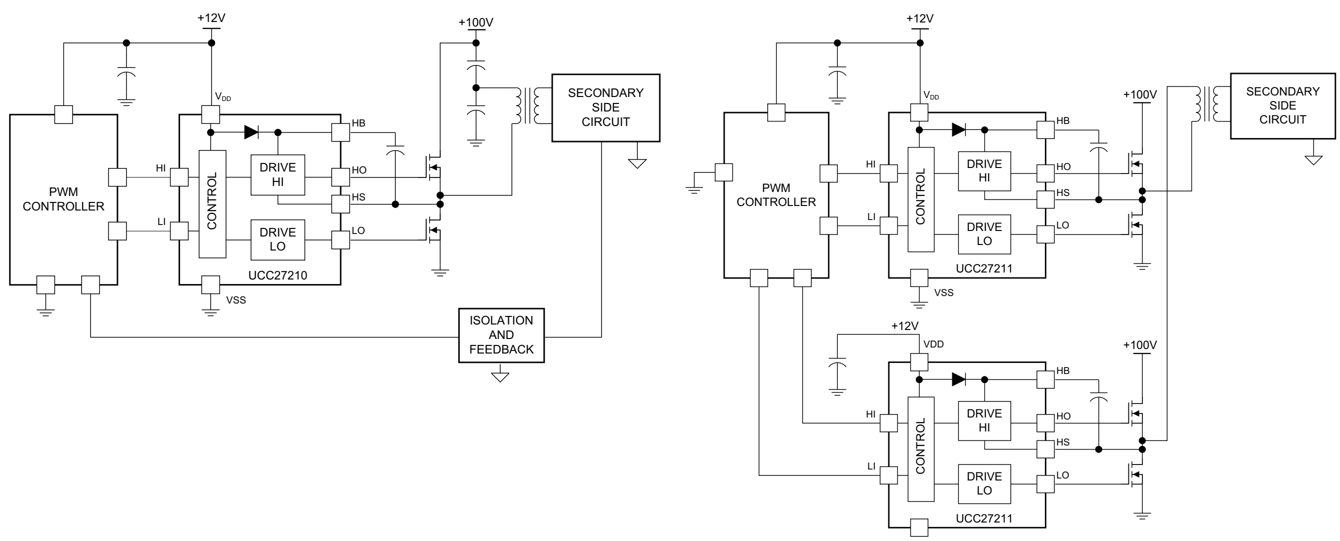
The UCC27210/1's switching node (HS pin) is able to handle -18 V maximum which allows the high-side channel to be protected from inherent negative voltages caused parasitic inductance and stray capacitance. The UCC27210 (Pseudo-CMOS inputs) and UCC27211 (TTL inputs) have increased hysteresis allowing for interface to analog or digital PWM controllers with enhanced noise immunity.

The low-side and high-side gate drivers are independently controlled and matched to 2 ns between the turn on and turn off of each other.

An on-chip 120-V rated bootstrap diode eliminates the external discrete diodes. Under-voltage lockout is provided for both the high-side and the low-side drivers providing symmetric turn-on/turn-off behavior and forcing the outputs low if the drive voltage is below the specified threshold.

Both devices are offered in 8-pin SOIC (D), PowerPAD™ SOIC-8 (DDA), 4-mm x 4-mm SON-8 (DRM) and SON-10 (DPR) packages.

Typical Application Diagrams



ORDERING INFORMATION (1)

TEMPERATURE RANGE $T_A = T_J$	INPUT COMPATIBILITY	PACKAGED DEVICES(1)			
		SOIC-8 (D)(2)	PowerPAD™ SOIC-8 (DDA)(2)	SON-8 (DRM)(3)	SON-10 (DPR)(4)
-40°C to 140°C	Pseudo CMOS	UCC27210D	UCC27210DDA	UCC27210DRM	UCC27210DPR
	TTL	UCC27211D	UCC27211DDA	UCC27211DRM	UCC27211DPR

(1) These products are packaged in Lead (Pb)-Free and green lead finish of PdNiAu which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
(2) D (SOIC-8) and DDA (Power Pad™ SOIC-8) packages are available taped and reeled. Add R suffix to device type (e.g. UCC27210ADR/UCC27211ADR) to order quantities of 2,500 devices per reel.
(3) DRM (SON-8) package comes either in a small reel of 250 pieces as part number UCC27210ADRMT/UCC27211ADRMT, or larger reels of 3000 pieces as part number UCC27210ADRMR/UCC27211ADRMR.
(4) DPR (SON-10) package comes either in a small reel of 250 pieces as part number UCC27210ADPRT/UCC27211ADPRT, or large reels of 3000 pieces as part number UCC27210ADPRR/UCC27211ADPRR.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range, V_{DD}[(1)], V_{HB} - V_{HS}		-0.3	20	V
Input voltages on LI and HI, V_{LI}, V_{HI}		-10	20	
Output voltage on LO, V_{LO}	DC	-0.3	V_{DD} + 0.3	
	Repetitive pulse <100 ns[(2)]	-2	V_{DD} + 0.3	
Output voltage on HO, V_{HO}	DC	V_{HS} – 0.3	V_{HB} + 0.3	
	Repetitive pulse <100 ns[(2)]	V_{HS} - 2	V_{HB} + 0.3	
Voltage on HS, V_{HS}	DC	-1	115	
	Repetitive pulse <100 ns[(2)]	-18	115	
Voltage on HB, V_{HB}		-0.3	120	
ESD	Human Body Model (HBM)		2	kV
	Field Induced Charged Device Model (FICDM)		1	
Operating virtual junction temperature range, T_J		-40	150	°C
Storage temperature, T_{STG}		-65	150	
Lead temperature (soldering, 10 sec.)			300	

(1) All voltages are with respect to VSS unless otherwise noted. Currents are positive into, negative out of the specified terminal.
(2) Verified at bench characterization.

RECOMMENDED OPERATING CONDITIONS

all voltages are with respect to V_{SS}; currents are positive into and negative out of the specified terminal. –40°C < T_J = T_A < 140°C (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage range, V_{DD}, V_{HB}-V_{HS}	8	12	17	V
Voltage on HS, V_{HS}	-1		105	
Voltage on HS, V_{HS} (repetitive pulse <100 ns)	-15		110	
Voltage on HB, V_{HB}	V_{HS} +8, V_{DD} –1		V_{HS} +17, 115	
Voltage slew rate on HS			50	V/ns
Operating junction temperature range	-40		140	°C

THERMAL INFORMATION

THERMAL METRIC		UCC27210/11 (1)		UNITS
		D	DDA	
		8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance (2)	111.8	37.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (3)	56.9	47.2	
θ_{JB}	Junction-to-board thermal resistance (4)	53.0	9.6	
ψ_{JT}	Junction-to-top characterization parameter (5)	7.8	2.8	
ψ_{JB}	Junction-to-board characterization parameter (6)	52.3	9.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (7)	n/a	3.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

THERMAL INFORMATION

THERMAL METRIC		UCC27210/11 (1)		UNITS
		DRM	DPR	
		8 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance (2)	33.9	36.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (3)	33.2	36.0	
θ_{JB}	Junction-to-board thermal resistance (4)	11.4	14.0	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.4	0.3	
ψ_{JB}	Junction-to-board characterization parameter (6)	11.7	14.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (7)	2.3	3.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
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(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, no load on LO or HO, T_A = T_J = -40°C to 140°C, (unless otherwise noted)

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Currents							
I_{DD}	V_{DD} quiescent current		V(LI) = V(HI) = 0 V	0.05	0.085	0.17	mA
I_{DDO}	V_{DD} operating current	UCC27210	f = 500 kHz, C_{LOAD} = 0	2.4	2.6	4.3	mA
		UCC27211		2.4	2.5	4.3	mA
I_{HB}	Boot voltage quiescent current		V(LI) = V(HI) = 0 V	0.015	0.065	0.1	mA
I_{HBO}	Boot voltage operating current		f = 500 kHz, C_{LOAD} = 0	1.5	2.5	4	mA
I_{HBS}	HB to V_{SS} quiescent current		V(HS) = V(HB) = 115 V		0.0005	0.13	µA
I_{HBSO}	HB to V_{SS} operating current		f = 500 kHz, C_{LOAD} = 0		0.07	0.9	mA
Input							
V_{HIT}	Input voltage threshold		UCC27210	4.2	5.0	5.8	V
V_{LIT}	Input voltage threshold			2.4	3.2	4.0	V
V_{IHYS}	Input voltage hysteresis				1.8		V
R_{IN}	Input pulldown resistance				102		kΩ
V_{HIT}	Input voltage threshold		UCC27211	1.9	2.3	2.7	V
V_{LIT}	Input voltage threshold			1.3	1.6	1.9	V
V_{IHYS}	Input voltage hysteresis				700		mV
R_{IN}	Input pulldown resistance				68		kΩ
Under-Voltage Lockout (UVLO)							
V_{DDR}	V_{DD} turn-on threshold			6.2	7.0	7.8	V
V_{DDHYS}	Hysteresis				0.5		V
V_{HBR}	V_{HB} turn-on threshold			5.6	6.7	7.9	V
V_{HBHYS}	Hysteresis				1.1		V
Bootstrap Diode							
V_F	Low-current forward voltage		I_{VDD-HB} = 100 µA		0.65	0.8	V
V_{FI}	High-current forward voltage		I_{VDD-HB} = 100 mA		0.85	0.95	V
R_D	Dynamic resistance, ΔVF/ΔI		I_{VDD-HB} = 100 mA and 80 mA	0.3	0.5	0.85	Ω
LO Gate Driver							
V_{LOL}	Low-level output voltage		I_{LO} = 100 mA	0.05	0.09	0.15	V
V_{LOH}	High level output voltage		I_{LO} = -100 mA, V_{LOH} = V_{DD} - V_{LO}	0.1	0.16	0.27	V
	Peak pull-up current (1)		V_{LO} = 0 V		3.7		A
	Peak pull-down current (1)		V_{LO} = 12 V		4.5		A
HO GATE Driver							
V_{HOL}	Low-level output voltage		I_{HO} = 100 mA	0.05	0.09	0.15	V
V_{HOH}	High-level output voltage		I_{HO} = -100 mA, V_{HOH} = V_{HB} - V_{HO}	0.1	0.16	0.27	V
	Peak pull-up current (1)		V_{HO} = 0 V		3.7		A
	Peak pull-down current (1)		V_{HO} = 12 V		4.5		A

(1) Ensured by design.

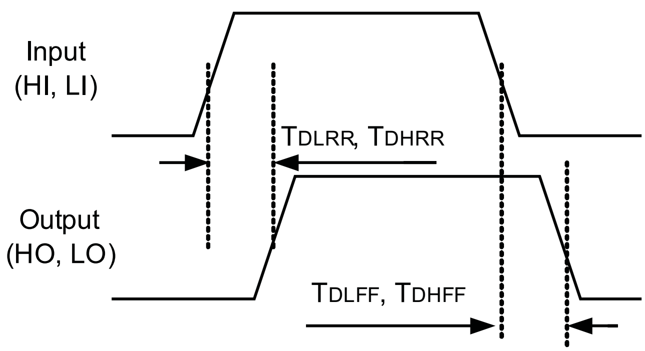
ELECTRICAL CHARACTERISTICS (continued)

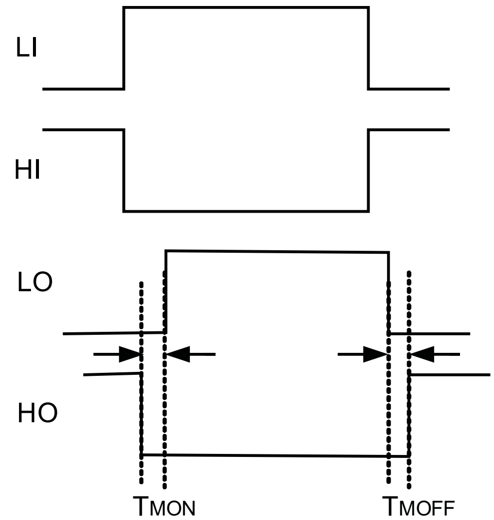
$V_{DD} = V_{HB}$ = 12 V, $V_{HS} = V_{SS}$ = 0 V, no load on LO or HO, $T_A = T_J$ = -40°C to 140°C, (unless otherwise noted)

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNITS
Switching Parameters: Propagation Delays							
T_{DLFF}	V_{LI} falling to V_{LO} falling		UCC27210, C_{LOAD} = 0	17	21	37	ns
T_{DHFF}	V_{HI} falling to V_{HO} falling			17	21	37	
T_{DLRR}	V_{LI} rising to V_{LO} rising			18	24	46	
T_{DHRR}	V_{HI} rising to V_{HO} rising			18	24	46	
T_{DLFF}	V_{LI} falling to V_{LO} falling		UCC27211, C_{LOAD} = 0	10	17	30	
T_{DHFF}	V_{HI} falling to V_{HO} falling			10	17	30	
T_{DLRR}	V_{LI} rising to V_{LO} rising			10	18	40	
T_{DHRR}	V_{HI} rising to V_{HO} rising			10	18	40	
Switching Parameters: Delay Matching							
T_{MON}	From HO OFF to LO ON	UCC27210	T_J = 25°C		3	11	ns
			T_J = –40°C to 140°C		3	14	
T_{MOFF}	From LO OFF to HO ON		T_J = 25°C		3	11	ns
			T_J = –40°C to 140°C		3	14	
T_{MON}	From HO OFF to LO ON	UCC27211	T_J = 25°C		2	9.5	ns
			T_J = –40°C to 140°C		2	14	
T_{MOFF}	From LO OFF to HO ON		T_J = 25°C		2	9.5	ns
			T_J = –40°C to 140°C		2	14	
Switching Parameters: Output Rise and Fall Time							
t_R	LO rise time		C_{LOAD} = 1000 pF, from 10% to 90%		7.2		ns
t_R	HO rise time				7.2		
t_F	LO fall time		C_{LOAD} = 1000 pF, from 90% to 10%		5.5		
t_F	HO fall time				5.5		
t_R	LO, HO		C_{LOAD} = 0.1 μF, (3 V to 9 V)		0.36	0.6	μs
t_F	LO, HO		C_{LOAD} = 0.1 μF, (9 V to 3 V)		0.15	0.4	
Switching Parameters: Miscellaneous							
	Minimum input pulse width that changes the output					50	ns
	Bootstrap diode turn-off time (2)(3)		I_F = 20 mA, I_{REV} = 0.5 A (4)		20		

(2) Ensured by design.
(3) I_F: Forward current applied to bootstrap diode, I_{REV}: Reverse current applied to bootstrap diode.
(4) Typical values for T_A = 25°C.

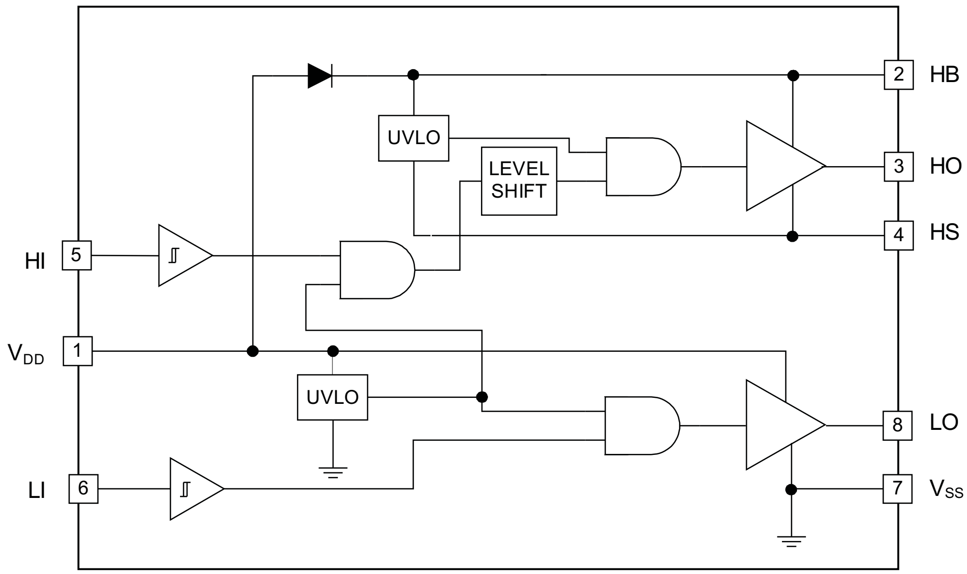
Timing Diagrams

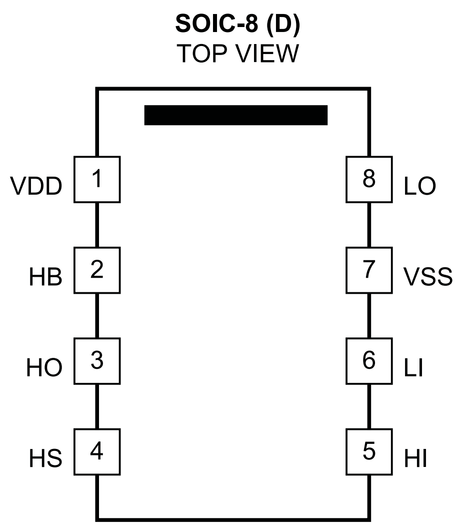


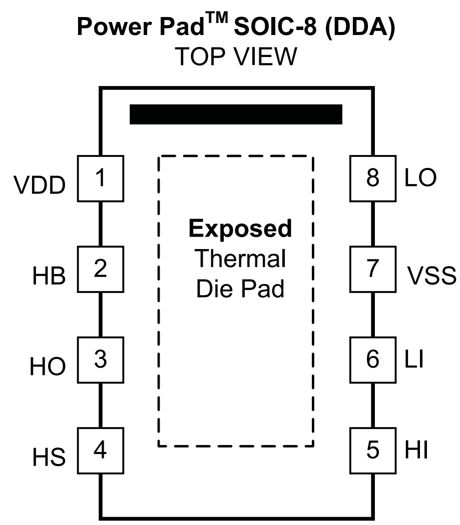


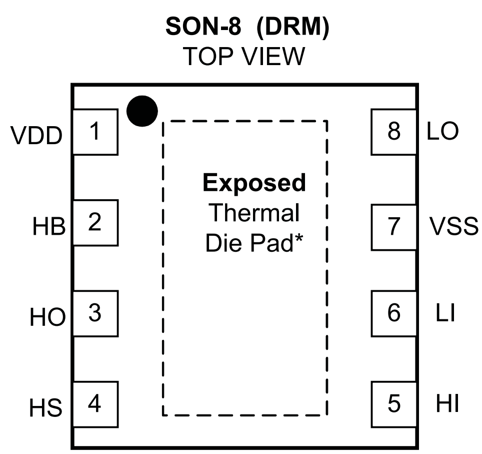
DEVICE INFORMATION

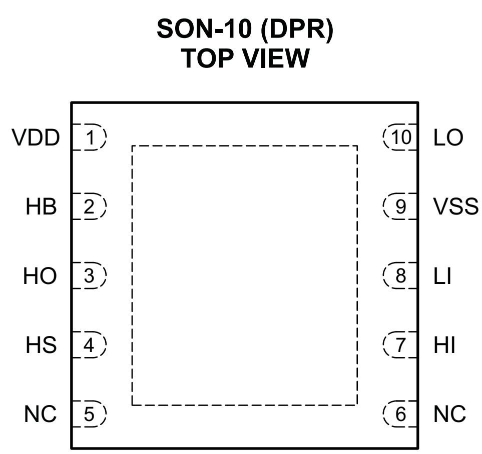
Functional Block Diagram











TERMINAL FUNCTIONS

PIN NAME	PIN		DESCRIPTION
	D/DDA/DRM	DPR	
VDD	1	1	Positive supply to the lower-gate driver. De-couple this pin to V_{SS} (GND). Typical decoupling capacitor range is 0.22 µF to 1.0 µF.
HB	2	2	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF. The capacitor value is dependant on the gate charge of the high-side MOSFET and should also be selected based on speed and ripple criteria
HO	3	3	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	4	High-side source connection. Connect to source of high-side power MOSFET. Connect the negative side of bootstrap capacitor to this pin.
HI	5	7	High-side input.
LI	6	8	Low-side input.
VSS	7	9	Negative supply terminal for the device which is generally grounded.
LO	8	10	Low-side output. Connect to the gate of the low-side power MOSFET.
N/C	-	5/6	Not Connected.
PowerPAD™ (1)	Pad	Pad	Utilized on the DDA, DRM and DPR packages only. Electrically referenced to V_{SS} (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

(1) The PowerPAD™ is not directly connected to any leads of the package. However it is electrically and thermally connected to the substrate which is the ground of the device.

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT vs SUPPLY VOLTAGE

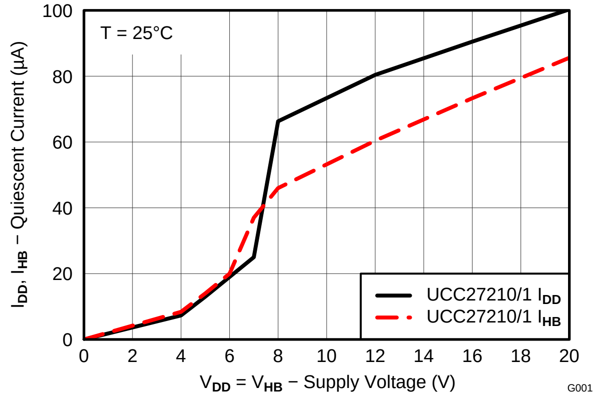


Figure 1.

UCC27210 IDD OPERATING CURRENT vs FREQUENCY

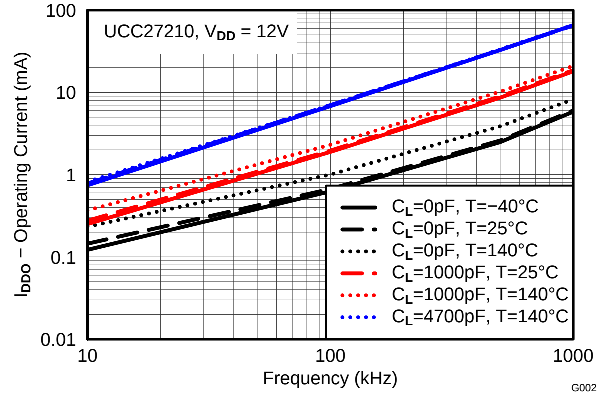


Figure 2.

UCC27211 IDD OPERATING CURRENT vs FREQUENCY

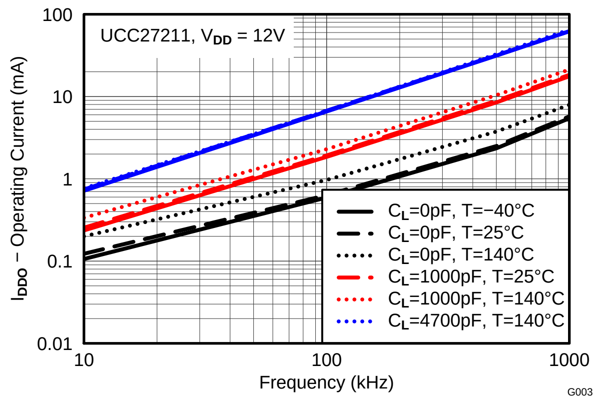


Figure 3.

BOOT VOLTAGE OPERATING CURRENT vs FREQUENCY (HB to HS)

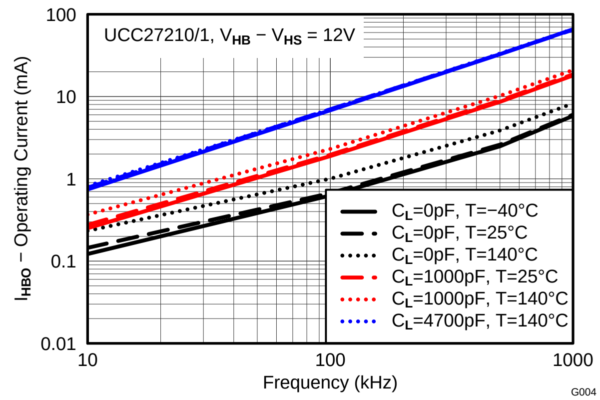


Figure 4.

UCC27210/11 INPUT THRESHOLD vs SUPPLY VOLTAGE

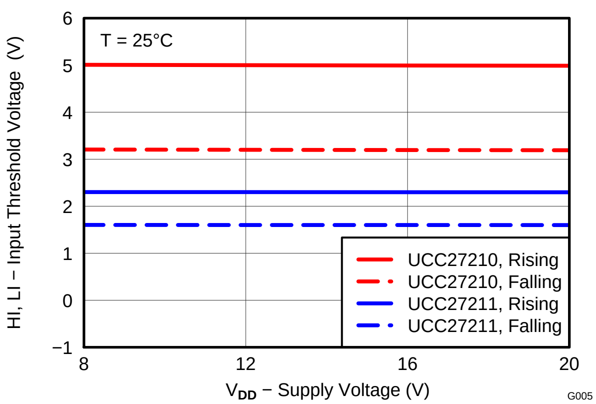


Figure 5.

UCC27210/11 INPUT THRESHOLDS vs TEMPERATURE

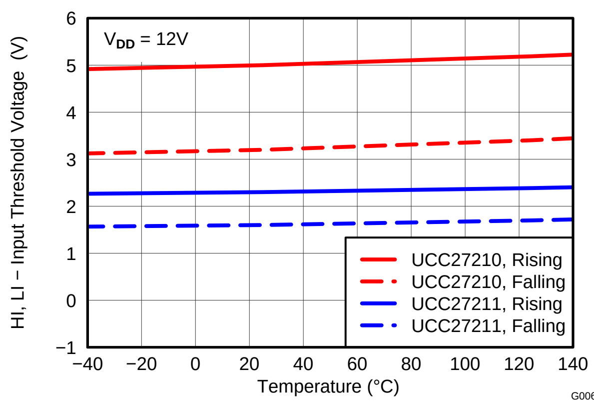


Figure 6.

TYPICAL CHARACTERISTICS (continued)

LO AND HO HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

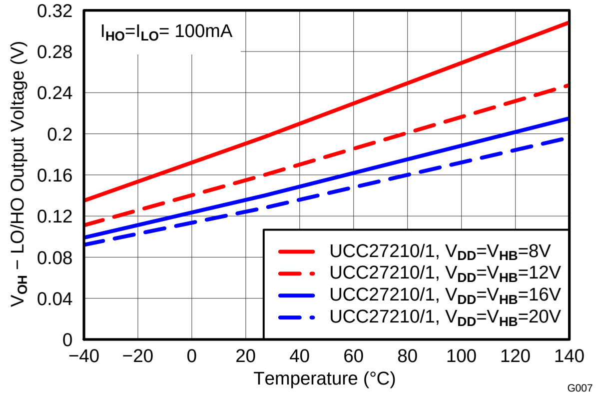


Figure 7.

LO AND HO LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

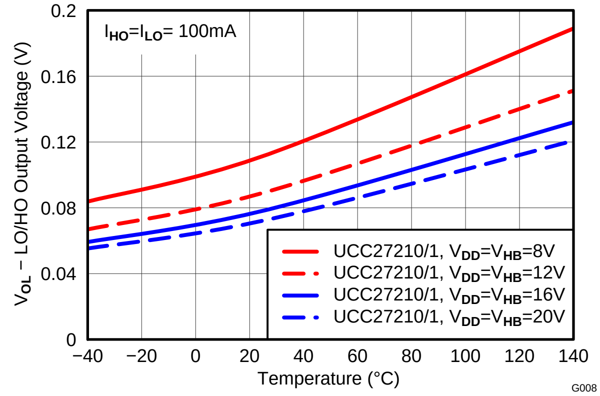


Figure 8.

UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

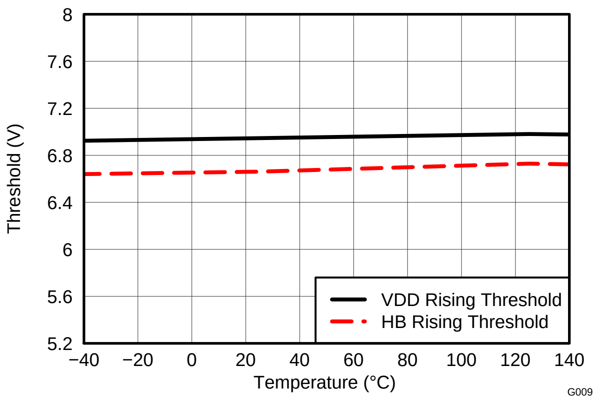


Figure 9.

UNDERVOLTAGE LOCKOUT THRESHOLD HYSTERESIS vs TEMPERATURE

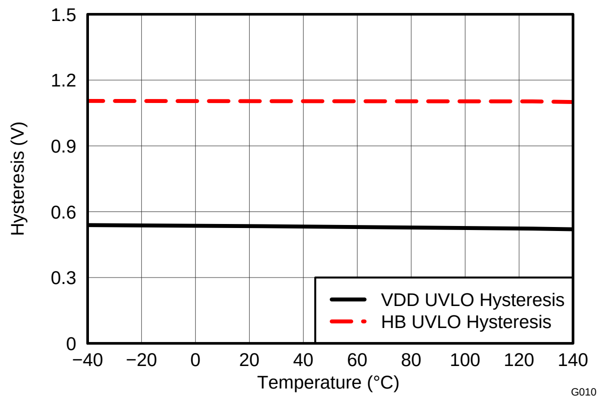


Figure 10.

UCC27210 PROPAGATION DELAYS vs TEMPERATURE

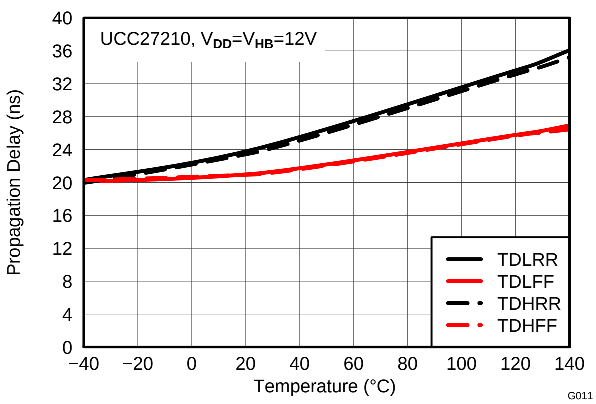


Figure 11.

UCC27211 PROPAGATION DELAYS vs TEMPERATURE

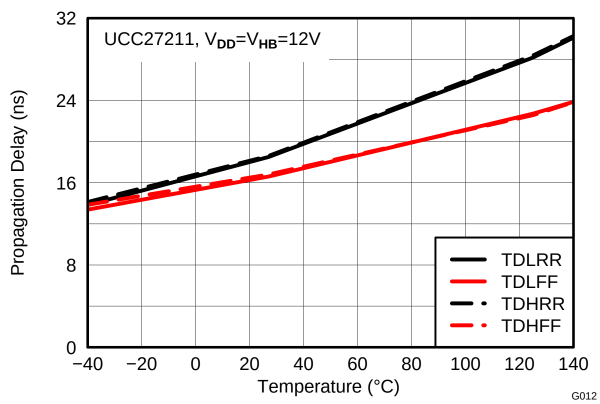


Figure 12.

TYPICAL CHARACTERISTICS (continued)

UCC27210 PROPAGATION DELAYS vs SUPPLY VOLTAGE

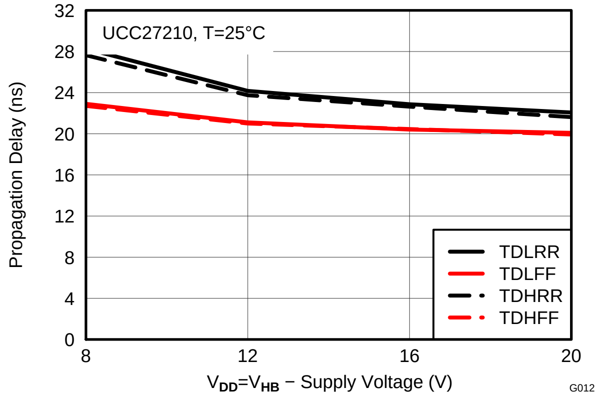


Figure 13.

UCC27211 PROPAGATION DELAYS vs SUPPLY VOLTAGE

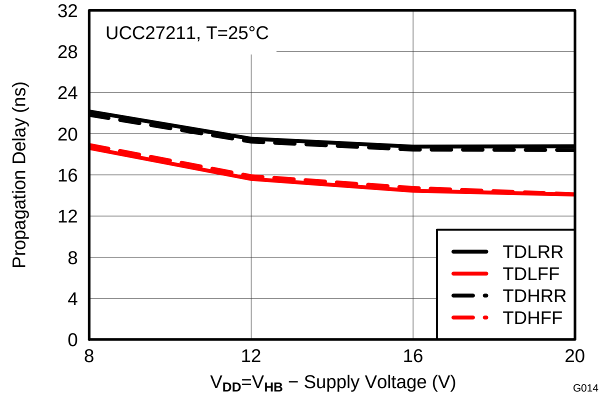


Figure 14.

DELAY MATCHING vs TEMPERATURE

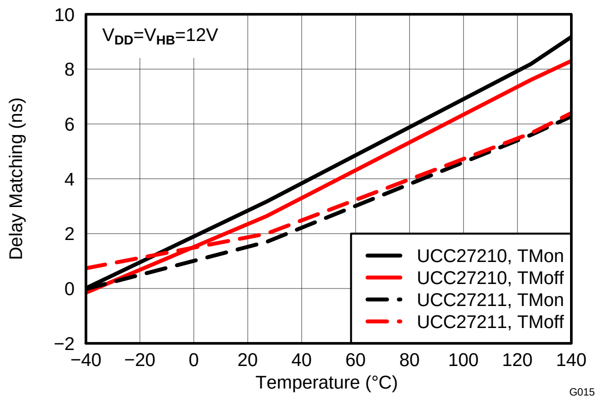


Figure 15.

OUTPUT CURRENT vs OUTPUT VOLTAGE

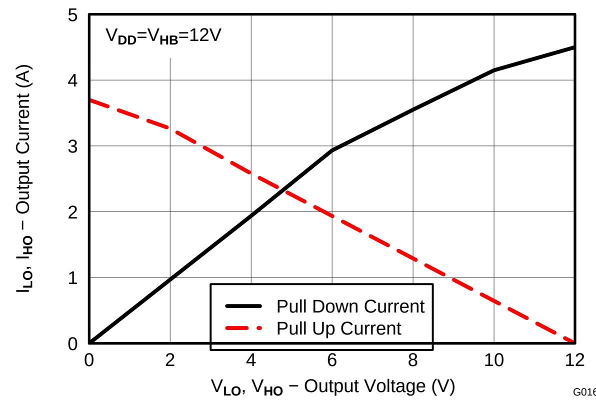


Figure 16.

TYPICAL CHARACTERISTICS (continued)

DIODE CURRENT vs DIODE VOLTAGE

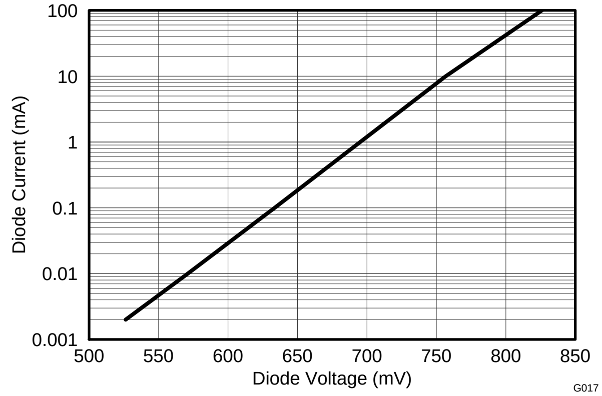


Figure 17.

NEGATIVE 10-V INPUT

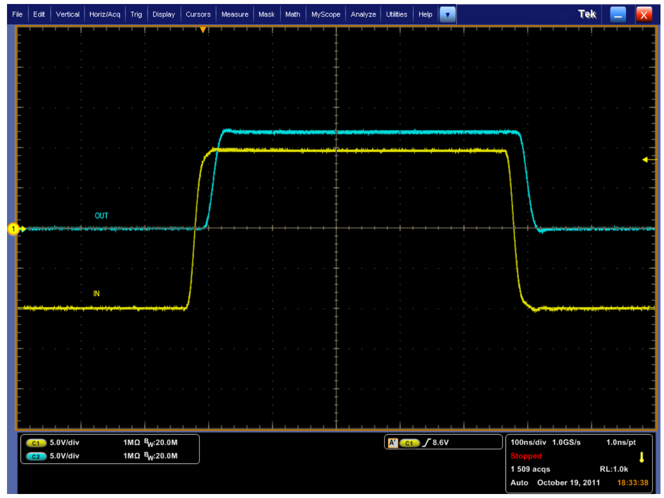


Figure 18.

STEP INPUT

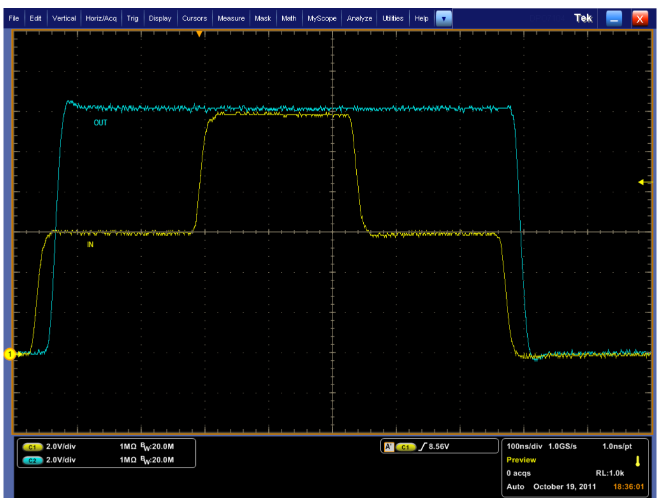


Figure 19.

SYMMETRICAL UVLO

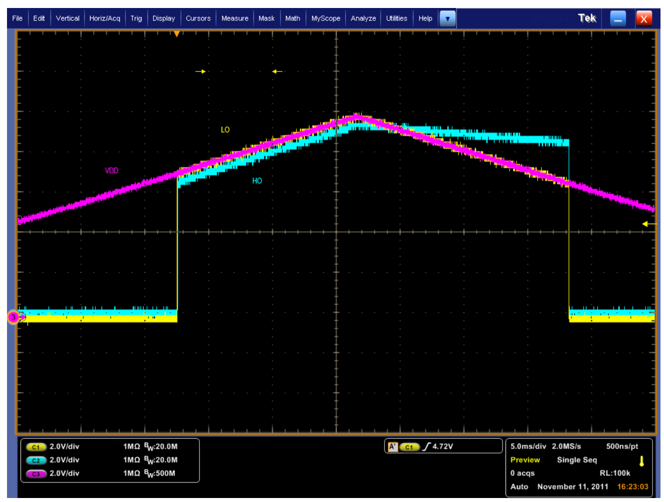


Figure 20.

APPLICATION INFORMATION

Functional Description

The UCC27210/11 represent Texas Instruments' latest generation of high voltage gate drivers which are designed to drive both the high-side and low-side of N-Channel MOSFETs in a half-/full-bridge or synchronous buck configuration. The floating high-side driver is capable of operating with supply voltages of up to 120 V. This allows for N-Channel MOSFET control in half-bridge, full-bridge, push pull, two-switch forward and active clamp forward converters.

The UCC27210/11 feature 4-A source/sink capability, industry best-in-class switching characteristics and a host of other features listed in the table below. These features combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

Table 1. UCC27210/11 Highlights

FEATURE	BENEFIT
4-A source and sink current with 0.9-Ω output resistance	High peak current ideal for driving large power MOSFETs with minimal power loss (fast-drive capability at Miller plateau)
Input pins (HI and LI) can directly handle -10 VDC up to 20 VDC	Increased robustness and ability to handle under/overshoot. Can interface directly to gate-drive transformers without having to use rectification diodes
120-V internal boot diode	Provides voltage margin to meet telecom 100-V surge requirements
Switch node (HS pin) able to handle -18 V maximum for 100 ns	Allows the high-side channel to have extra protection from inherent negative voltages caused parasitic inductance and stray capacitance.
Robust ESD circuitry to handle voltage spikes	Excellent immunity to large dV/dT conditions
18-ns propagation delay with 7.2-ns / 5.5-ns rise/fall Times	Best-in-class switching characteristics and extremely low-pulse transmission distortion
2-ns (typ) delay matching between channels	Avoids transformer volt-second offset in bridge
Symmetrical UVLO circuit	Ensures high-side and low-side shut down at the same time
CMOS optimized threshold or TTL optimized thresholds with increased hysteresis	Complementary to analog or digital PWM controllers. Increased hysteresis offers added noise immunity

In UCC27210/11, the high side and low side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27210 and UCC27211. The UCC27210 is the Pseudo-CMOS compatible input version and the UCC27211 is the TTL or logic compatible version. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V_{SS} which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

Input Stages

The input stages provide the interface to the PWM output signals. The input impedance of the UCC27210 is 100 kΩ nominal and input capacitance is approximately 2 pF. The 100 kΩ is a pull-down resistance to V_{SS} (ground). The UCC27210 Pseudo-CMOS input structure has been designed to provide large hysteresis and at the same time to allows interfacing to a multitude of analog or digital PWM controllers. In some CMOS designs, the input thresholds are determined as a percentage of VDD. By doing so, the high-level input threshold can become unreasonably high and unusable. The UCC27210 recognizes the fact that VDD levels are trending downward and it therefore provides a rising threshold with 5.0 V (typ) and falling threshold with 3.2 V (typ). The input hysteresis of the UCC27210 is 1.8 V (typ).

The input stages of the UCC27211 have impedance of 70 kΩ nominal and input capacitance is approximately 2 pF. Pull-down resistance to V_{SS} (ground) is 70 kΩ. The logic level compatible input provides a rising threshold of 2.3 V and a falling threshold of 1.6 V.

Under Voltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection. V_{DD} as well as V_{HB} to V_{HS} differential voltages are monitored. The V_{DD} UVLO disables both drivers when V_{DD} is below the specified threshold. The rising V_{DD} threshold is 7.0 V with 0.5-V hysteresis. The VHB UVLO disables only the high-side driver when the V_{HB} to V_{HS} differential voltage is below the specified threshold. The V_{HB} UVLO rising threshold is 6.7 V with 1.1-V hysteresis.

Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27210/11 family of drivers. The diode anode is connected to V_{DD} and cathode connected to V_{HB}. With the V_{HB} capacitor connected to HB and the HS pins, the V_{HB} capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from V_{DD} to V_{SS} and the high side is referenced from V_{HB} to V_{HS}.

Layout Recommendations

To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and V_{HB} (bootstrap) capacitors as close as possible to the driver.
- Pay close attention to the GND trace. Use the thermal pad of the DDA and DRM package as GND by connecting it to the VSS pin (GND). The GND trace from the driver goes directly to the source of the MOSFET but should not be in the high current path of the MOSFET(S) drain or source current.
- Use similar rules for the HS node as for GND for the high-side driver.
- Use wide traces for LO and HO closely following the associated GND or HS traces. 60 to 100-mils width is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node needs to be routed from one layer to another. For GND the number of vias needs to be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid LI and HI (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.

Keep in mind that a poor layout can cause a significant drop in efficiency versus a good PCB layout and can even lead to decreased reliability of the whole system.

Example Component Placement

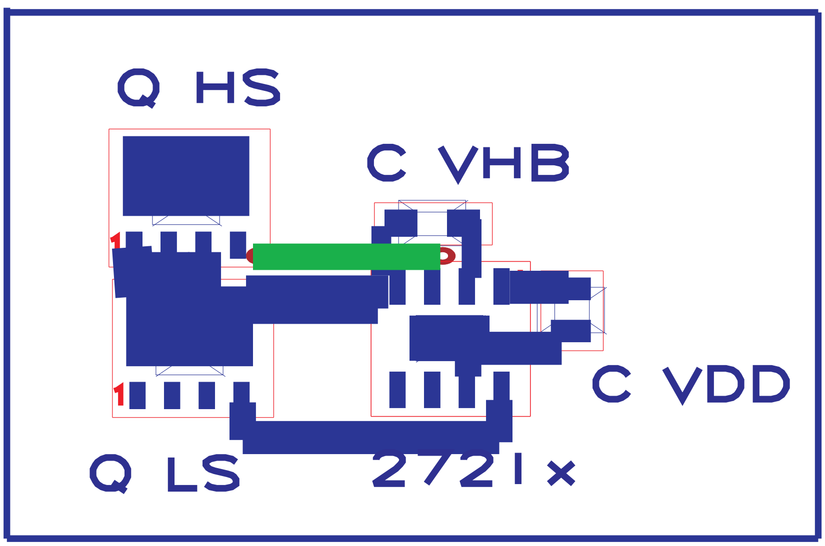


Figure 21. UCC27210/11 Component Placement

Additional References

These references and links to additional information may be found at www.ti.com

- Additional layout guidelines for PCB land patterns may be found in, *QFN/SON PCB Attachment*, Application Brief (Texas Instrument's Literature Number SLUA271)
- Additional thermal performance guidelines may be found in, *PowerPAD™ Thermally Enhanced Package Application Report*, Application Report (Texas Instrument's Literature Number SLMA002A)
- Additional thermal performance guidelines may be found in, *PowerPAD™ Made Easy*, Application Report (Texas Instrument's Literature Number SLMA004)

REVISION HISTORY

Changes from Revision A (November, 2011) to Revision B	Page
• Changed ordering information notes to reflect corrected part number. ...	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC27210D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27210DDA	PREVIEW	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
UCC27210DDAR	PREVIEW	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
UCC27210DPRR	ACTIVE	WSON	DPR	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC27210DPRT	ACTIVE	WSON	DPR	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC27210DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27210DRMR	ACTIVE	VSON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27210DRMT	ACTIVE	VSON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27211D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27211DDA	PREVIEW	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
UCC27211DDAR	PREVIEW	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
UCC27211DPRR	ACTIVE	WSON	DPR	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC27211DPRT	ACTIVE	WSON	DPR	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC27211DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27211DRMR	ACTIVE	VSON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27211DRMT	ACTIVE	VSON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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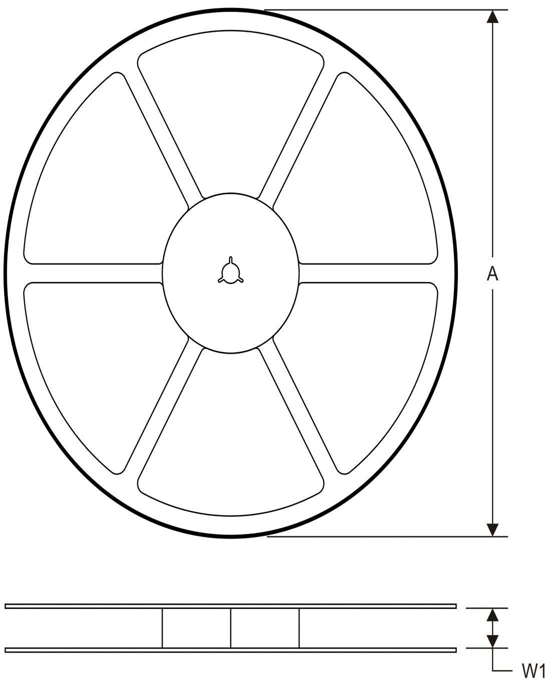
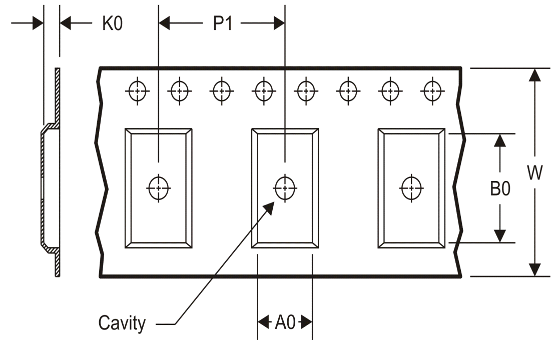
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



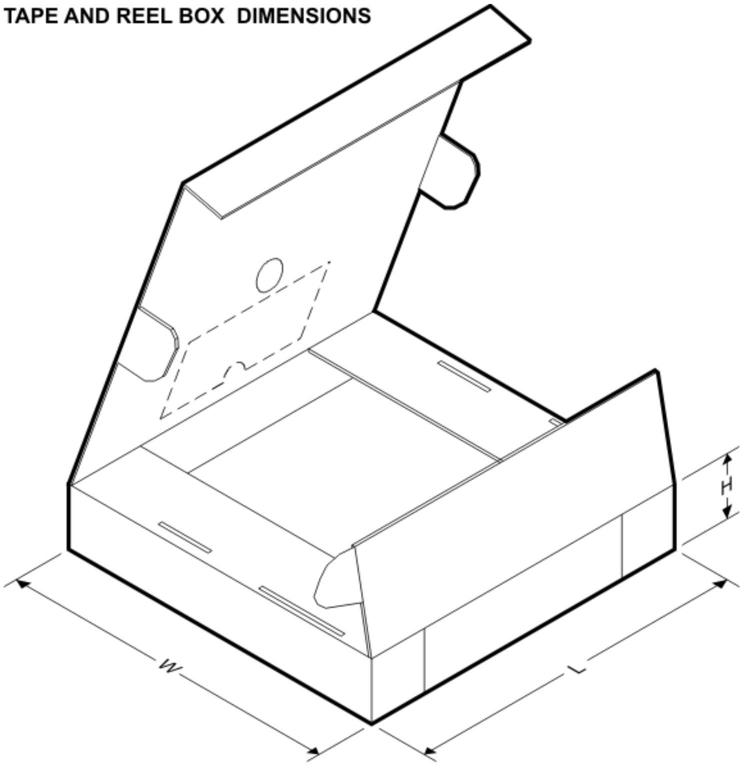
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27210DPRR	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27210DPRT	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27210DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27210DRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27211DPRR	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27211DPRT	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27211DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27211DRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27211DRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

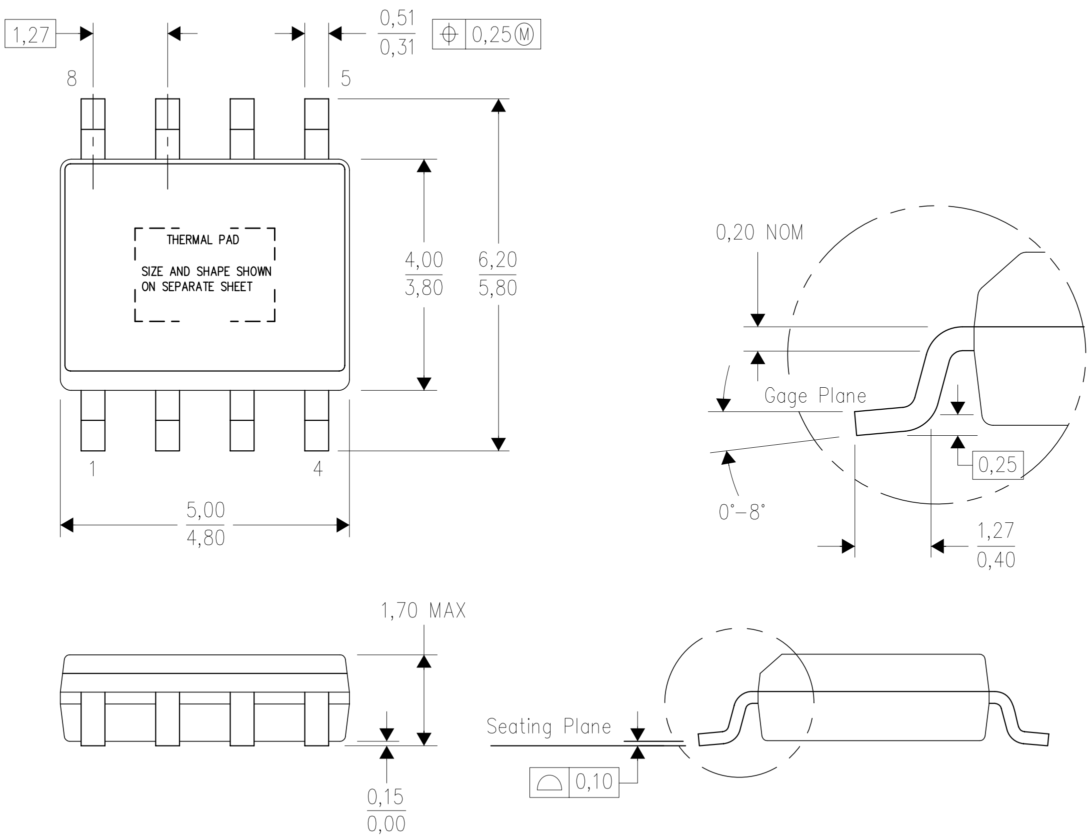
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27210DPRR	WSON	DPR	10	3000	346.0	346.0	29.0
UCC27210DPRT	WSON	DPR	10	250	210.0	185.0	35.0
UCC27210DR	SOIC	D	8	2500	346.0	346.0	29.0
UCC27210DRMR	VSON	DRM	8	3000	346.0	346.0	29.0
UCC27211DPRR	WSON	DPR	10	3000	346.0	346.0	29.0
UCC27211DPRT	WSON	DPR	10	250	210.0	185.0	35.0
UCC27211DR	SOIC	D	8	2500	346.0	346.0	29.0
UCC27211DRMR	VSON	DRM	8	3000	346.0	346.0	29.0
UCC27211DRMT	VSON	DRM	8	250	210.0	185.0	35.0

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. This package complies to JEDEC MS-012 variation BA

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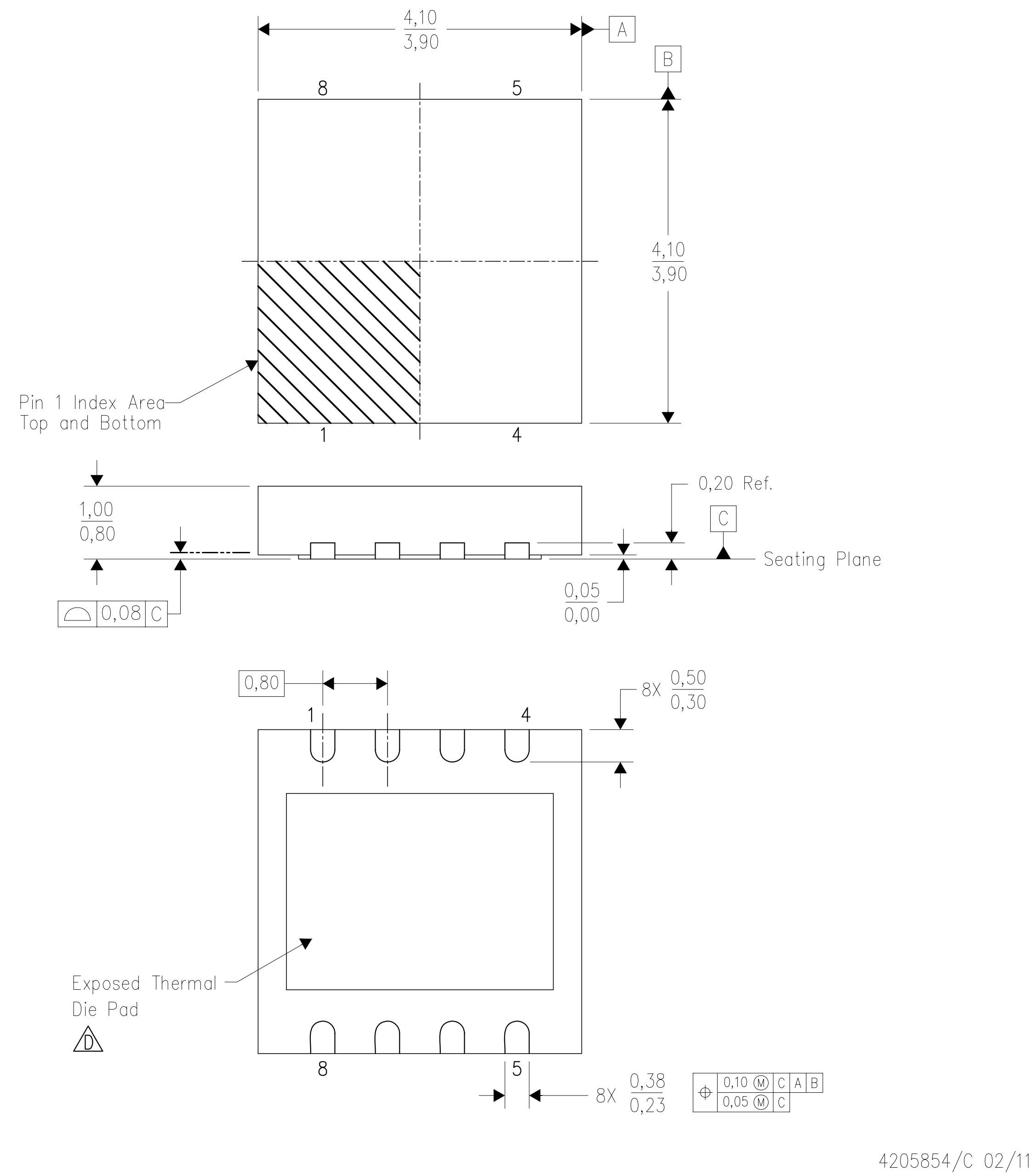
DRM (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



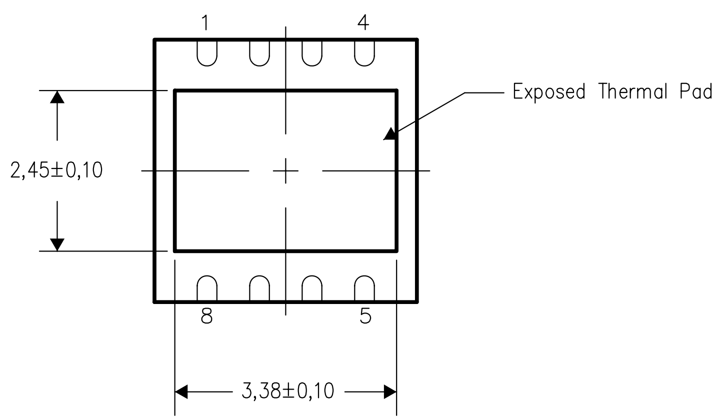
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

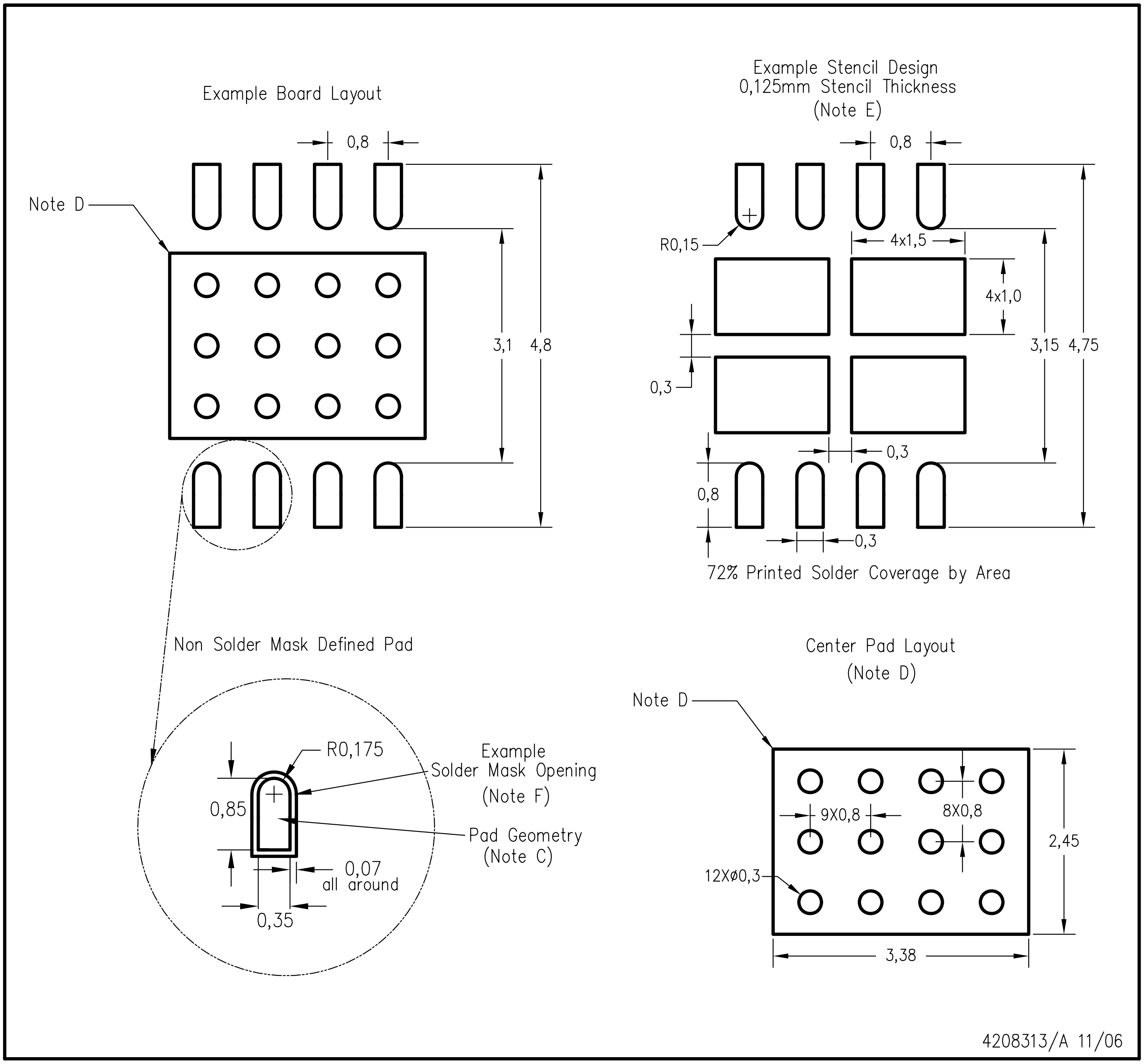


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

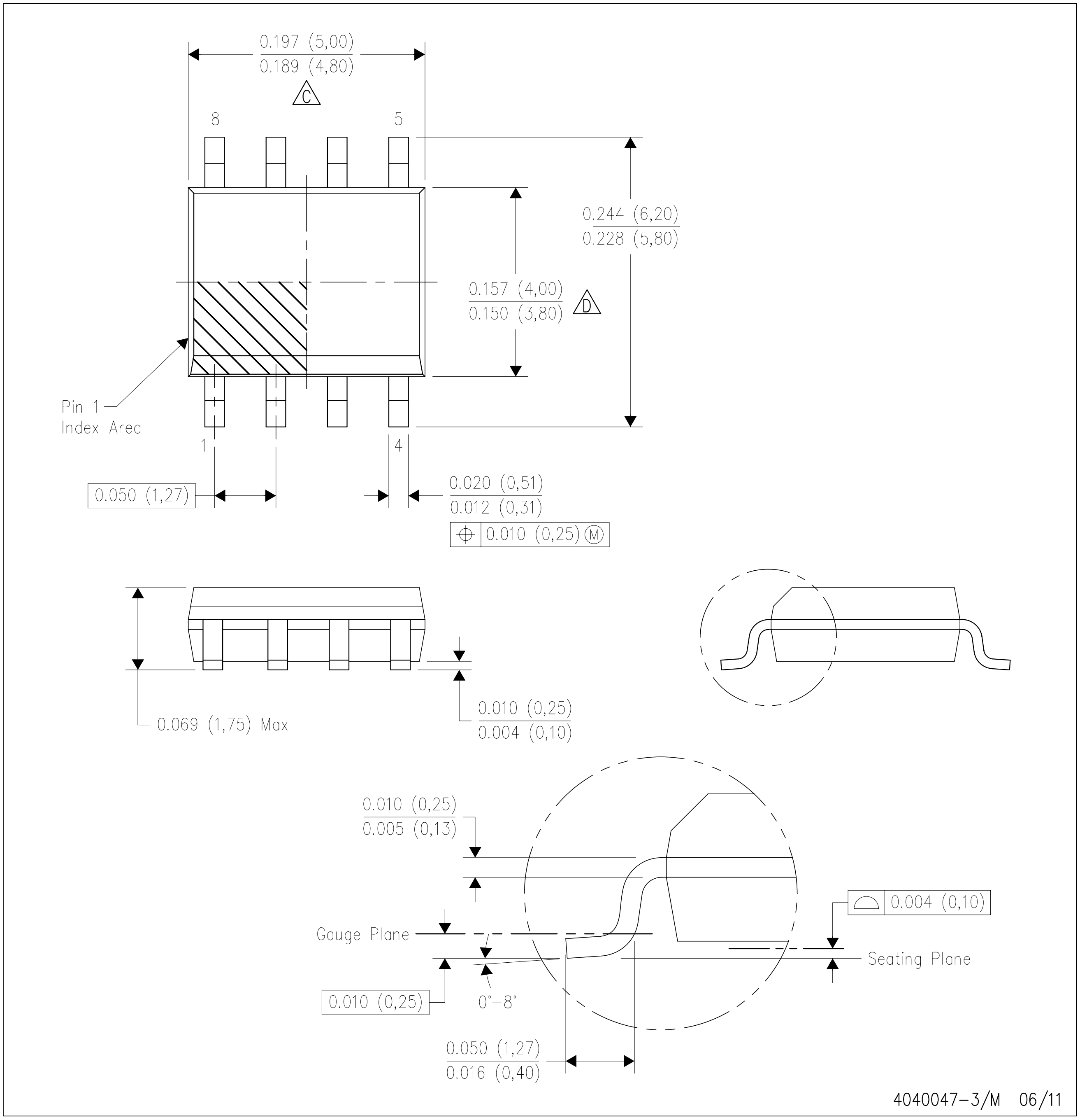
DRM (S-PDSO-N8)



NOTES:

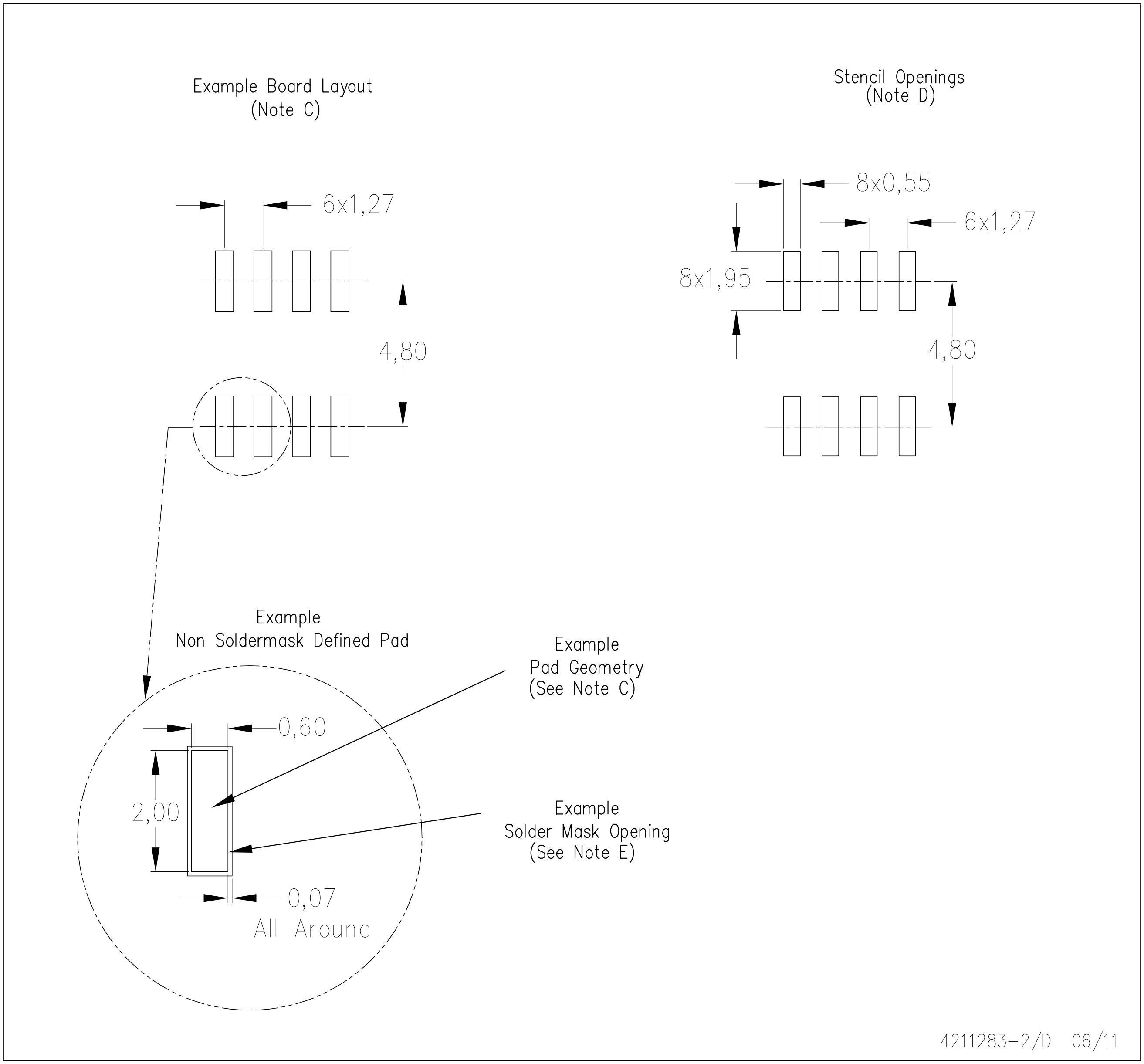
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
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