

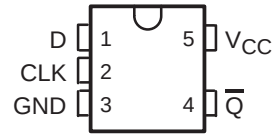
SN74AUC1G80

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

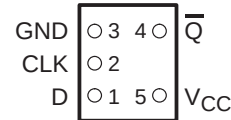
SCES388H – MARCH 2002 – REVISED FEBRUARY 2004

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub 1-V Operable
- Max t_{pd} of 1.9 ns at 1.8 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DBV OR DCK PACKAGE
(TOP VIEW)



YEA OR YZA PACKAGE
(BOTTOM VIEW)



description/ordering information

This single positive-edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the $\overline{Q}$ output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ WCSP (DSBGA) – YEA	Tape and reel	SN74AUC1G80YEAR	___UX_
	NanoFree™ WCSP (DSBGA) – YZA (Pb-free)	Tape and reel	SN74AUC1G80YZAR	
	SOT (SOT-23) – DBV	Tape and reel	SN74AUC1G80DBVR	U80_
	SOT (SC-70) – DCK	Tape and reel	SN74AUC1G80DCKR	UX_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEA/YZA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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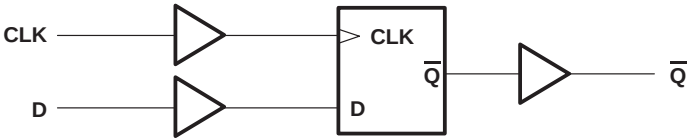
SN74AUC1G80 SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

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FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	$\overline{Q}$
↑	H	L
↑	L	H
L	X	$\overline{Q_0}$

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 3.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 3.6 V
Output voltage range, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Continuous output current, I_O	±20 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	252°C/W
YEA/YZA package	154°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}		V
		V _{CC} = 1.1 V to 1.95 V	0.65×V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	1.7		
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0		V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	0.7		
V _I	Input voltage		0	3.6	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	−0.7		mA
		V _{CC} = 1.1 V	−3		
		V _{CC} = 1.4 V	−5		
		V _{CC} = 1.65 V	−8		
		V _{CC} = 2.3 V	−9		
I _{OL}	Low-level output current	V _{CC} = 0.8 V	0.7		mA
		V _{CC} = 1.1 V	3		
		V _{CC} = 1.4 V	5		
		V _{CC} = 1.65 V	8		
		V _{CC} = 2.3 V	9		
Δt/Δv	Input transition rise or fall rate		20		ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	0.8 V to 2.7 V	V _{CC} -0.1			V
		I _{OH} = -0.7 mA	0.8 V	0.55			
		I _{OH} = -3 mA	1.1 V	0.8			
		I _{OH} = -5 mA	1.4 V	1			
		I _{OH} = -8 mA	1.65 V	1.2			
		I _{OH} = -9 mA	2.3 V	1.8			
V _{OL}		I _{OL} = 100 μA	0.8 V to 2.7 V	0.2			V
		I _{OL} = 0.7 mA	0.8 V	0.25			
		I _{OL} = 3 mA	1.1 V	0.3			
		I _{OL} = 5 mA	1.4 V	0.4			
		I _{OL} = 8 mA	1.65 V	0.45			
		I _{OL} = 9 mA	2.3 V	0.6			
I _I	D or CLK input	V _I = V _{CC} or GND	0 to 2.7 V	±5		μA	
I _{off}		V _I or V _O = 2.7 V	0	±10		μA	
I _{CC}		V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V	10		μA	
C _i		V _I = V _{CC} or GND	2.5 V	2.5		pF	

[†] All typical values are at T_A = 25°C.



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SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		UNIT
		TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	50	200		225		250		275		MHz
t _w	Pulse duration, CLK high or low	4.6	1.7		1.7		1.7		1.7		ns
t _{su}	Setup time before CLK↑, Data high or low	1.6	1.1		0.8		0.6		0.5		ns
t _h	Hold time, data after CLK↑	0	0		0.1		0.1		0.1		ns

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f _{max}			50	200		225		250			275		MHz
t _{pd}	CLK	$\overline{Q}$	5	1	3.9	0.8	2.5	0.3	1	1.9	0.3	1.3	ns

switching characteristics over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f _{max}			250			275		ns
t _{pd}	CLK	$\overline{Q}$	0.8	1.5	2.4	0.6	1.8	ns

operating characteristics, T_A = 25°C

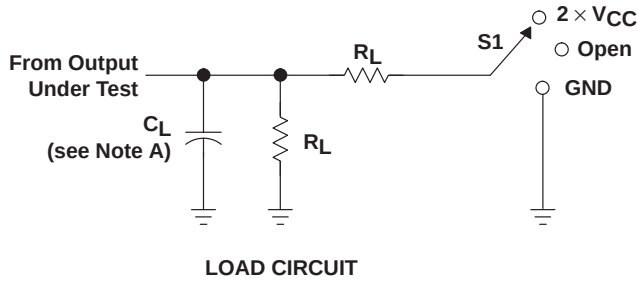
PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT
		TYP	TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance f = 10 MHz	18	18	18	18.5	20.5	pF

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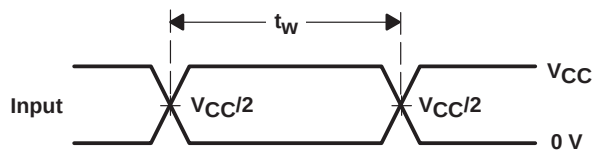
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PARAMETER MEASUREMENT INFORMATION

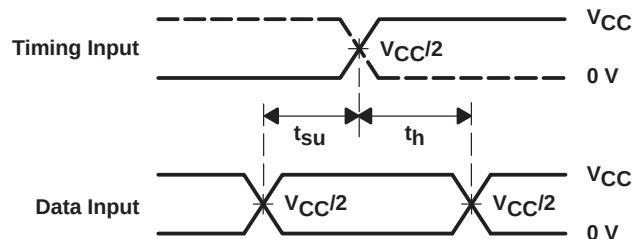


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

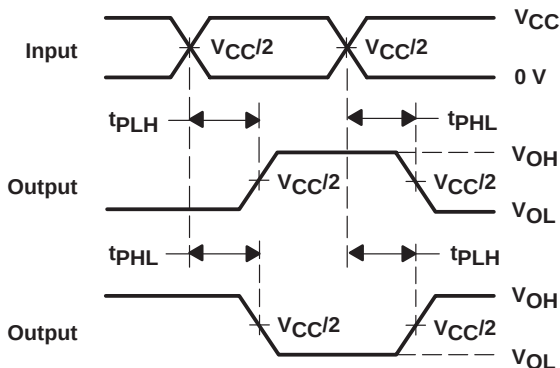
V_{CC}	C_L	R_L	V_{Δ}
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k Ω	0.15 V
1.8 V $\pm$ 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



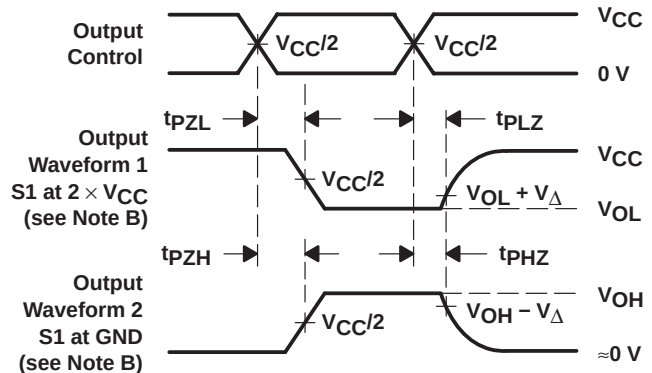
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

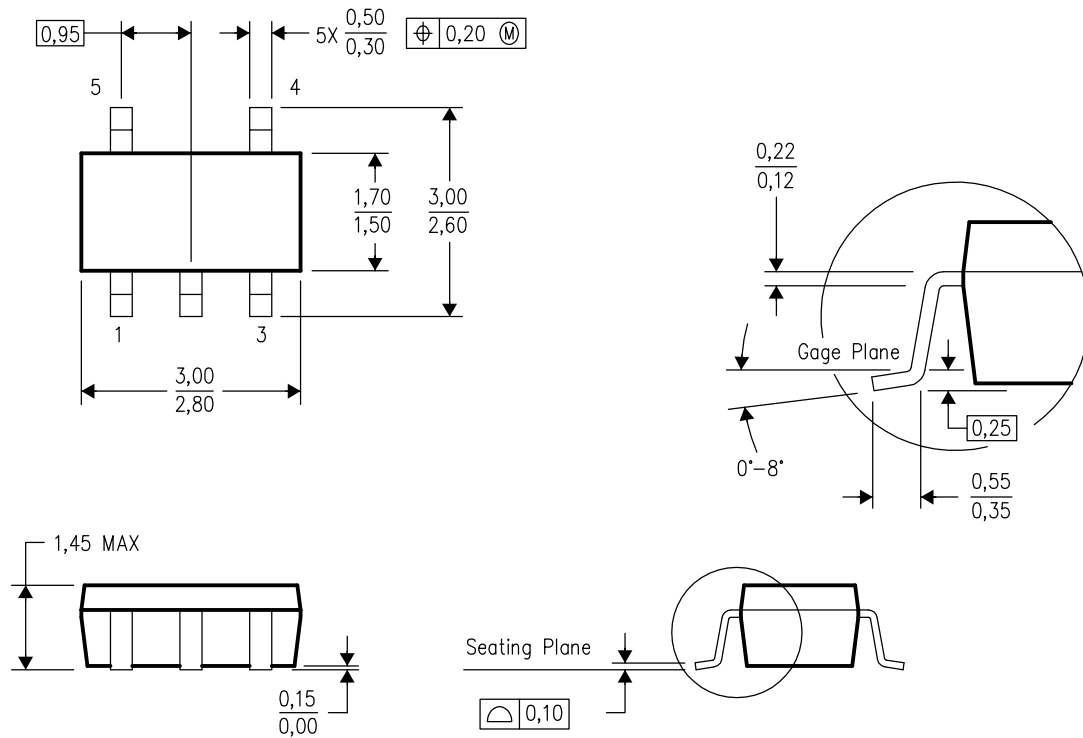
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$, slew rate $\geq$ 1 V/ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

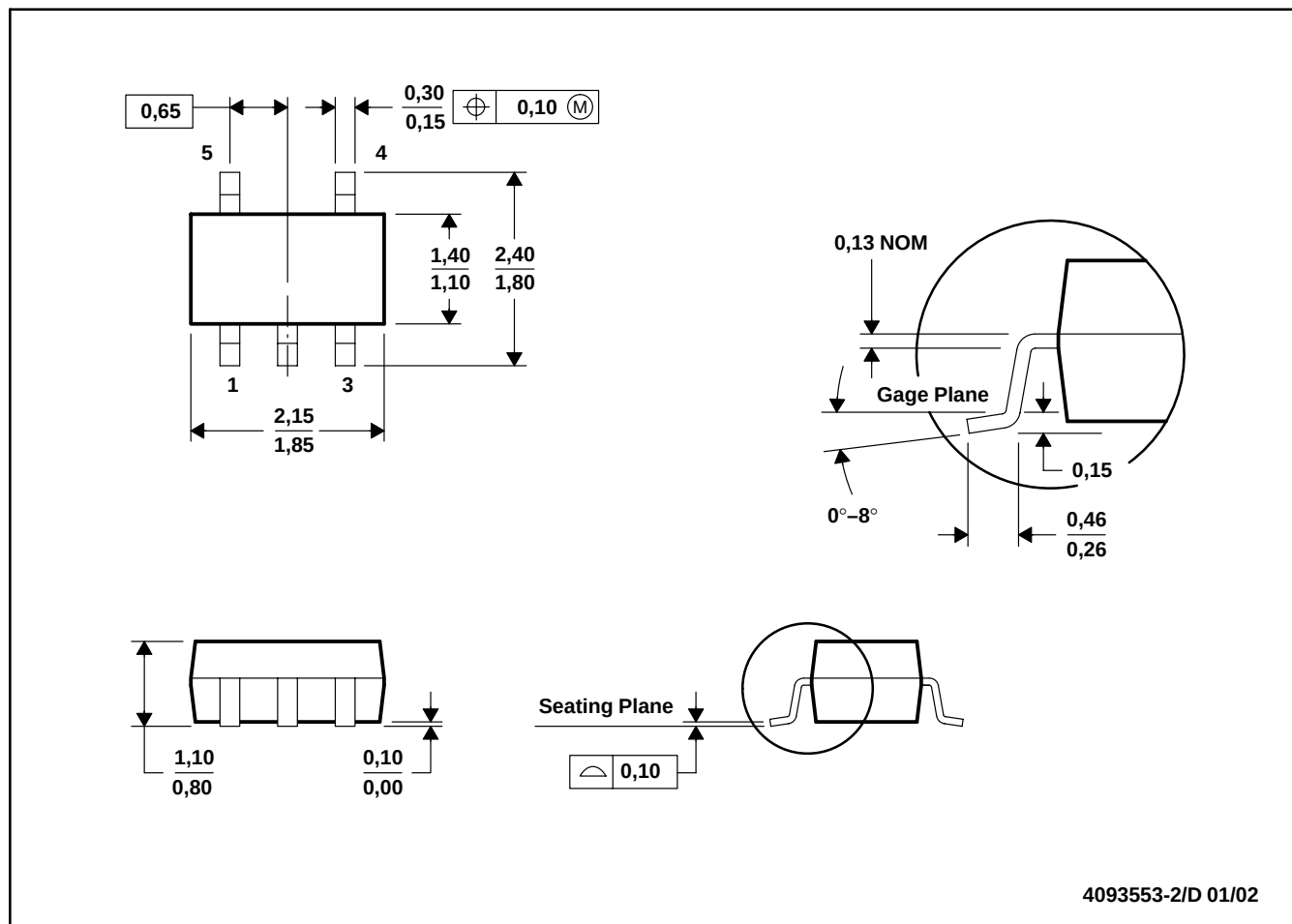


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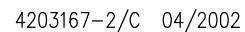
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



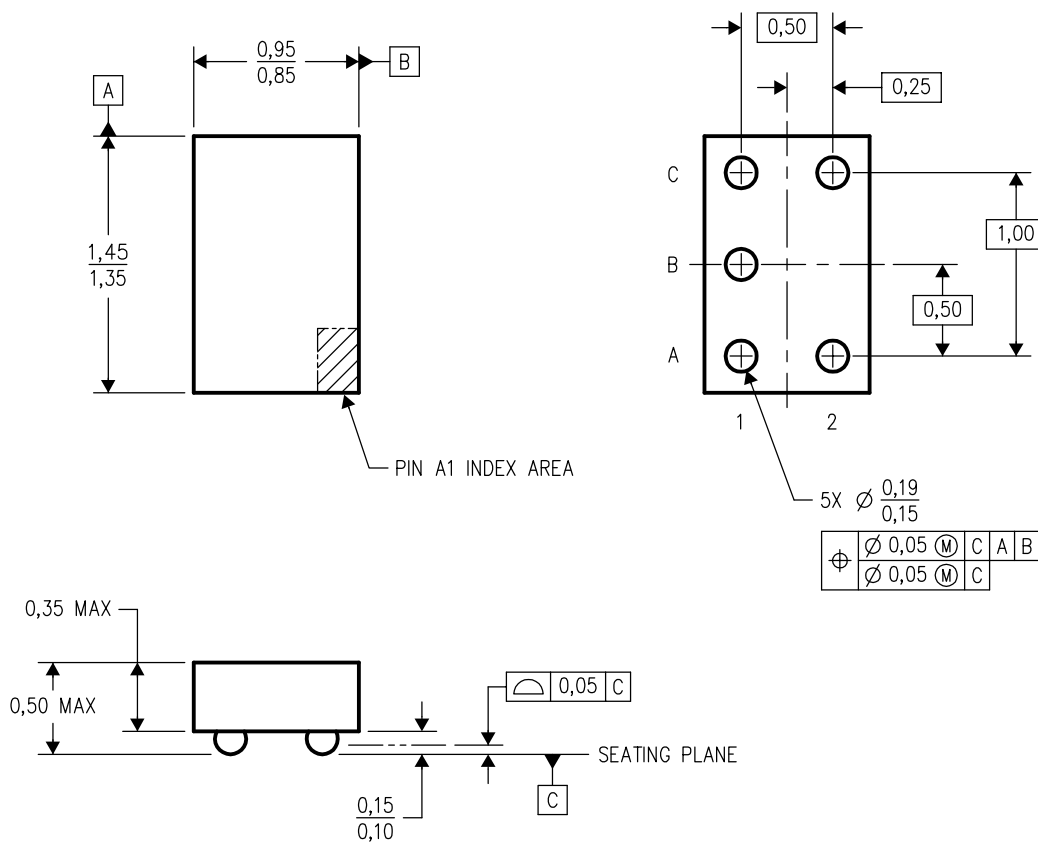
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-203



A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. Package complies to JEDEC MO-211 variation EA.
E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



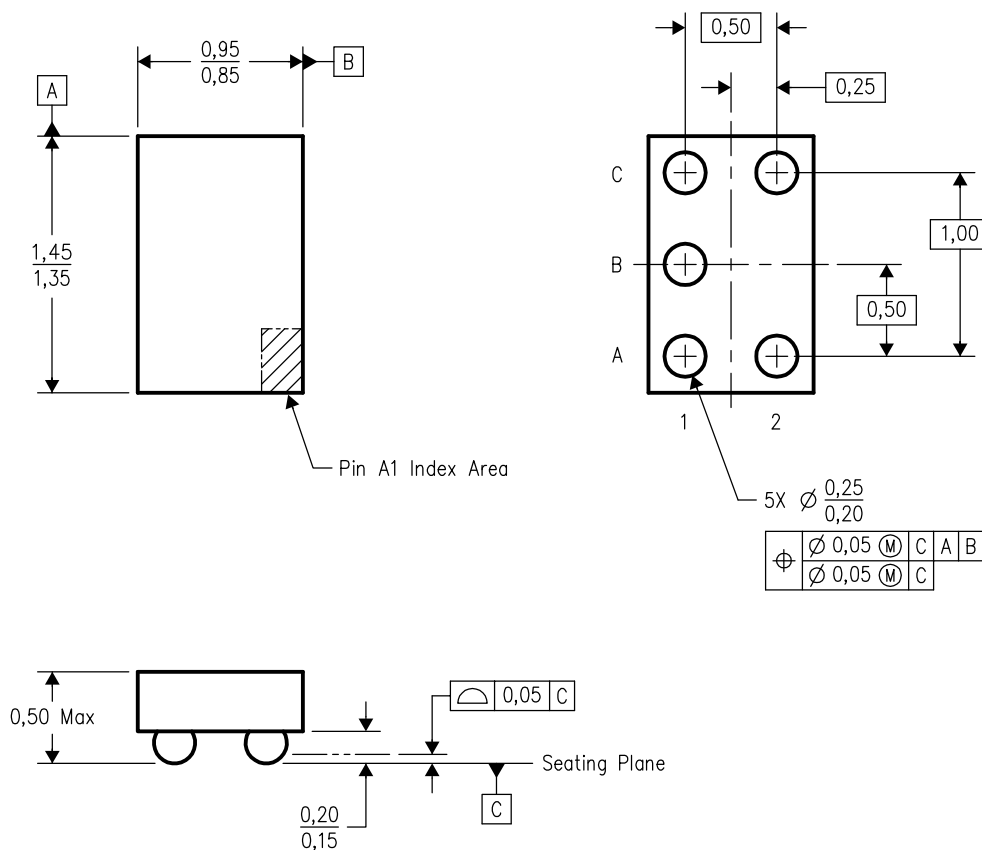
4204151-2/B 03/2002

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoFree™ package configuration.
 - Package complies to JEDEC MO-211 variation EA.
 - This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

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YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



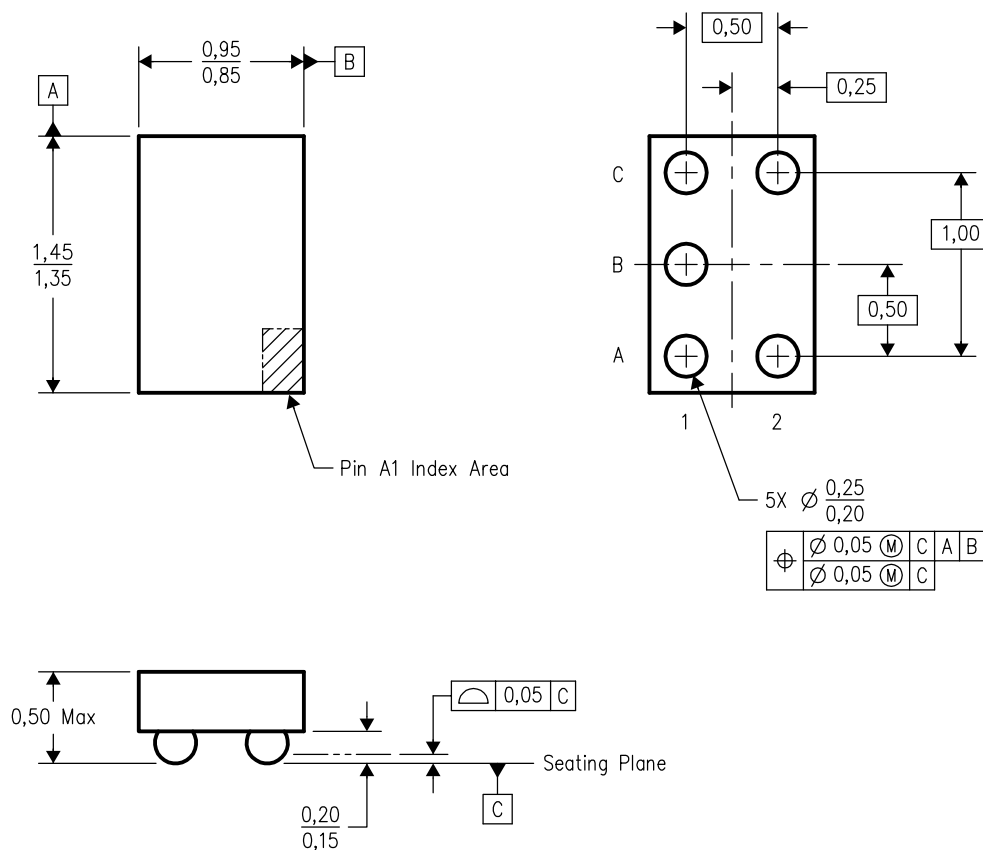
4204741-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204725-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

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