

HIGH PERFORMANCE CURRENT MODE PWM CONTROLLER

NOT FOR NEW DESIGN

1 FEATURES

- TRIMMED OSCILLATOR DISCHARGE CURRENT
- CURRENT MODE OPERATION TO 500kHz
AUTOMATIC FEED FORWARD
COMPENSATION
- LATCHING PWM FOR CYCLE-BY-CYCLE
CURRENT LIMITING
- INTERNALLY TRIMMED REFERENCE WITH
UNDERVOLTAGE LOCKOUT
- HIGH CURRENT TOTEM POLE OUTPUT
UNDERVOLTAGE LOCKOUT WITH
HYSTERESIS
- LOW START-UP CURRENT ($< 0.5\text{mA}$)
DOUBLE PULSE SUPPRESSION

2 DESCRIPTION

The UC384xA family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise DUTY CYCLE CONTROL under voltage lockout featuring start-up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Figure 1. Package

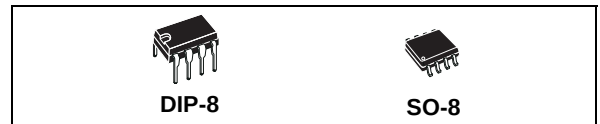


Table 1. Order Codes

Part Number	Package
UC2842AD1; UC3842AD1; UC2843AD1; UC3843AD1; UC2844AD1; UC3844AD1; UC2845AD1; UC3845AD1	SO-8
UC2842AN; UC3842AN; UC2843AN; UC3843AN; UC2844AN; UC3844AN; UC2845AN; UC3845AN	DIP-8

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842A and UC3844A have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications. The corresponding thresholds for the UC3843A and UC3845A are 8.5 V and 7.9V. The UC3842A and UC3843A can operate to duty cycles approaching 100%. A range of the zero to $< 50\%$ is obtained by the UC3844A and UC3845A by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

Figure 2. Block Diagram (toggle flip flop used only in UC3844A and UC3845A)

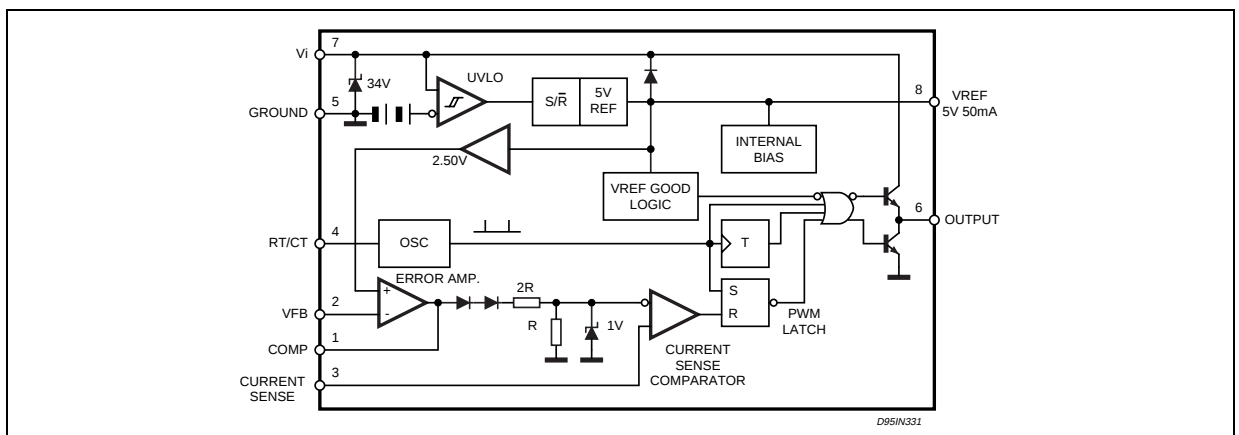


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage ($I_i < 30\text{mA}$)	Self Limiting	
I_O	Output Current	± 1	A
E_O	Output Energy (capacitive load)	5	μJ
	Analog Inputs (pins 2, 3)	- 0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (DIP-8)	1.25	W
P_{tot}	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (SO-8)	800	mW
T_{stg}	Storage Temperature Range	- 65 to 150	$^\circ\text{C}$
T_J	Junction Operating Temperature	- 40 to 150	$^\circ\text{C}$
T_L	Lead Temperature (soldering 10s)	300	$^\circ\text{C}$

* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

Figure 3. DIP-8/SO-8 Pin Connection (Top view)

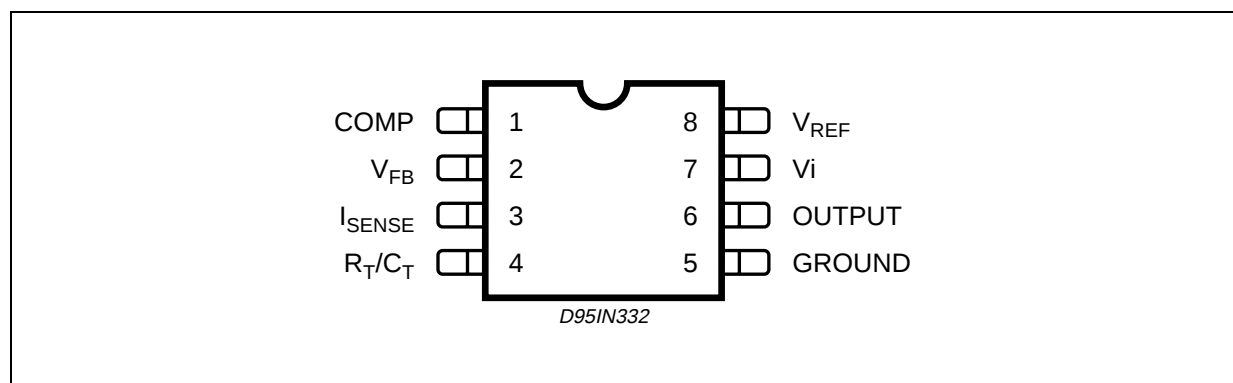


Table 3. Pin Description

N°	Pin	Function
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T .

Table 4. Thermal Data

Symbol	Parameter	DIP-8	SO-8	Unit
$R_{th j-amb}$	Thermal Resistance Junction-ambient	Max. 100	150	°C/W

Table 5. Electrical Characteristics

([note 1] Unless otherwise stated, these specifications apply for $-25 < T_{amb} < 85^{\circ}\text{C}$ for UC284XA; $0 < T_{amb} < 70^{\circ}\text{C}$ for UC384XA; $V_i = 15\text{V}$ (note 5); $R_T = 10\text{K}$; $C_T = 3.3\text{nF}$)

Symbol	Parameter	Test Condition	UC284XA			UC384XA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V _{REF}	Output Voltage	T _j = 25°C I _o = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV _{REF}	Line Regulation	12V ≤ V _i ≤ 25V		2	20		2	20	mV
ΔV _{REF}	Load Regulation	1 ≤ I _o ≤ 20mA		3	25		3	25	mV
ΔV _{REF} /ΔT	Temperature Stability	(Note 2)		0.2			0.2		mV/°C
	Total Output Variation	Line, Load, Temperature	4.9		5.1	4.82		5.18	V
e _N	Output Noise Voltage	10Hz ≤ f ≤ 10KHz T _j = 25°C (note 2)		50			50		μV
	Long Term Stability	T _{amb} = 125°C, 1000Hrs (note 2)		5	25		5	25	mV
I _{SC}	Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
OSCILLATOR SECTION									
f _{OSC}	Frequency	T _j = 25°C	47	52	57	47	52	57	KHz
Δf _{OSC} /ΔV	Frequency Change with Volt.	V _{CC} = 12V to 25V	–	0.2	1	–	0.2	1	%
ΔV _{REF} /ΔT	Frequency Change with Temp.	T _A = T _{low} to T _{high}	–	5	–	–	5	–	%
V _{OSC}	Oscillator Voltage Swing	(peak to peak)	–	1.6	–	–	1.6	–	V
I _{dischg}	Discharge Current (V _{OSC} =2V)	T _J = 25°C	7.8	8.3	8.8	7.8	8.3	8.8	mA
ERROR AMP SECTION									
V ₂	Input Voltage	V _{PIN1} = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
I _b	Input Bias Current	V _{FB} = 5V		-0.1	-1		-0.1	-2	μA
	A _{VOL}	2V ≤ V _o ≤ 4V	65	90		65	90		dB
BW	Unity Gain Bandwidth	T _J = 25°C	0.7	1		0.7	1		MHz
PSRR	Power Supply Rejec. Ratio	12V ≤ V _i ≤ 25V	60	70		60	70		dB
I _o	Output Sink Current	V _{PIN2} = 2.7V V _{PIN1} = 1.1V	2	12		2	12		mA
I _o	Output Source Current	V _{PIN2} = 2.3V V _{PIN1} = 5V	-0.5	-1		-0.5	-1		mA
	V _{OUT} High	V _{PIN2} = 2.3V;R _L = 15KΩ to Ground	5	6.2		5	6.2		V
	V _{OUT} Low	V _{PIN2} = 2.7V;R _L = 15KΩ to Pin 8		0.8	1.1		0.8	1.1	V
CURRENT SENSE SECTION									
G _V	Gain	(note 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
V ₃	Maximum Input Signal	V _{PIN1} = 5V (note 3)	0.9	1	1.1	0.9	1	1.1	V
SVR	Supply Voltage Rejection	12 ≤ V _i ≤ 25V (note 3)		70			70		dB
I _b	Input Bias Current			-2	-10		-2	-10	μA
	Delay to Output			150	300		150	300	ns

Table 5. Electrical Characteristics (continued)

([note 1] Unless otherwise stated, these specifications apply for $-25 < T_{amb} < 85^{\circ}\text{C}$ for UC284XA;
 $0 < T_{amb} < 70^{\circ}\text{C}$ for UC384XA; $V_i = 15\text{V}$ (note 5); $R_T = 10\text{K}$; $C_T = 3.3\text{nF}$)

Symbol	Parameter	Test Condition	UC284XA			UC384XA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OUTPUT SECTION									
V _{OL}	Output Low Level	I _{SINK} = 20mA		0.1	0.4		0.1	0.4	V
		I _{SINK} = 200mA		1.6	2.2		1.6	2.2	V
V _{OH}	Output High Level	I _{SOURCE} = 20mA	13	13.5		13	13.5		V
		I _{SOURCE} = 200mA	12	13.5		12	13.5		V
V _{OLS}	UVLO Saturation	V _{CC} = 6V; I _{SINK} = 1mA		0.7	1.2		0.7	1.2	V
t _r	Rise Time	T _j = 25°C C _L = 1nF ⁽²⁾		50	150		50	150	ns
t _f	Fall Time	T _j = 25°C C _L = 1nF ⁽²⁾		50	150		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION									
	Start Threshold	X842A/4A	15	16	17	14.5	16	17.5	V
		X843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
	Min Operating Voltage After Turn-on	X842A/4A	9	10	11	8.5	10	11.5	V
PWM SECTION									
	Maximum Duty Cycle	X842A/3A	94	96	100	94	96	100	%
		X844A/5A	47	48	50	47	48	50	%
	Minimum Duty Cycle				0			0	%
TOTAL STANDBY CURRENT									
I _{st}	Start-up Current	V _i = 6.5V for UCX843A/45A		0.3	0.5		0.3	0.5	mA
		V _i = 14V for UCX842A/44A		0.3	0.5		0.3	0.5	mA
I _i	Operating Supply Current	V _{PIN2} = V _{PIN3} = 0V		12	17		12	17	mA
V _{iz}	Zener Voltage	I _i = 25mA	30	36		30	36		V

Notes: 1. Max package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T_j as close to T_{amb} as possible.

2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at trip point of latch with V_{PIN2} = 0.

4. Gain defined as : $A = \Delta V_{PIN1} / \Delta V_{PIN3}$; $0 \leq V_{PIN3} \leq 0.8\text{V}$

5. Adjust V_i above the start threshold before setting at 15 V.

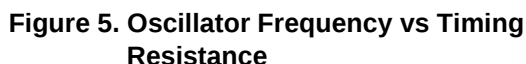


Figure 9. Current Sense Input Threshold vs. Error Amp Output Voltage.

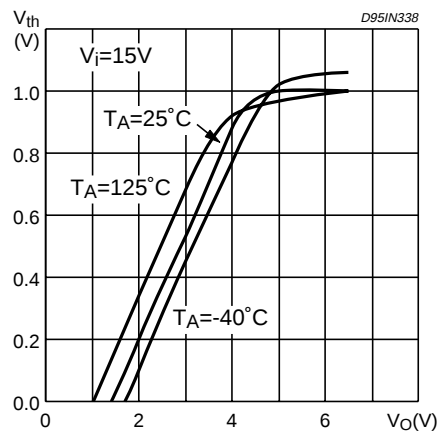


Figure 10. Reference Voltage Change vs. Source Current..

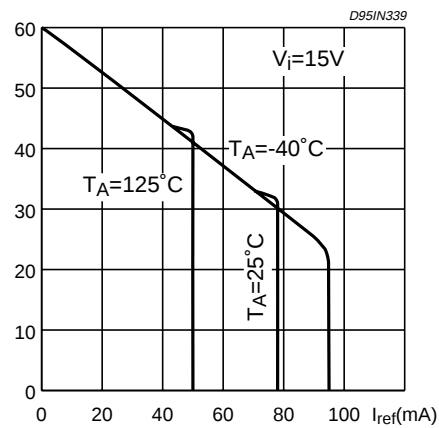


Figure 11. Reference Short Circuit Current vs. Temperature..

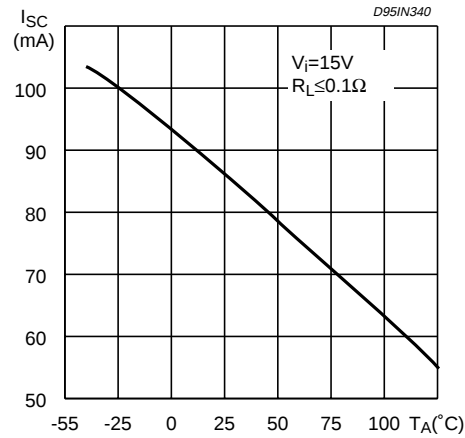


Figure 12. Output Saturation Voltage vs. Load Current.

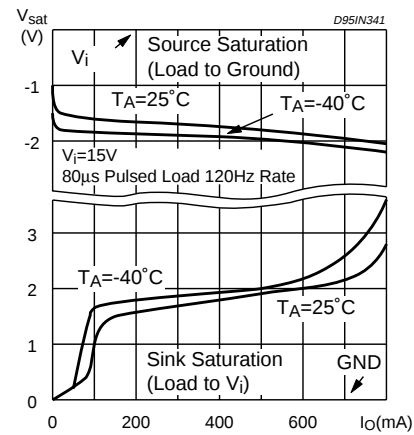


Figure 13. Supply Current vs. Supply Voltage.

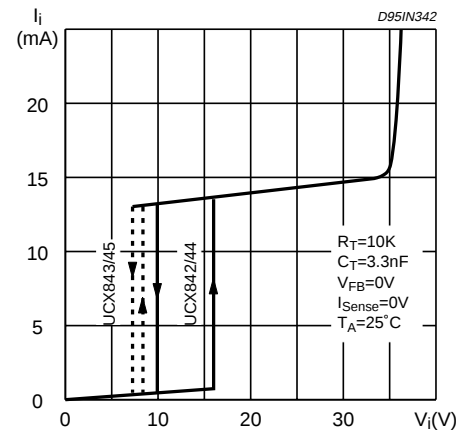


Figure 18. Under Voltage Lockout.

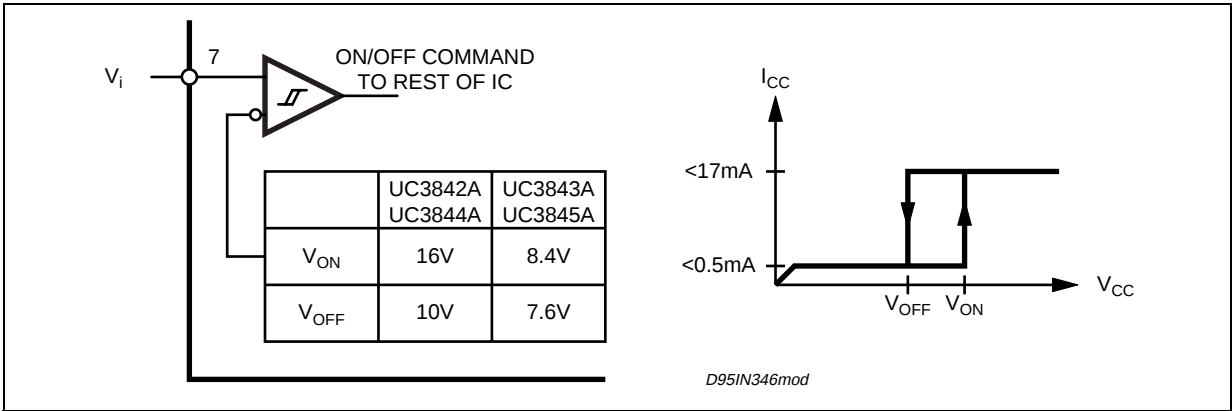
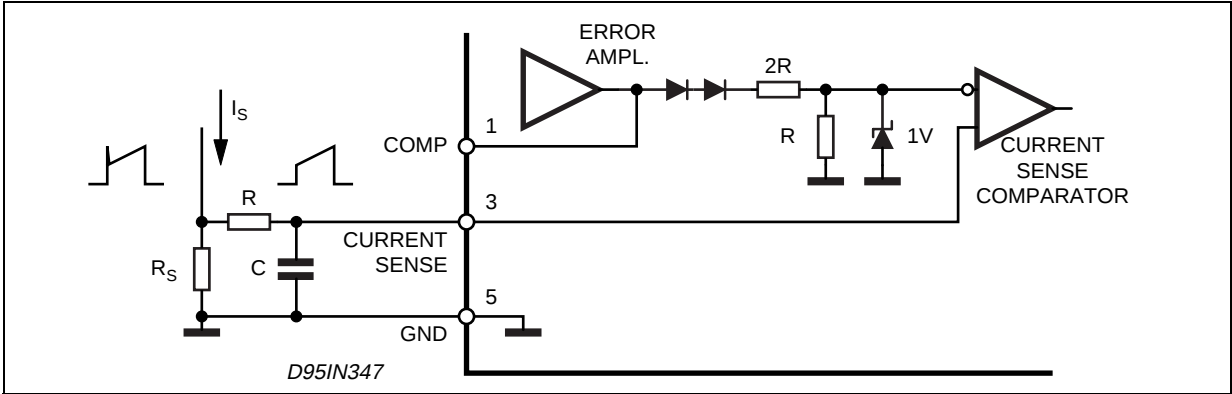


Figure 19. Current Sense Circuit.



Peak current (i_s) is determined by the formula

$$I_{Smax} \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 20. Slope Compensation Techniques.

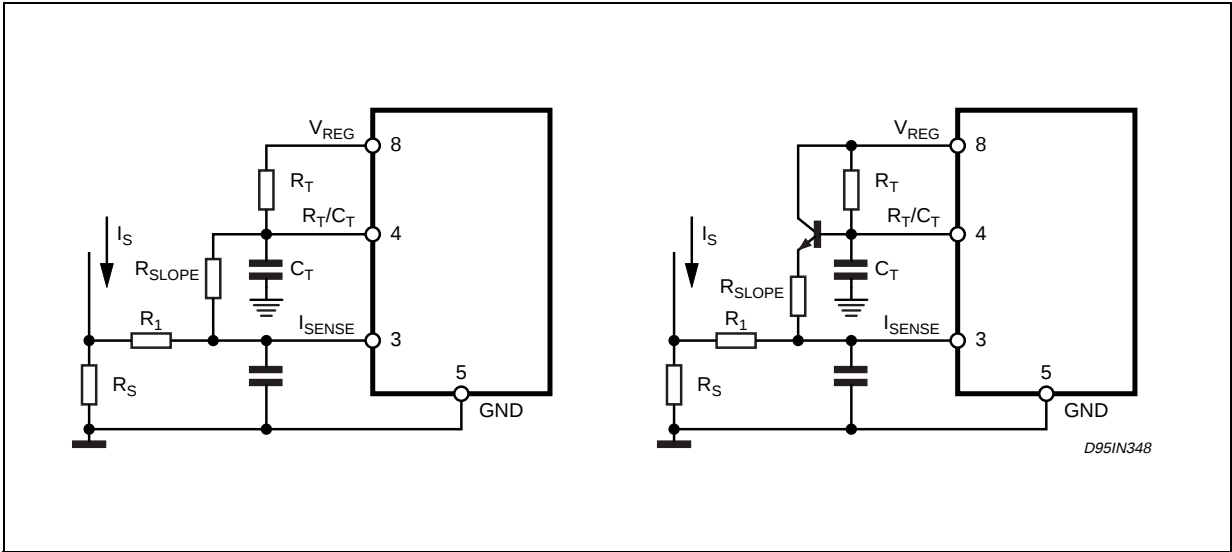
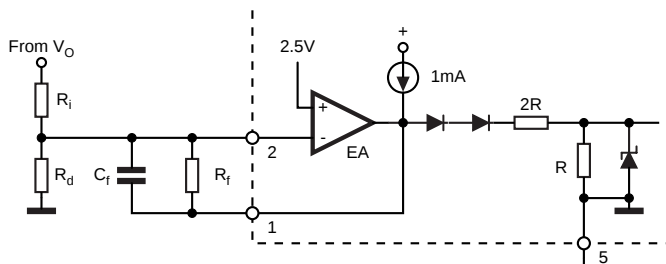
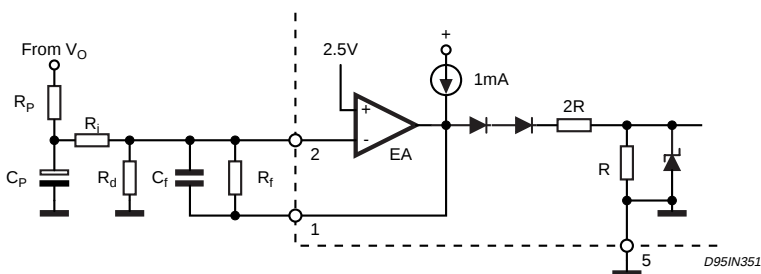


Figure 23. Error Amplifier Compensation

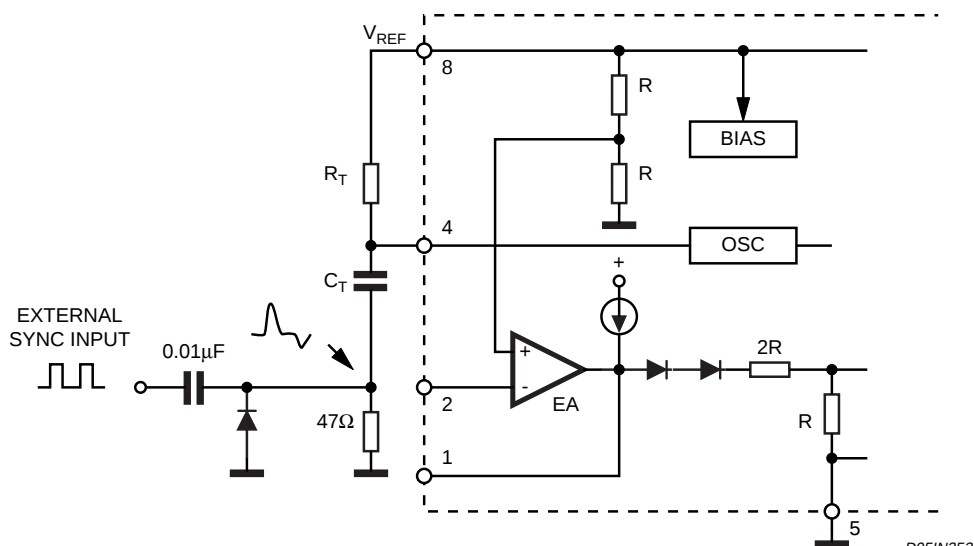


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 24. External Clock Synchronization.



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300mV below ground

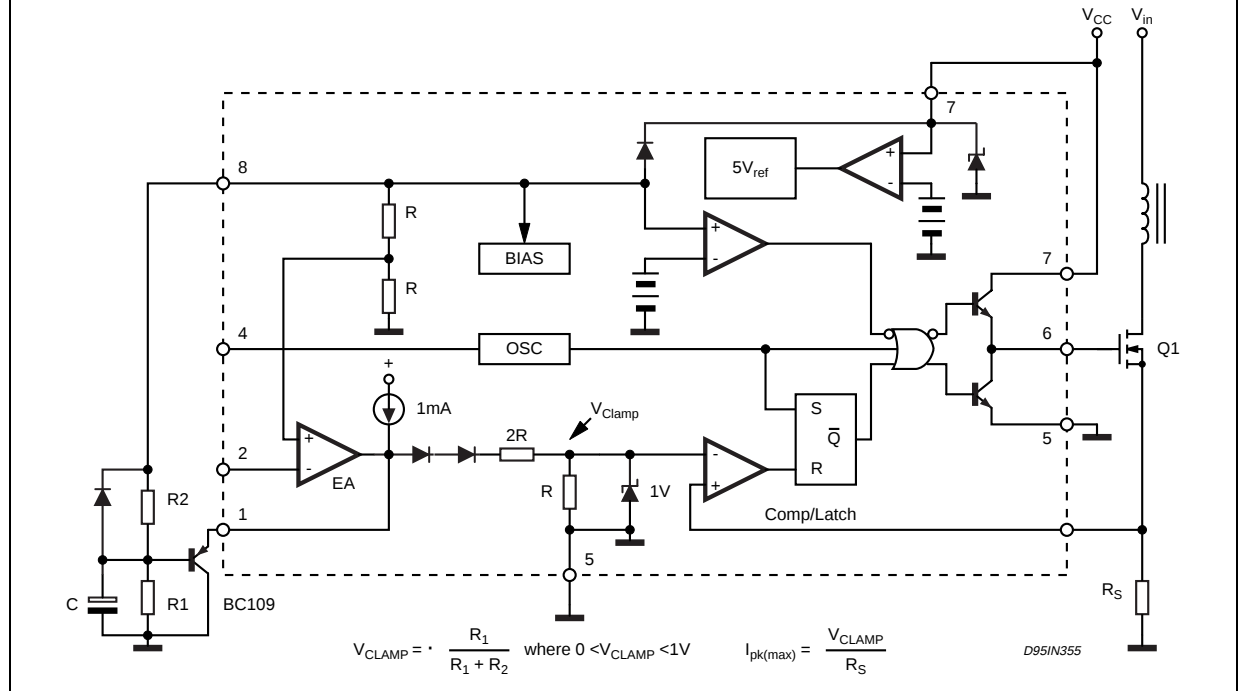
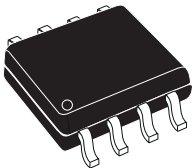


Figure 28. SO-8 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D ⁽¹⁾	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004
Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).						

OUTLINE AND
MECHANICAL DATA



SO-8

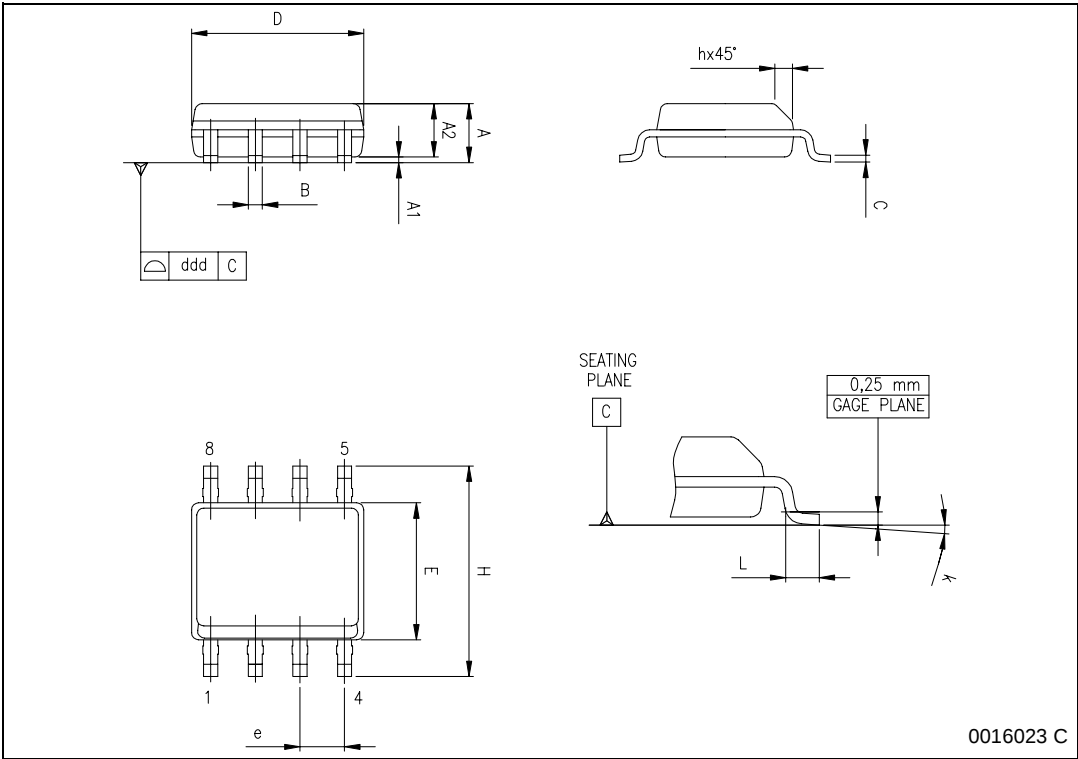
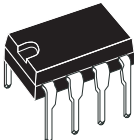


Figure 29. DIP-8 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



DIP-8

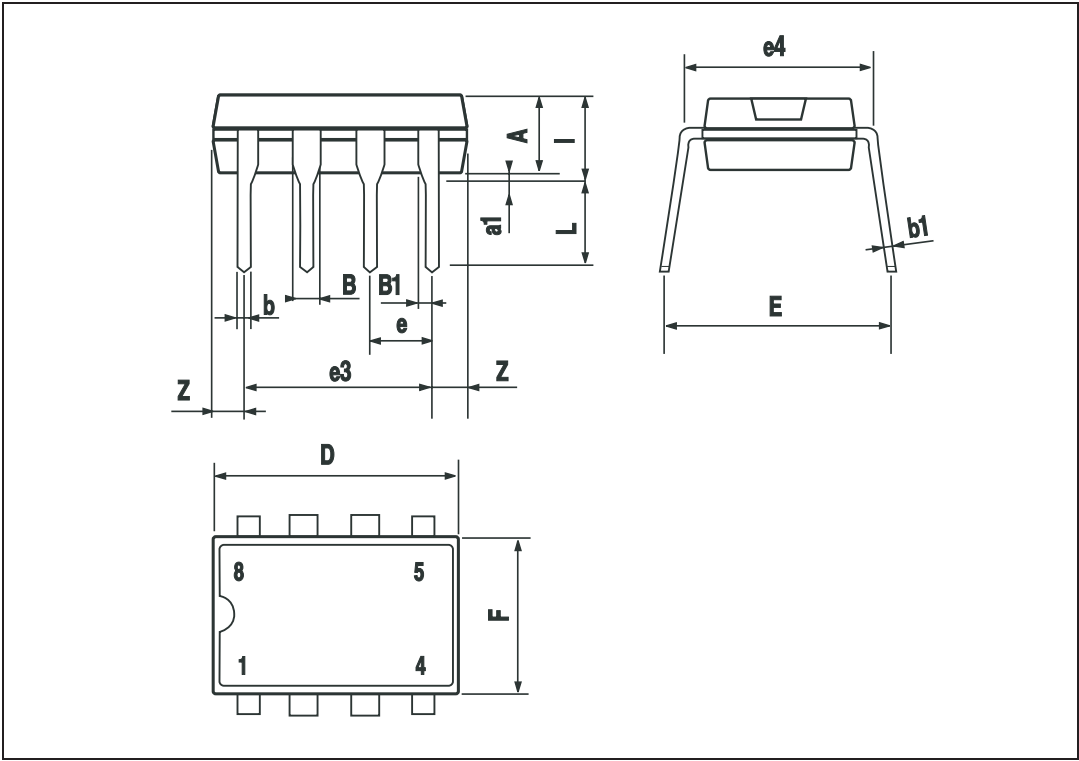


Table 6. Revision History

Date	Revision	Description of Changes
March 1999	4	First Issue in EDOCS
May 2004	5	NOT FOR NEW DESIGN

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