

PJD15N06L

60V N-Channel Enhancement Mode MOSFET

FEATURES

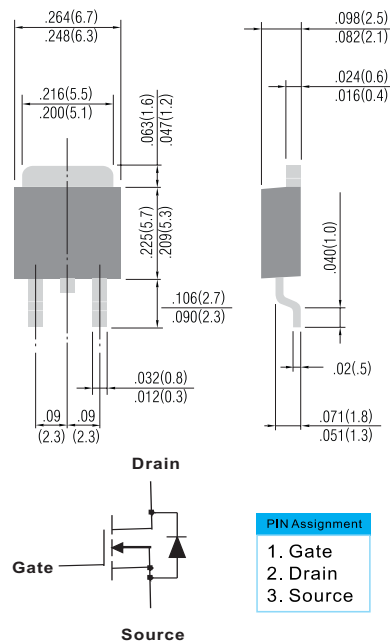
- $R_{DS(ON)}$ $V_{GS}@10V, I_{DS}@10A=40m\Omega$
- $R_{DS(ON)}$ $V_{GS}@4.5V, I_{DS}@8.0A=50m\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for DC/DC Converters
- Fully Characterized Avalanche Voltage and Current
- Pb free product : 99% Sn above can meet RoHS environment substance directive request

MECHANICAL DATA

- Case: TO-252 Molded Plastic
- Terminals : Solderable per MIL-STD-750D, Method 1036.3
- Marking : 15N06L

DPAK / TO-252

Unit: inch (mm)



Maximum RATINGS and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	15	A
Pulsed Drain Current ¹⁾	I_{DM}	60	A
Maximum Power Dissipation	P_D	$T_A=25^\circ\text{C}$ 38 $T_A=75^\circ\text{C}$ 22	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	$^\circ\text{C}$
Avalanche Energy with Single Pulse $I_D=21A, V_{DD}=30V, L=0.5mH$	E_{AS}	120	mJ
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	3.3	$^\circ\text{C/W}$
Junction-to Ambient Thermal Resistance(PCB mounted) ²	$R_{\theta JA}$	50	$^\circ\text{C/W}$

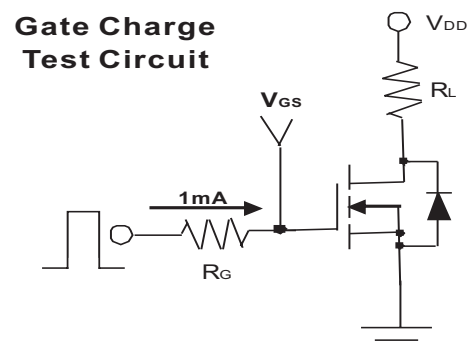
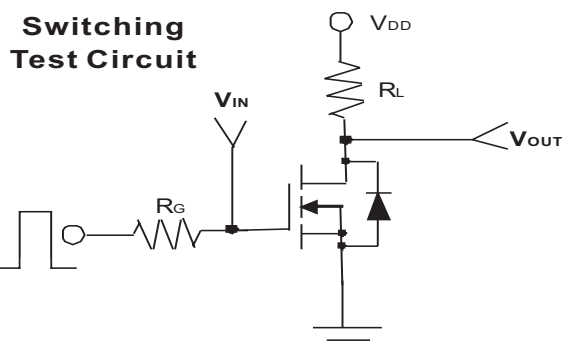
Note: 1. Maximum DC current limited by the package
2. Surface mounted on FR4 board, $t \leq 10$ sec

PANJIT RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN,FUNCTIONS AND RELIABILITY WITHOUT NOTICE

PJD15N06L

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	60	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =8.0A	-	36	50	mΩ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =10A	-	32	40	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	uA
Gate Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Forward Transconductance	g _{fS}	V _{DS} =10V, I _D =10A	20	-	-	S
Dynamic						
Total Gate Charge	Q _g	V _{DS} =30V, I _D =10A, V _{GS} =5V	-	17.20	-	nC
		V _{DS} =30V, I _D =10A V _{GS} =10V	-	32.5	-	
Gate-Source Charge	Q _{gs}		-	3.6	-	
Gate-Drain Charge	Q _{gd}		-	5.4	-	
Turn-On Delay Time	T _{d(on)}	V _{DD} =30V, R _L =30Ω I _D =1A, V _{GEN} =10V R _G =3.6Ω	-	13.2	16.5	ns
Turn-On Rise Time	t _{rr}		-	5.8	7.6	
Turn-Off Delay Time	t _{d(off)}		-	42	55	
Turn-Off Fall Time	t _f		-	6.2	7.8	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V f=1.0MH _z	-	1750	-	pF
Output Capacitance	C _{oss}		-	130	-	
Reverse Transfer Capacitance	C _{rss}		-	80	-	
Source-Drain Diode						
Max. Diode Forward Current	I _s	-	-	-	10	A
Diode Forward Voltage	V _{SD}	I _s =10A , V _{GS} =0V	-	0.9	1.2	V



PJD15N06L

Typical Characteristics Curves ($T_J=25^\circ\text{C}$, unless otherwise noted)

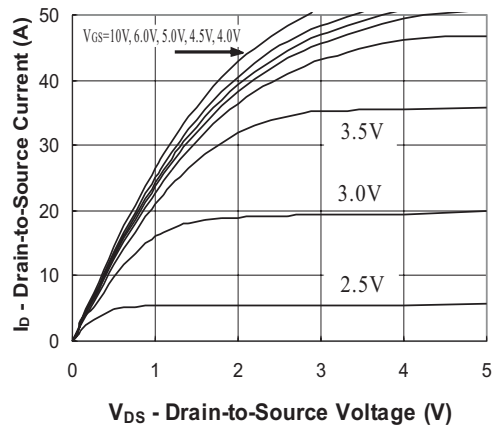


FIG.1- Output Characteristic

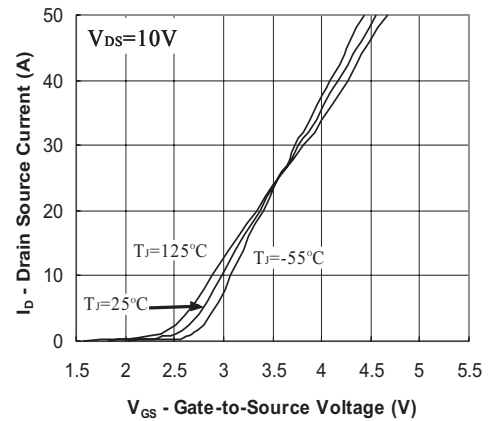


FIG.2- Transfer Characteristic

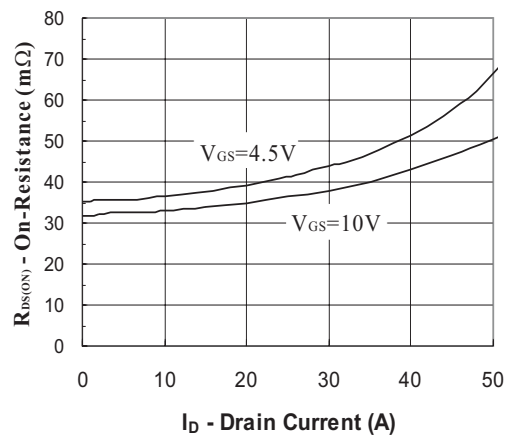


FIG.3- On Resistance vs Drain Current

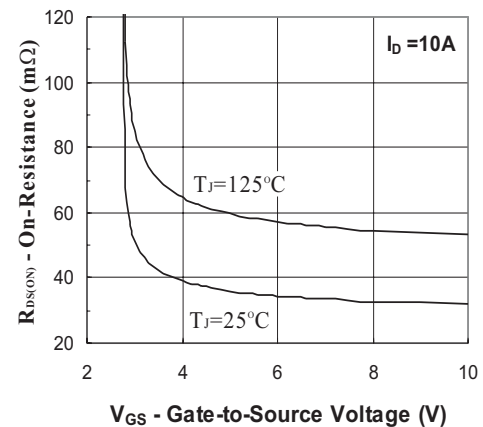


FIG.4- On Resistance vs Gate to Source Voltage

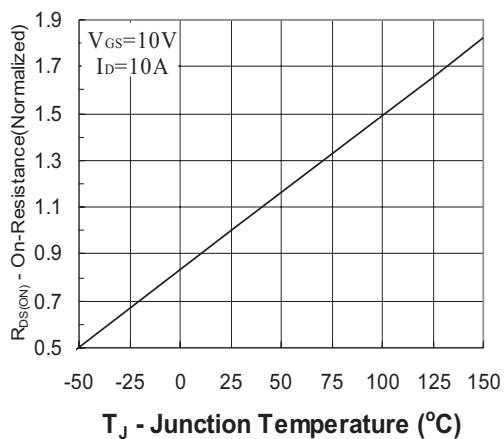
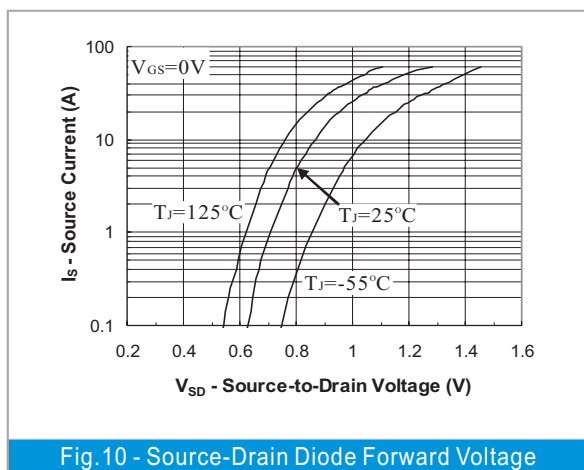
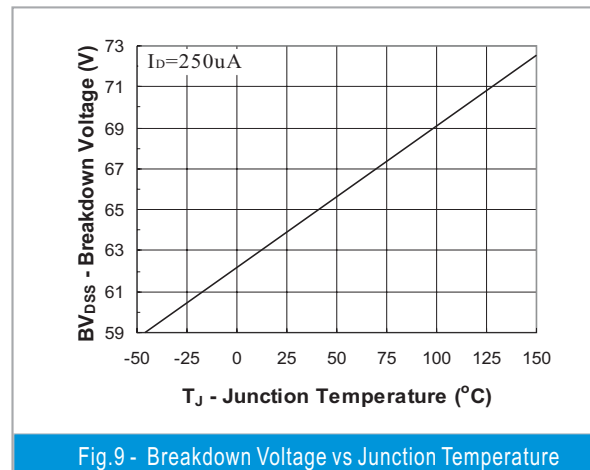
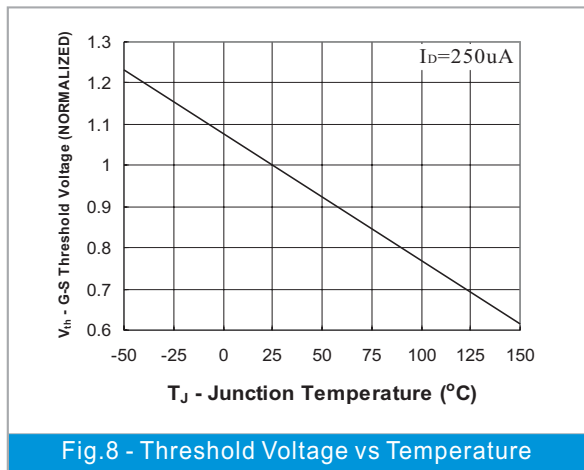
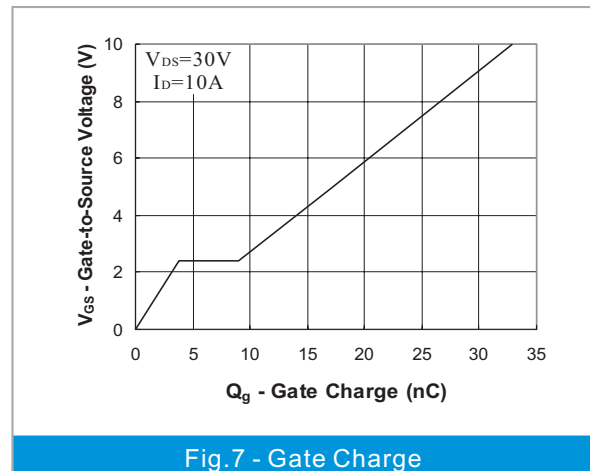
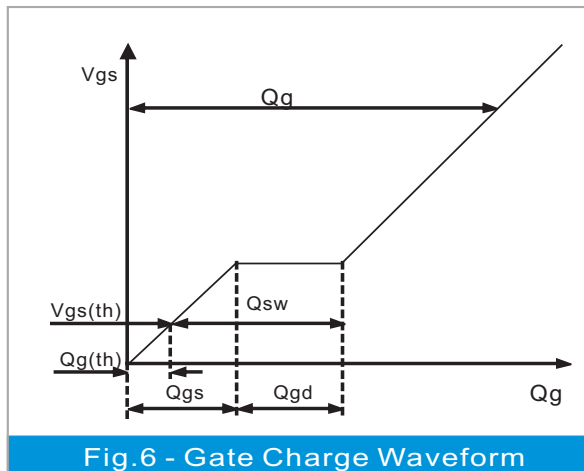


FIG.5- On Resistance vs Junction Temperature

PJD15N06L



LEGAL STATEMENT

Copyright PanJit International, Inc 2006

The information presented in this document is believed to be accurate and reliable. The specifications and information herein are subject to change without notice. Pan Jit makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose. Pan Jit products are not authorized for use in life support devices or systems. Pan Jit does not convey any license under its patent rights or rights of others.