## Features

- **Comprehensive Library of Standard Logic and I/O Cells**
- **ATC18 Core and I/O Cells Designed to Operate with VDD = 1.8V ± 0.15V as Main Target Operating Conditions**
- **IO25 and IO33 Pad Libraries Provide Interfaces to 2.5V and 3V Environments**
- **Oscillators Provide Stable Clock Sources**
- **Basic Analog Input/Output, Power, Ground and Multiplexer Cells Available**
- **General-purpose Analog Cells Include Regulators, Power Management Cells, Op Amps, Comparators, ADCs and DACs, High-performance Analog Cells Can Be Developed on Request**
- **Memory Cells Compiled to the Precise Requirements of the Design**
- **Compatible with Atmel's Extensive Range of Microcontroller, DSP, Standard-interface and Application-specific Cells**

## 1. Description

The Atmel ATC18 Library is fabricated on a proprietary 0.18 micron, up to six-layer-metal CMOS process intended for use with a supply voltage of 1.8V ± 0.15V. Table 1-1 shows the range for which Atmel library cells have been characterized.

**Table 1-1.** Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | Core and Standard I/Os | 1.65 | 1.8 | 1.95 | V |
| $V_{DD2.5}$ | DC Supply voltage | 2.5V Interface I/Os | 2.25 | 2.5 | 2.75 | V |
| $V_{DD3.3}$ | DC Supply Voltage | 3.3V Interface I/Os | 3 | 3.3 | 3.6 | V |
| $V_I$ | DC Input Voltage | | 0 | | $V_{DD}$ | V |
| $V_O$ | DC Output Voltage | | 0 | | $V_{DD}$ | V |
| TEMP | Operating Free Air Temperature Range | Industrial | -40 | | +85 | °C |
| TSG | Storage Temperature | | -60 | | +150 | °C |

# Cell-based ASIC

# ATC18

# Summary

**NOTE:** This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

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## 1.1 Absolute Maximum Ratings

Operation of a device outside the range given in Table 1-2 may cause permanent damage to the device and/or affect reliability.

**Table 1-2.** Absolute Maximum Ratings

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | Core | -0.3 | 2.0 | V |
| $V_{DD2.5}$ | DC Supply voltage | 2.5V Interface I/Os | -0.3 | 4.0 | V |
| $V_{DD3.3}$ | DC Supply Voltage | 3.3V Interface I/Os | -0.3 | 4.0 | V |
| $V_I$ | DC Input Voltage,1.8V I/Os | | -0.3 | $V_{DD}$ + 0.3, 2.0 max | V |
| $V_I$ | DC Input Voltage, 3.3V I/Os | | -0.3 | $V_{DD3.3}$ + 0.3, 4.0 max | V |
| $V_O$ | DC Output Voltage, 1.8V I/Os | | -0.3 | $V_{DD}$+ 0.3, 2.0 max | V |
| $V_O$ | DC Output Voltage, 3.3V I/Os | | -0.3 | $V_{DD3.3}$ + 0.3, 4.0 max | V |
| TEMP | Operating Free Air Temperature Range | Industrial | -40 | +125 | °C |
| TSG | Storage Temperature | | -60 | +150 | °C |

The Atmel cell libraries have been designed in order to be compatible with each other. Simulation representations exist for three types of operating conditions. They correspond to the characterization conditions defined as follows:

- MIN conditions (industrial best case):

  $T_J$ = -40° C

  $V_{DD}$(cell) = 1.95V

  Process = fast

- TYP conditions (industrial typical case):

  $T_J$ = +25° C

  $V_{DD}$(cell) = 1.8V

  Process = typ

- MAX conditions (industrial worst case):

  $T_J$ = +100° C

  $V_{DD}$(cell) = 1.60V

  Process = slow

Delays to tristate are defined as delay to turn off (VGS < VT) of the driving devices.

Output pad drain current corresponds to the output current of the pad when the output voltage is $V_{OL}$ or $V_{OH}$. The output resistor of the pad and the voltage drop due to access resistors (in and out of the die) are taken into account. In order to have accurate timing estimates, all characterization has been run on electrical netlists extracted from the layout database.

# 2. Standard Cell Library SClib

The Atmel Standard Cell Library, SClib, contains a comprehensive set of combinational logic and storage cells. The SClib library includes cells which belong to the following categories:

- Buffers and Gates
- Multiplexers
- Flip-flops
- Scan Flip-flops
- Latches
- Adders and Subtractors

## 2.1 Decoding the Cell Name

Table 2-1 shows the naming conventions for the cells in the SClib library. Each cell name begins with either a two-, three-, or four-letter code that defines the type of cell. This indicates the range of standard cells available.

**Table 2-1.** Cell Codes

| Code | Description | Code | Description |
|---|---|---|---|
| AD | Adder | INVB | Balanced Inverter |
| AH | Half Adder | INVT | Inverting 3-State Buffer |
| AS | Adder/Subtractor | LA | D Latch |
| AN | AND Gate | MI | Inverting Multiplexer |
| AOI | AND-OR-Invert Gate | MX | Multiplexer |
| AON | AND-OR-AND-Invert Gates | ND | NAND Gate |
| AOR | AND-OR Gate | NR | NOR Gate |
| BH | Bus Holder | OAI | OR-AND-Invert Gate |
| BUFB | Balanced Buffer | OAN | OR-AND-OR-Invert Gates |
| BUFF | Non-Inverting Buffer | OR | OR Gate |
| BUFT | Non-Inverting 3-State Buffer | ORA | OR-AND Gate |
| CG | Carry Generator | SD | Multiplexed Scan D Flip-Flop |
| CLK2 | Clock Buffer | SE | Multiplexed Scan Enable D Flip-Flop |
| DE | D-Enabled Flip-Flop | SU | Subtractor |
| DF | D Flip-Flop | XN | Exclusive NOR Gate |
| INV0 | Inverter | XR | Exclusive OR Gate |

## 2.2 Cell Matrices

Table 2-2 and Table 2-3 show storage elements in the SClib library. Note that all storage elements feature buffered clock inputs and buffered output.

**Table 2-2.** D Flip-Flops

| Macro Name | Set | Clear | Enabled D Input | 1 x Drive | 2 x Drive | Single Output |
|---|---|---|---|---|---|---|
| DFBRBx | ∞ | ∞ | | ∞ | ∞ | |
| DFCRBx | | ∞ | | ∞ | ∞ | |
| DFCRQx | | • | | • | • | • |
| DFCRNx | | • | | • | • | |
| DFNRBx | | | | ∞ | ∞ | |
| DFNRQx | | | | ∞ | ∞ | ∞ |
| DFPRBx | ∞ | | | ∞ | ∞ | |
| DEPRQx | ∞ | | ∞ | ∞ | • | ∞ |
| DECRQx | | ∞ | ∞ | ∞ | ∞ | ∞ |
| DENRQx | | | ∞ | ∞ | ∞ | ∞ |
| DENRBx | | | ∞ | ∞ | ∞ | |

**Table 2-3.** Scan Flip-flops

| Macro Name | Set | Clear | 1xDrive | 2xDrive | Single Output |
|---|---|---|---|---|---|
| SDBRBx | • | • | • | • | |
| SDCRBx | | • | • | • | |
| SDCRNx | | • | • | • | • |
| SDCRQx | | • | • | • | • |
| SDNRBx | | | • | • | |
| SDNRNx | | | • | • | • |
| SDNRQx | | | • | • | • |
| SDPRBx | • | | • | • | |
| SECRQx | | • | • | • | • |
| SENRQx | | | • | • | • |
| SEPRQx | • | | • | • | • |

# 3. Input/Output Pad Cell Libraries IO18lib, IO25lib and IO33lib

The Atmel Input/Output Cell Library IO18lib contains a comprehensive list of input, output, bi-directional and tristate cells. The ATC18 (1.8V) cell library includes a special set of I/O cells, IO25lib (IO33lib), for interfacing with external 2.5V (3.3V) devices.

## 3.1 Voltage Levels

The IO18lib library is made up exclusively of low-voltage chip interface circuits powered by a voltage level in the range of 1.65V to 1.95V. The library is compatible with SClib, 1.8-volt standard cell library.

## 3.2 Power and Ground Pads

Designers are strongly encouraged to provide three kinds of power pairs for the IO18lib library. These are “AC”, “DC” and core power pairs. AC power is used by the I/O to switch its output from one state to the other. This switching generates noise in the AC power buses on the chip. DC power is used by the I/O to maintain its output in a steady state. The best noise performance is achieved when the DC power buses on the chip are free of noise; you are encouraged to use separate power pairs for AC and DC power to prevent most of the noise in the AC power buses from reaching the DC power buses. You can use the same power pairs to supply both DC power to the I/Os and power to the core without affecting noise performance.

**Table 3-1.** VSS Power Pad Combinations

| Core | Switching I/O | Quiet I/O | | |
|---|---|---|---|---|
| Vssi/gnd | VssAC | VssDC | Library Cell Name | Signal Name |
| •/• | | | pv18i00 | VSS |
| | • | | pv18a00 | VSS |
| | | • | pv18d00 | VSS |
| | • | • | pv18e00 | VSS |
| •/• | | • | pv18b00 | VSS |
| •/• | • | • | pv18f00 | VSS |
| /• | | | pv18c00 | VSS |

**Table 3-2.** VDD Power Pad Combinations

| Core | Switching I/O | Quiet I/O | | |
|---|---|---|---|---|
| Vddi/vdd | VddAC | VddDC | Library Cell Name | Signal Name |
| •/• | | | pv18i18 | VDD |
| | • | | pv18a18 | VDD |
| | | • | pv18d18 | VDD |
| | • | • | pv18e18 | VDD |
| •/• | | • | pv18b18 | VDD |
| •/• | • | • | pv18f18 | VDD |
| /• | | | pv18c18 | VDD |

## 3.3 Cell Matrices

**Table 3-3.** CMOS Pads

| CMOS Cell Name | 3-state I/O | Output Only | 3-state Output Only | Drive Strength | Pad Sites Used |
|---|---|---|---|---|---|
| PC18B01 | • | | | 1x | 1 |
| PC18B02 | • | | | 2x | 1 |
| PC18B03 | • | | | 3x | 1 |
| PC18B04 | • | | | 4x | 1 |
| PC18B05 | • | | | 5x | 1 |
| PC18O01 | | • | | 1x | 1 |
| PC18O02 | | • | | 2x | 1 |
| PC18O03 | | • | | 3x | 1 |
| PC18O04 | | • | | 4x | 1 |
| PC18O05 | | • | | 5x | 1 |
| PC18T01 | | | • | 1x | 1 |
| PC18T02 | | | • | 2x | 1 |
| PC18T03 | | | • | 3x | 1 |
| PC18T04 | | | • | 4x | 1 |
| PC18T05 | | | • | 5x | 1 |

**Table 3-4.** TTL Pads

| TTL Cell Name | 3-state I/O | Output Only | 3-state Output Only | Drive Strength | Pad Sites Used |
|---|---|---|---|---|---|
| PT18B01 | • | | | 2 mA | 1 |
| PT18B02 | • | | | 4 mA | 1 |
| PT18B03 | • | | | 8 mA | 1 |
| PT18O01 | | • | | 2 mA | 1 |
| PT18O02 | | • | | 4 mA | 1 |
| PT18O03 | | • | | 8 mA | 1 |
| PT18T01 | | | • | 2 mA | 1 |
| PT18T02 | | | • | 4 mA | 1 |
| PT18T03 | | | • | 8 mA | 1 |

**Table 3-5.** CMOS/TTL Input Only Pad

| CMOS Cell Name | Input Levels | Schmitt Input Level Shifter | Non-inverting | Inverting | Pad Sites Used |
|---|---|---|---|---|---|
| PC18D01 | CMOS | | • | | 1 |
| PC18D11 | CMOS | | | • | 1 |
| PC18D21 | CMOS | • | • | | 1 |
| PC18D31 | CMOS | • | | • | 1 |

Note: All 3-state I/Os, 3-state output only and input pads are also available with pull-up and pull-down device.

## 4. Basic Analog Cell Library, ANA18lib, ANA25lib, ANA33lib

The Atmel basic analog library makes the following parts available:

- Multiplexer modules
  - Multiplexers to minimize cross-talk (for use with high-impedance nodes).
  - Multiplexers to minimize ON resistance.
- Analog input and output cells
- Analog power and ground cells

A special set of basic analog I/O cells, ANA25lib (ANA33lib), is available for interfacing with external 2.5V (3.3V) devices.

## 5. General-purpose Analog Cell Library, GPlib

The General-purpose Analog Cell Library (GPlib) is composed of cells performing various analog functions.

Currently available are:

- Regulators
- Power Management Cells
- Op Amps
- Comparators
- ADCs
- DACs
- PLLs

Additional high-performance, complex analog cells can be developed according to specific customer requirements.

## 6. Oscillator Cell Library, OSC18lib

The Atmel Oscillator Library provides stable clock sources. It comprises five standard oscillators.

The Atmel two-pad oscillators are designed with the Pierce three-point oscillator structure.

For the 32.768 kHz oscillator, the load capacitance must be between 6 pF and 12.5 pF. For high-frequency oscillators, the load capacitance must be between 15 pF and 20 pF. External capacitors must be added in order to obtain the correct load capacitance.

Clock output is high at off state (onosc = 0). The oscillators provide a bypass mode (onosc = 0), clock = not (xin).

Table 6-1 gives the available OSC18lib cells and their major characteristics.

**Table 6-1.** Oscillator Cells

| Cell Name | Description |
|---|---|
| OSC18f33K | 32.786 kHz crystal |
| OSC18f9M | 9 MHz crystal oscillator |
| OSC18f16M | 16 MHz crystal oscillator |
| OSC18f27M | 27 MHz crystal oscillator |

# 7. Compiled CMOS Memories

The Atmel CMOS Memory Compiler Library enables users to compile memories for the functions Single-port Synchronous RAM, Dual-port Synchronous RAM, Via Programmable ROM and Two-port Synchronous Register File according to their precise requirements. Memories compiled in this way can be instanced as often as required in designs, alongside cells from other Atmel CBIC libraries.

## 7.1 Single-port Synchronous SRAM

Key features of the single-port synchronous SRAM are:

- High-density (HD) SRAM
- 350 MHz worst-case cycle time
- Zero Quiescent Current
- 3-state outputs
- Several aspect ratios for optimization
- Separate Data-in, Data-out pins support a write-through feature
- Asynchronous write-through for testing interface shadow logic
- BIST interface
- Optional Sub-word write decode

The single-port SRAM compiler is a high-density RAM compiler with quiescent current consumption equal to zero when the SRAM is not in a read or write mode. The compiler is optimized for a power supply voltage range of 1.62V to 1.98V and can operate at voltages as low as 1.2V. The SRAM instances can be built with several aspect ratios for maximum area and performance optimization. Separate output (Q) and input (D) pins allow a write-through cycle feature. An asynchronous write through mode (AWT) allows testing of interface shadow logic. Built-in BIST interface allows for easy connection to most memBIST solutions. The special test modes allow externally bypassing read and write self-timed circuits and adjusting read and write margins. The SRAM memory also includes a sub-word feature where selective write to each group of 8-bit subwords can be done. A maskable write enable signal is provided for each 8-bit group.

Table 7-1 gives the range of permitted single-port synchronous RAM configurations.

**Table 7-1.** Configuration Range

| Parameter | Min | Max | Increment |
|---|---|---|---|
| Address Locations (words) | 32 | 16K | 1 x CM(1) |
| Word Size (Number of I/O bits) | 2 | 128 | 1 bit |
| Total Bits in Core (Word Size x Address Locations) | 128 | 512K | |

Note: 1. CM = 4, 8, 16: Column Mux option

## 7.2 Dual-port Synchronous RAM

Key features of the dual-port synchronous RAM are:

- High-density (HD) SRAM
- 300 MHz worst-case cycle time
- Zero Quiescent Current
- 3-state outputs

- Several aspect ratios for optimization
- Separate Data-in, Data-out pins support a write-through feature
- Asynchronous write-through for testing interface shadow logic
- BIST interface
- Optional Sub-word decode

The dual-port synchronous RAM compiler is a high-density RAM compiler with quiescent current consumption equal to zero when the SRAM is not in a read or write mode. The compiler is optimized for a power supply voltage range of 1.62V to 1.98V and can operate at voltages as low as 1.2V. The SRAM instances can be built with several aspect ratios for maximum area and performance optimization. Separate output (Q) and input (D) pins allow a write-through cycle feature. An asynchronous write-through mode (AWT) allows testing of interface shadow logic through scan. Built-in BIST interface allows for easy connection to most memBIST solutions. The special test modes allow externally bypassing read and write self-timed circuits and adjusting read and write margins. The SRAM compiler also includes a sub-word feature where selective write to each group of 8-bit sub-words can be done. A maskable write enable signal is provided for each 8-bit group.

Table 7-2 gives the range of permitted dual-port synchronous RAM configurations.

**Table 7-2.** Configuration Range

| Parameter | Min | Max | Increment |
|---|---|---|---|
| Address Locations (words) | 32 | 8K | 1 x CM(1) |
| Word Size (Number of I/O bits) | 2 | 128 | 1 bit |
| Total Bits in Core (Word Size x Address Locations) | 128 | 256K | |

Note: 1. CM = 4, 8, 16: Column Mux option

## 7.3 Via Programmable ROM

Key features of the via programmable ROM are:

- 1-port high-density synchronous via-2 programmable ROM
- 290 MHz worst-case cycle time (2K x 16) with no limitation on clock duty cycle
- Zero Quiescent Current
- 3-state outputs
- Several aspect ratios for optimization
- Programming support

The via programmable ROM compiler is a high-density low-power synchronous ROM compiler. The quiescent current consumption is zero when the ROM is not enabled. The compiler is optimized for a power supply voltage range of 1.62V to 1.98V and can operate at voltages as low as 1.26V. The ROM instances can be built with several aspect ratios for maximum area and performance optimization. Within limits, the user has flexibility in specifying the logical size of the ROM, including word size, number of address locations and column mux.

Table 7-3 gives the range of permitted via programmable ROM configurations.

**Table 7-3.** Configuration Range

| Parameter | Min | Max | Increment |
|---|---|---|---|
| Address Locations (words) | 256[2] | 64K | 4 x CM[1] |
| Word Size (Number of I/O bits) | 8 | 64 | 1 bit |
| Total Bits in Core (Word Size x Address Locations) | 2K | 1M | |

Notes: 1. CM = 16, 32, 64: Column Mux option
2. Min = 256 for CM = 16; min = 512 for CM = 32; min = 1K for CM = 64

## 7.4 Two-port Synchronous Register File

Key features of the two-port synchronous register file are:

- 2-Port (1R, 1W) high-speed/low-power Register File
- 500MHz worst-case cycle time for 32 words x 32 bits
- Zero Quiescent Current
- 3-state outputs
- Several aspect ratios for optimization
- Separate Data-in, Data-out pins
- Optional sub word write decode

The two-port synchronous register file compiler is a 2-port (1R, 1W) memory designed in 0.18-micron process. This is a high-speed/low-power synchronous register file compiler. The quiescent current consumption is zero when all Register File inputs (including CLKA and CLKB) are stable. The compiler is optimized for a power supply voltage range of 1.6V to 2.0V and can operate at voltages as low as 1.2V. The Register File instances can be built with several aspect ratios for maximum area and performance optimization. Separate clocks (CLKA, CLKB), output (QB), and input (DA) pins allow independent read and write cycles. Built-in BIST interface allows for easy connection to most memBIST solutions. The memory also includes a sub-word feature where selective write to each group of 2-, 4- or 8-bit sub-words can be done. A maskable write enable signal is optionally provided for each 2-, 4-, or 8-bit group. Within limits, the user has flexibility in specifying the logical size of the Register File, including word size, number of address locations and column mux.

Table 7-4 gives the range of permitted two-port synchronous register file configurations.

**Table 7-4.** Configuration Range

| Parameter | Min | Max | Increment |
|---|---|---|---|
| Address Locations (words) | 8 | 1024 | 1 x CM[1] |
| Word Size (Number of I/O bits) | 2[2] | 256 | 1 bit |
| Total Bits in Core (Word Size x Address Locations) | 16 | 16K | |

Notes: 1. CM = 1, 2, 4: Column Mux option
2. Minimum word size is 8 at column mux 4.

# 8. Revision History

**Table 8-1.** Revision History

| Document Ref. | Comments | Change Request Ref. |
|---|---|---|
| 1389AS | First issue. | |
| 1389BS | Reformatted. | |
| 1389CS | Added Table 1-2, “Absolute Maximum Ratings,” on page 2. | |

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