Low Noise, Low Power, I^2C® Bus, 128 Taps, Wiper Only

The ISL22319 integrates a single digitally controlled potentiometer (DCP) and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^2C bus interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power up the device recalls the content of the DCP's IVR to the WR.

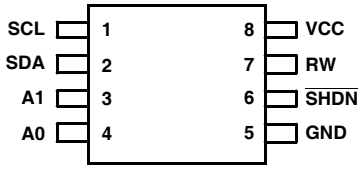
The DCP can be used as a voltage divider in a wide variety of applications including control, parameter adjustments, AC measurement and signal processing.

Features

- 128 resistor taps
- I^2C serial interface
  - Two address pins, up to four devices/bus
- Non-volatile storage of wiper position
- Wiper resistance: 70Ω typical @ 3.3V
- Shutdown mode
- Shutdown current 5µA max
- Power supply: 2.7V to 5.5V
- 50kΩ or 10kΩ total resistance
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ $T \leq 55$ °C
- 8 Ld MSOP
- Pb-free plus anneal product (RoHS compliant)

Pinout

ISL22319
(8 LD MSOP)
TOP VIEW



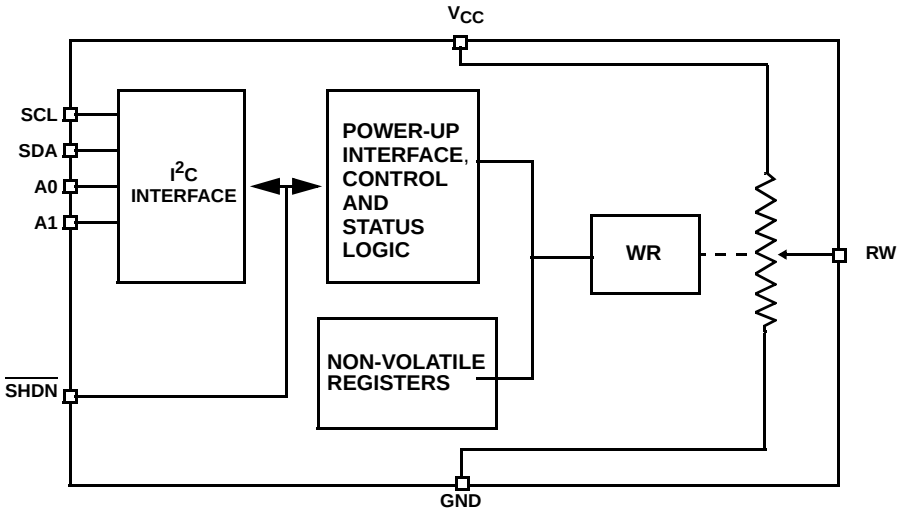
Ordering Information

PART NUMBER	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL22319UFU8Z (Notes 1, 2)	319UZ	50	-40 to +125	8 Ld MSOP (Pb-Free)	M8.118
ISL22319WFU8Z (Notes 1, 2)	319WZ	10	-40 to +125	8 Ld MSOP (Pb-Free)	M8.118

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-TK" suffix for 1,000 Tape and Reel option

Block Diagram



Pin Descriptions

MSOP PIN	SYMBOL	DESCRIPTION
1	SCL	Open drain I^2C interface clock input
2	SDA	Open drain serial data I/O for the I^2C interface
3	A1	Device address input for the I^2C interface
4	A0	Device address input for the I^2C interface
5	GND	Device ground pin
6	$\overline{SHDN}$	Shutdown active low input
7	RW	“Wiper” terminal of DCP
8	V_{CC}	Power supply pin

Absolute Maximum Ratings

Storage Temperature . . . . . .-65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . . .-0.3V to V_{CC}+0.3
V_{CC} . . . . . .-0.3V to +6V
Voltage at any DCP Pin with
respect to GND. . . . . -0.3V to V_{CC}
Lead Temperature (Soldering, 10s) . . . . . .300°C
I_W (10s) . . . . . ±6mA
Latchup (Note 4) . . . . . Class II, Level B @+125°C
ESD (HBM) 5kV
(CDM) 1kV

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
10 Lead MSOP.	130

Maximum Junction Temperature (Plastic Package). . . . . .150°C

Recommended Operating Conditions

Ambient Temperature (Extended Industrial) . . . . . .-40°C to 125°C
V_{CC} Voltage for DCP Operation . . . . . 2.7V to 5.5V
Wiper Current . . . . . -3mA to 3mA
Power Rating 5mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5V on the SHDN pin, and using a max negative pulse of -1V for all pins.

Analog Specifications Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
R_{TOTAL}	End-to-End Resistance	W option		10		kΩ
		U option		50		kΩ
	End-to-End Resistance Tolerance		-20		+20	%
	End-to-End Temperature Coefficient	W option		±50		ppm/°C (Note 14)
		U option		±80		ppm/°C (Note 14)
R_W (Note 14)	Wiper Resistance	V_{CC} = 3.3V @ 25°C, wiper current = V_{CC}/R_{TOTAL}		70		Ω
C_W (Note 14)	Wiper Capacitance			25		pF
I_{LkgRW}	Leakage on RW Pin	Voltage at pin from GND to V_{CC}		2	4	µA
VOLTAGE DIVIDER MODE (measured at R_W, unloaded)						
INL (Note 10)	Integral Non-linearity		-1		1	LSB (Note 6)
DNL (Note 9)	Differential Non-linearity	Monotonic over all tap positions	-0.5		0.5	LSB (Note 6)
ZSerror (Note 7)	Zero-scale Error	W option	0	1	5	LSB (Note 6)
		U option	0	0.5	2	
FSerror (Note 8)	Full-scale Error	W option	-5	-1	0	LSB (Note 6)
		U option	-2	-1	0	
TC_V (Note 11, 14)	Ratiometric Temperature Coefficient	DCP register set to 40 hex		±4		ppm/°C

Operating Specifications Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	10k DCP, f_{SCL} = 400kHz; (for I^2C active, read and write states)			1	mA
	V_{CC} Supply Current (volatile write/read, non-volatile read)	50k DCP, f_{SCL} = 400kHz; (for I^2C active, read and write states)			0.5	mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	10k DCP, f_{SCL} = 400kHz; (for I^2C active, read and write states)			3.2	mA
	V_{CC} Supply Current (non-volatile write/read)	50k DCP, f_{SCL} = 400kHz; (for I^2C active, read and write states)			2.7	mA
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V , 10k DCP, I^2C interface in standby state			850	µA
		V_{CC} = +3.6V, 10k DCP, I^2C interface in standby state			550	µA
		V_{CC} = +5.5V, 50k DCP, I^2C interface in standby state			160	µA
		V_{CC} = +3.6V, 50k DCP, I^2C interface in standby state			100	µA
I_{SD}	V_{CC} Current (shutdown)	V_{CC} = +5.5V @ +85°C, I^2C interface in standby state			3	µA
		V_{CC} = +5.5V @ +125°C, I^2C interface in standby state			5	µA
		V_{CC} = +3.6V @ +85°C, I^2C interface in standby state			2	µA
		V_{CC} = +3.6V @ +125°C, I^2C interface in standby state			4	µA
I_{LkgDig}	Leakage Current, at Pins A0, A1, $\overline{SHDN}$, SDA, and SCL	Voltage at pin from GND to V_{CC}	-1		1	µA
t_{DCP} (Note 14)	DCP Wiper Response Time	SCL falling edge of last bit of DCP data byte to wiper new position		1.5		µs
$t_{ShdnRec}$ (Note 14)	DCP Recall Time from Shutdown Mode	From rising edge of $\overline{SHDN}$ signal to wiper stored position and RH connection		1.5		µs
		SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection		1.5		µs
Vpor	Power-on Recall Voltage	Minimum V_{CC} at which memory recall occurs	2.0		2.6	V
V_{CC} Ramp	V_{CC} Ramp Rate		0.2			V/ms
t_D	Power-up Delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			3	ms
EEPROM SPECIFICATION						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤ 55 °C	50			Years
t_{WC} (Note 15)	Non-volatile Write Cycle Time			12	20	ms
SERIAL INTERFACE SPECS						
V_{IL}	A1, A0, $\overline{SHDN}$, SDA, and SCL Input Buffer LOW Voltage		-0.3		0.3*V_{CC}	V
V_{IH}	A1, A0, $\overline{SHDN}$, SDA, and SCL Input Buffer HIGH Voltage		0.7*V_{CC}		V_{CC}+0.3	V

Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

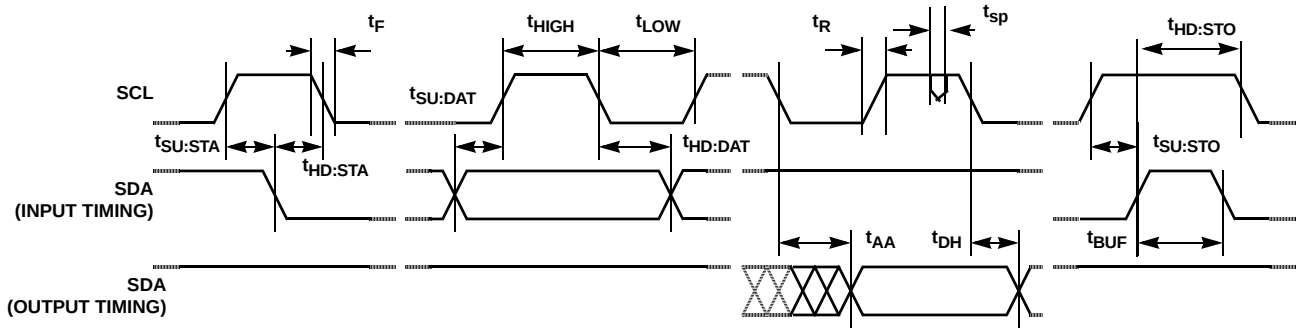
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
Hysteresis	SDA and SCL Input Buffer Hysteresis		0.05* V_{CC}			V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin	A1, A0, $\overline{SHDN}$, SDA, and SCL Pin Capacitance				10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{sp}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			900	ns
t_{BUF}	Time the Bus Must be Free before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	1300			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2~2.5kΩ For Cb = 40pF, max is about 15~20kΩ	1			kΩ
$t_{SU:A}$	A1 and A0 Setup Time	Before START condition	600			ns
$t_{HD:A}$	A1 and A0 Hold Time	After STOP condition	600			ns

NOTES:

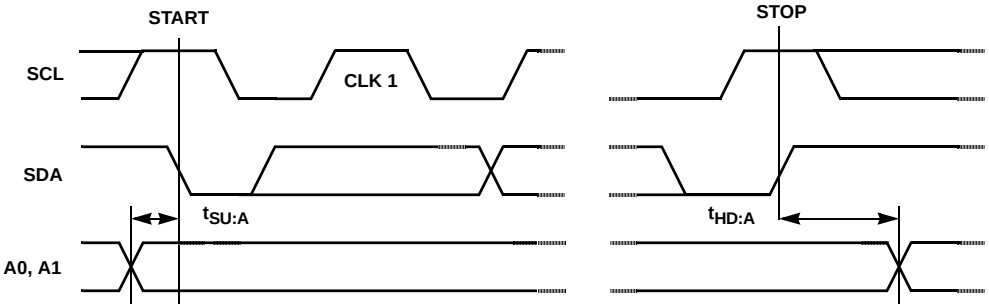
5. Typical values are for T_A = 25°C and 3.3V supply voltage.
6. LSB: $[V(R_W)_{127} – V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
7. ZS error = $V(RW)_0$/LSB.

8. FS error = $[V(RW)_{127} – V_{CC}]$/LSB.
9. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 127. i is the DCP register setting.
10. INL = $[V(RW)_i – (i • LSB) – V(RW)_0]$/LSB for i = 1 to 127
11. $TC_V = \frac{Max(V(RW)_i) – Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{165°C}$ for i = 16 to 127 decimal, T = -40°C to 125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
12. MI = $|RW_{127} – RW_0|$/127. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
13. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{127}/MI, when measuring between RW and RH.
14. This parameter is not 100% tested.
15. t_{WC} is the time from a valid STOP condition at the end of a Write sequence of I2C serial interface, to the end of the self-timed internal non-volatile write cycle.

SDA vs SCL Timing



A0 and A1 Pin Timing



Typical Performance Curves

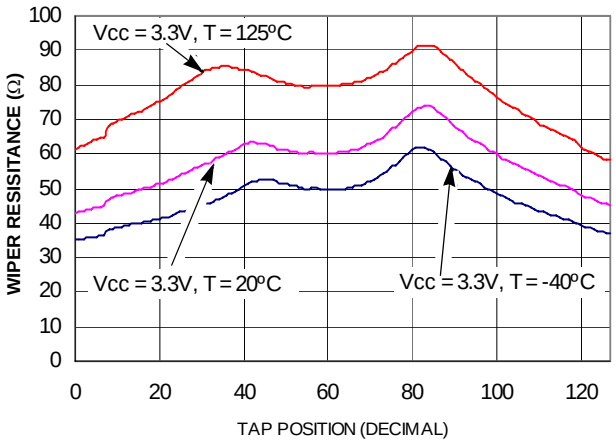


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

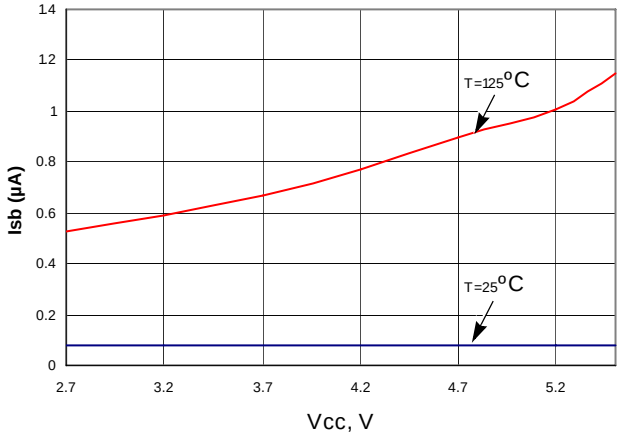


FIGURE 2. STANDBY I_{CC} vs V_{CC}

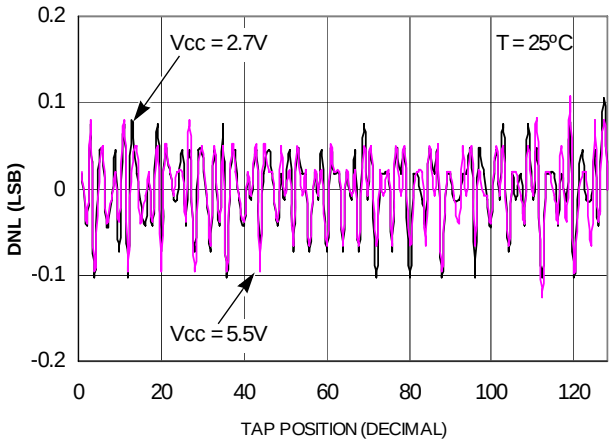


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

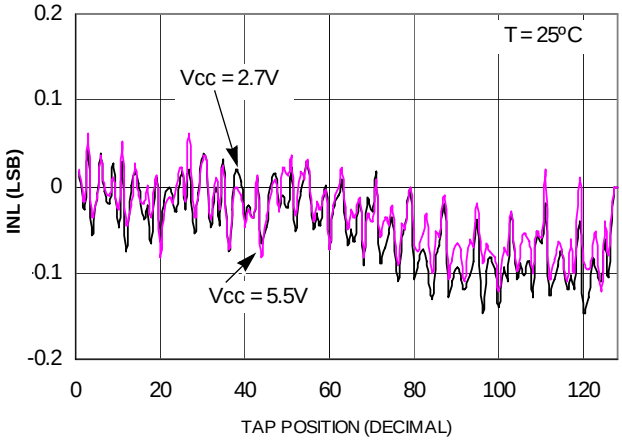


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

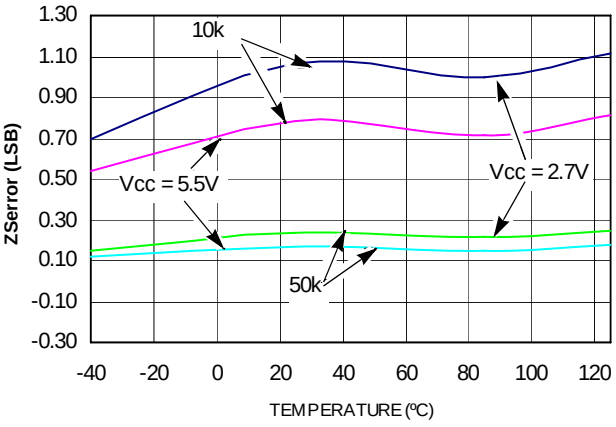


FIGURE 5. ZSerror vs TEMPERATURE

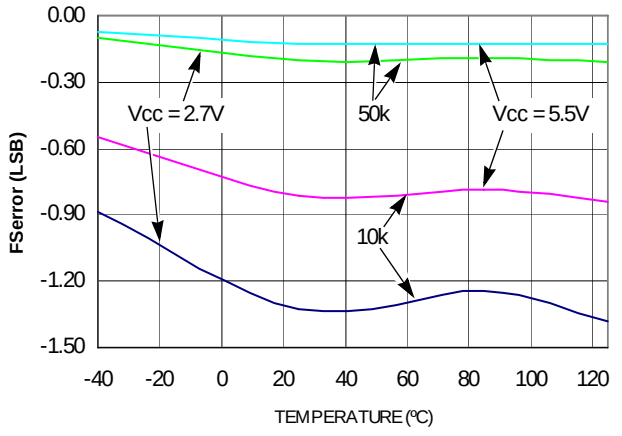


FIGURE 6. FSerror vs TEMPERATURE

Typical Performance Curves (Continued)

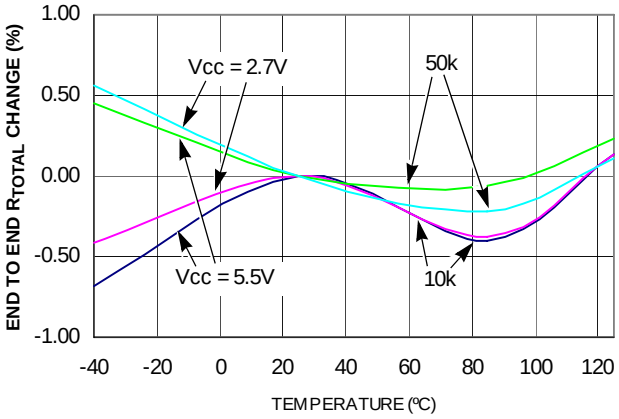


FIGURE 7. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

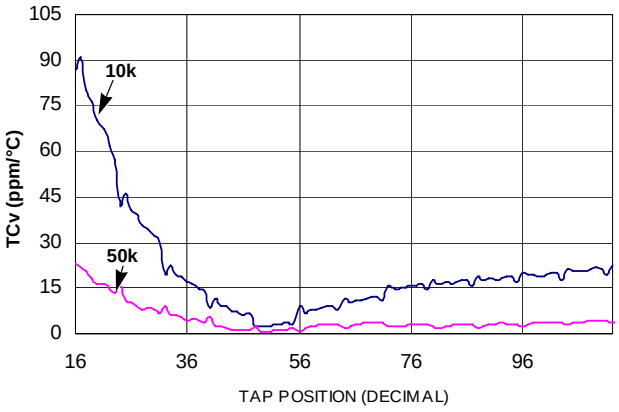


FIGURE 8. TC FOR VOLTAGE DIVIDER MODE IN ppm

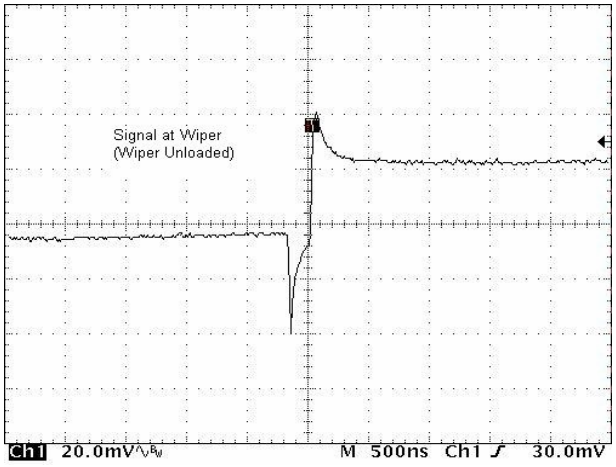


FIGURE 9. MIDSCALE GLITCH, CODE 3Fh TO 40h

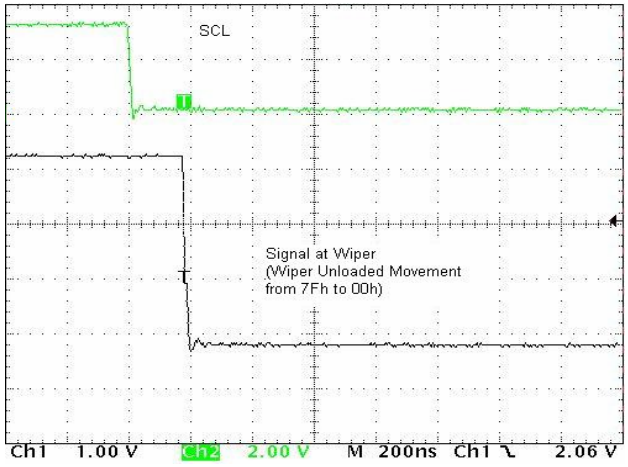


FIGURE 10. LARGE SIGNAL SETTLING TIME

Pin Description

Potentiometers Pins

RW

RW is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

$\overline{SHDN}$

The active low $\overline{SHDN}$ pin forces the resistor to end-to-end open circuit condition and shorts RWi to GND. When $\overline{SHDN}$ is returned to logic high, the previous latch settings put RW at the same resistance setting prior to shutdown. This pin is logically OR'd with SHDN bit in ACR register. I^2C interface is still available in shutdown mode and all registers are accessible. This pin must remain HIGH for normal operation.

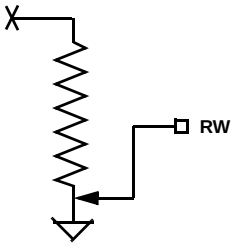


FIGURE 11. DCP CONNECTION IN SHUTDOWN MODE

Bus Interface Pins

Serial Data Input/Output (SDA)

The SDA is a bidirectional serial data input/output pin for I^2C interface. It receives device address, operation code, wiper address and data from an I^2C external master device at the

rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

Serial Clock (SCL)

This is the serial clock input of the I2C serial interface. SCL requires an external pull-up resistor, since it is an open drain input.

Device Address (A1, A0)

The address inputs are used to set the least significant 2 bits of the 7-bit I^2C interface slave address. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL22319. A maximum of 4 ISL22319 devices may occupy the I^2C serial bus.

Principles of Operation

The ISL22319 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory and an I^2C serial interface providing direct communication between a host and the potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVR will be maintained in the non-volatile memory. When power is restored, the contents of the IVR is recalled and loaded into the WR to set the wiper to the initial value.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer and internally connected to V_{CC} and GND. The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 7-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR[6:0]= 00h), its wiper terminal (RW) is closest to GND. When the WR register of a DCP contains all ones (WR[6:0]= 7Fh), its wiper terminal (RW) is closest to V_{CC}. As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to GND to the closest to V_{CC}.

While the ISL22319 is being powered up, the WR is reset to 40h (64 decimal), which locates RW roughly at the center between V_{CC} and GND. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WR will be reload with the value stored in a non-volatile Initial Value Register (IVR).

The WR and IVR can be read or written to directly using the I^2C serial interface as described in the following sections.

Memory Description

The ISL22319 contains one non-volatile 8-bit register, known as the Initial Value Register (IVR), and two volatile 8-bit registers, Wiper Register (WR) and Access Control Register (ACR). The memory map of ISL22319 is on Table 1. The non-volatile register (IVR) at address 0, contains initial wiper position and volatile register (WR) contains current wiper position.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
2	—	ACR
1	Reserved	
0	IVR	WR

The non-volatile IVR and volatile WR registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described below in Table 2.

The VOL bit (ACR[7]) determines whether the access is to wiper registers WR or initial value registers IVR.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

VOL	SHDN	WIP	0	0	0	0	0

If VOL bit is 0, the non-volatile IVR register is accessible. If VOL bit is 1, only the volatile WR is accessible. Note, value is written to IVR register also is written to the WR. The default value of this bit is 0.

The SHDN bit (ACR[6]) disables or enables Shutdown mode. This bit is logically OR ‘d with $\overline{SHDN}$ pin. When this bit is 0, DCP is in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR[5]) is read only bit. It indicates that nonHvolatile write operation is in progress. It is impossible to write to the WR or ACR while WIP bit is 1.

I^2C Serial Interface

The ISL22319 supports an I^2C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22319 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 12). On power-up of the ISL22319 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22319 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 12). A START condition is ignored during the powerHup of the device.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 12). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 13).

The ISL22319 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22319 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following two bits matching the logic values present at pins A1 and A0. The LSB is the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation (See Table 3).

TABLE 3. IDENTIFICATION BYTE FORMAT

					Logic values at pins A1 and A0 respectively		
0	1	0	1	0	A1	A0	R/$\overline{\text{W}}$
(MSB)							(LSB)

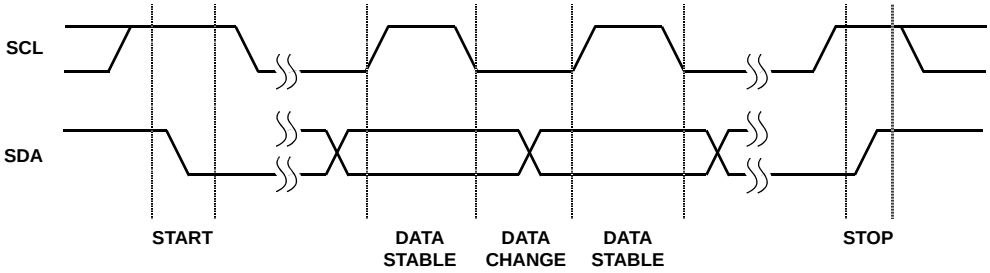


FIGURE 12. VALID DATA CHANGES, START, AND STOP CONDITIONS

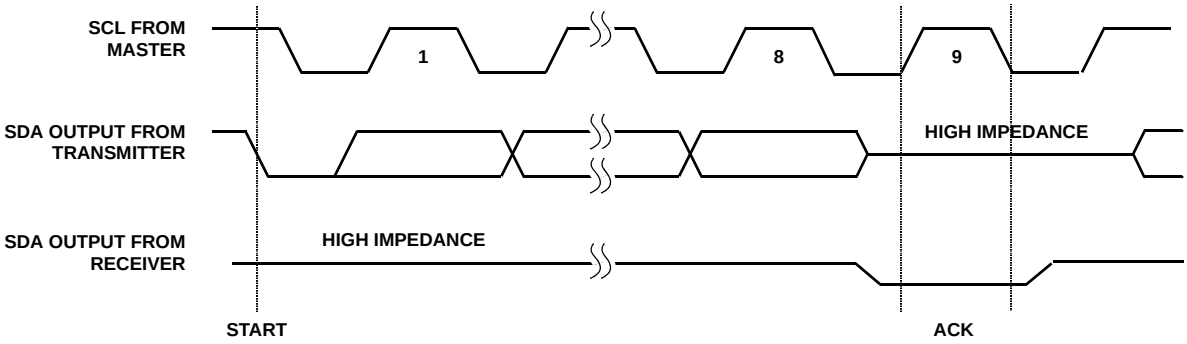


FIGURE 13. ACKNOWLEDGE RESPONSE FROM RECEIVER

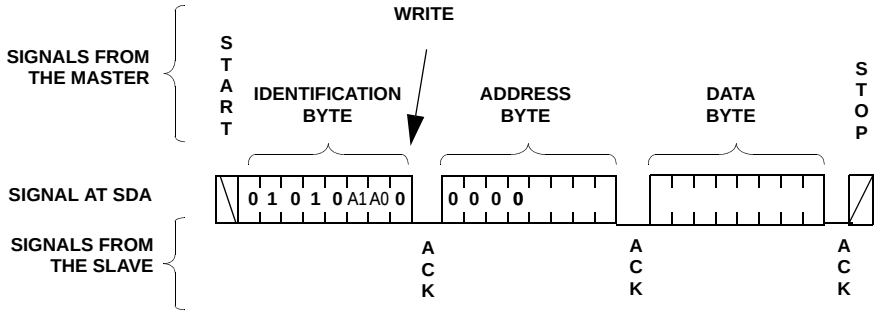


FIGURE 14. BYTE WRITE SEQUENCE

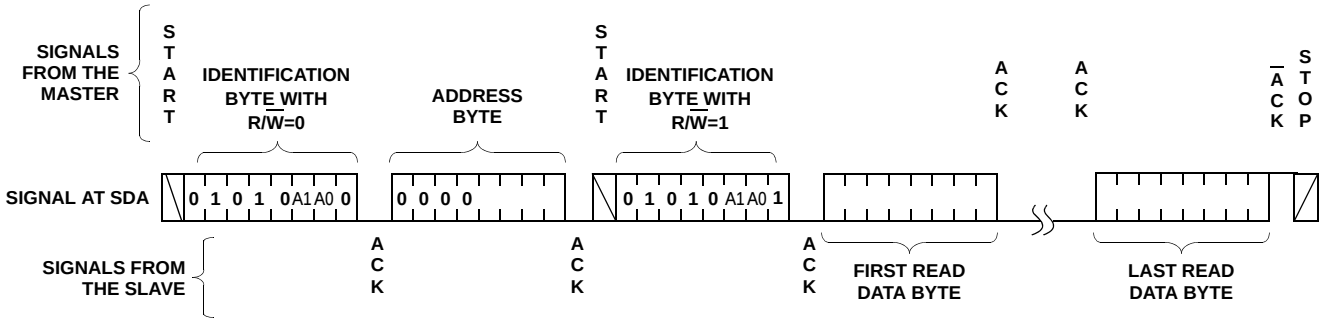


FIGURE 15. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22319 responds with an ACK. At this time, the device enters its standby state (See Figure 14).

The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (See Figure 15). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL22319 responds with an ACK. Then the ISL22319 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a $\overline{ACK}$ and STOP condition) following the last bit of the last Data Byte (See Figure 15).

In order to read back the non-volatile IVR, it is recommended that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

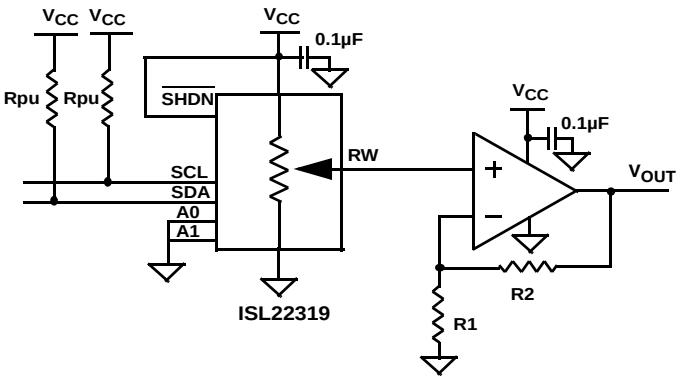
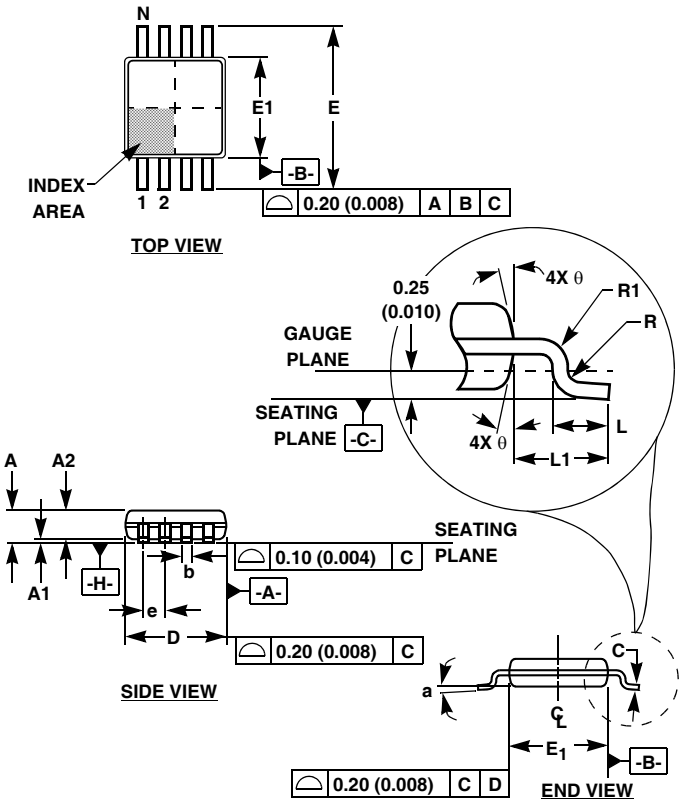


FIGURE 16. TYPICAL APPLICATION DIAGRAM FOR IMPLEMENTING ADJUSTABLE VOLTAGE REFERANCE

Applications Information

The typical application diagram is shown on Figure 16. For proper operation adding 0.1µF decoupling ceramic capacitor to V_{CC} is recommended. The capacitor value may vary based on expected noise frequency of the design.

Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.