

ZXMN3F31DN8

30V SO8 dual N-channel enhancement mode MOSFET

Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.024 @ $V_{GS} = 10V$	7.3
	0.039 @ $V_{GS} = 4.5V$	5.7



Description

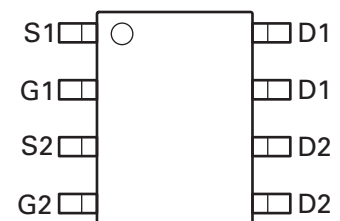
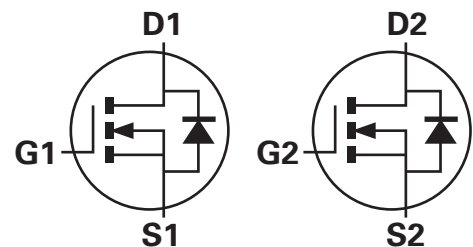
This new generation Trench MOSFET from Zetex features low on-resistance achievable with 4.5V gate drive.

Features

- Low on-resistance
- 4.5V gate drive capability

Applications

- DC-DC Converters
- Power management functions
- Load switching
- Motor control
- Back lighting



Ordering information

DEVICE	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN3F31DN8TA	7	12	500

Device marking

ZXMN

3F31D

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Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain source voltage	V_{DSS}	30	V
Gate source voltage	V_{GS}	± 20	V
Continuous Drain Current @ $V_{GS}=10$; $T_A=25^{\circ}\text{C}^{(b)}$ @ $V_{GS}=10$; $T_A=70^{\circ}\text{C}^{(b)}$ @ $V_{GS}=10$; $T_A=25^{\circ}\text{C}^{(a)}$	I_D	7.3 5.9 5.7	A A A
Pulsed drain current ^(c)	I_{DM}	33	A
Continuous source current (body diode) ^(b)	I_S	3	A
Pulsed source current (body diode) ^(c)	I_{SM}	33	A
Power dissipation at $T_A=25^{\circ}\text{C}^{(a)(d)}$ Linear derating factor	P_D	1.25 10	W mW/ $^{\circ}\text{C}$
Power dissipation at $T_A=25^{\circ}\text{C}^{(a)(e)}$ Linear derating factor	P_D	1.8 14	W mW/ $^{\circ}\text{C}$
Power dissipation at $T_A=25^{\circ}\text{C}^{(b)(d)}$ Linear derating factor	P_D	2.1 17	W mW/ $^{\circ}\text{C}$
Operating and storage temperature range	T_j, T_{stg}	-55 to 150	$^{\circ}\text{C}$

Thermal resistance

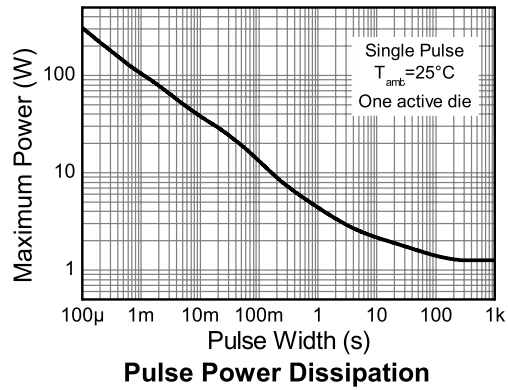
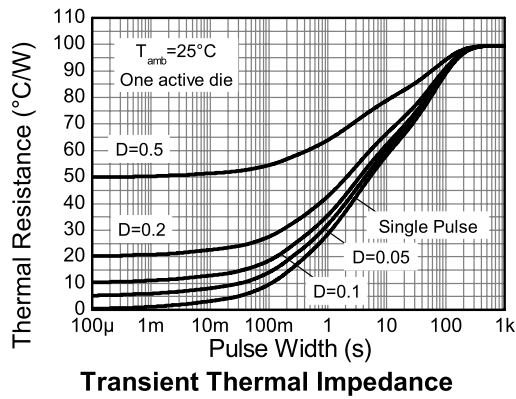
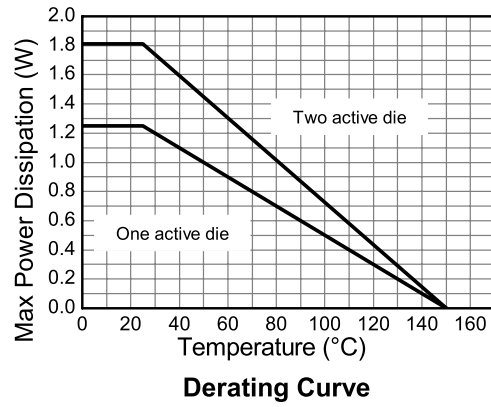
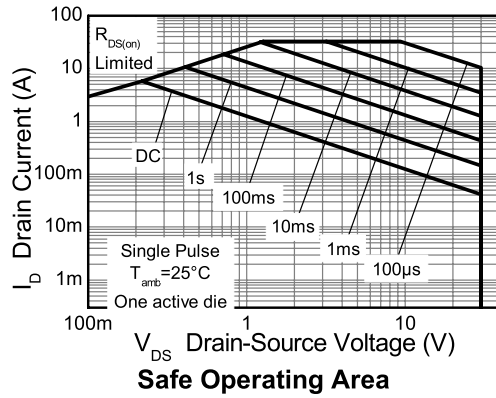
Parameter	Symbol	Limit	Unit
Junction to ambient ^{(a)(d)}	$R_{\theta JA}$	100	$^{\circ}\text{C/W}$
Junction to ambient ^{(a)(e)}	$R_{\theta JA}$	70	$^{\circ}\text{C/W}$
Junction to ambient ^{(b)(d)}	$R_{\theta JA}$	60	$^{\circ}\text{C/W}$
Junction to lead ^(f)	$R_{\theta JL}$	53	$^{\circ}\text{C/W}$

NOTES:

- (a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 PCB measured at $t \leq 10$ sec.
- (c) Repetitive rating - 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300 μs - pulse width limited by maximum junction temperature.
- (d) For a dual device with one active die.
- (e) For a device with two active die running at equal power.
- (f) Thermal resistance from junction to solder-point (at end of drain lead).

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Thermal characteristics



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Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	30			V	I _D = 250μA, V _{GS} =0V
Zero Gate Voltage Drain Current	I _{DSS}			0.5	μA	V _{DS} = 30V, V _{GS} =0V
Gate-Body Leakage	I _{GSS}			100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-Source Threshold Voltage	V _{GS(th)}	1.0		3.0	V	I _D = 250μA, V _{DS} =V _{GS}
Static Drain-Source On-State Resistance ^(*)	R _{DS(on)}			0.024 0.039	Ω Ω	V _{GS} = 10V, I _D = 7.0A V _{GS} = 4.5V, I _D = 6.0A
Forward Transconductance ^(*) (†)	g _{fs}		16.5		S	V _{DS} = 15V, I _D = 7A
Dynamic ^(†)						
Input Capacitance	C _{iss}		608		pF	V _{DS} = 15V, V _{GS} =0V f=1MHz
Output Capacitance	C _{oss}		132		pF	
Reverse Transfer Capacitance	C _{rss}		71		pF	
Switching ^(‡) (†)						
Turn-On-Delay Time	t _{d(on)}		2.9		ns	V _{DD} = 15V, I _D = 1A R _G ≅ 6.0Ω, V _{GS} =10V
Rise Time	t _r		3.3		ns	
Turn-Off Delay Time	t _{d(off)}		16		ns	
Fall Time	t _f		8		ns	
Total Gate Charge	Q _g		12.9		nC	V _{DS} = 15V, V _{GS} = 10V I _D = 7A
Gate-Source Charge	Q _{gs}		2.5		nC	
Gate Drain Charge	Q _{gd}		2.52		nC	
Source-drain diode						
Diode Forward Voltage ^(*)	V _{SD}		0.82	1.2	V	T _j =25°C, I _S = 1.7A, V _{GS} =0V

NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

(†) For design aid only, not subject to production testing

(‡) Switching characteristics are independent of operating junction temperature.

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Typical characteristics

Fig1. $I_D - V_{DS}$

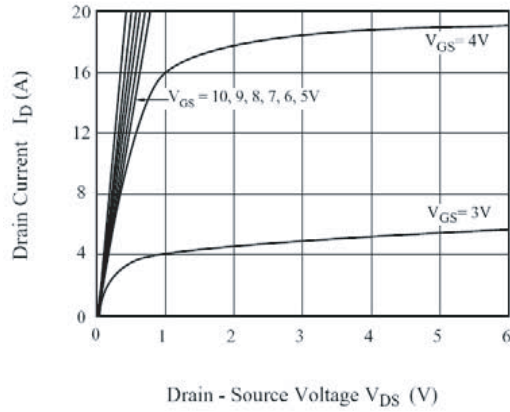


Fig2. $I_D - V_{GS}$

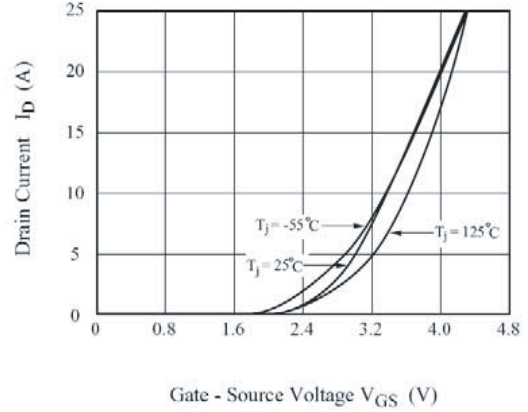


Fig3. $V_{th} - T_J$

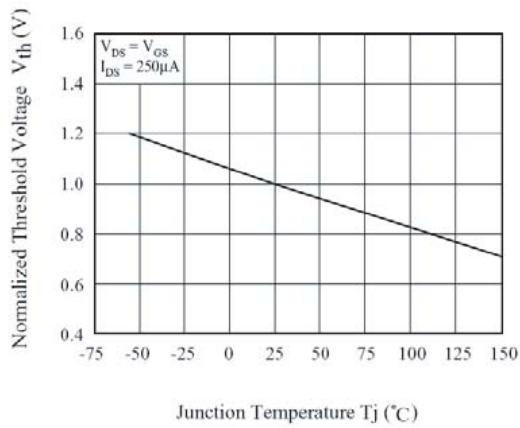


Fig4. $I_{DR} - V_{SD}$

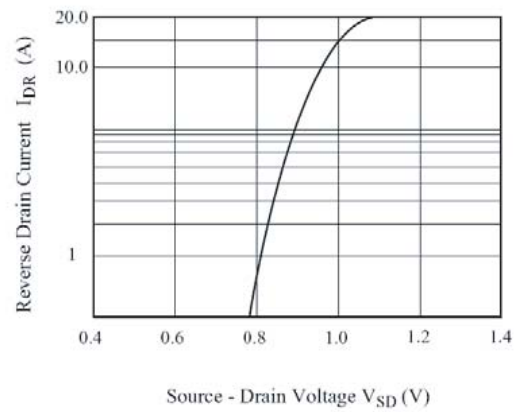
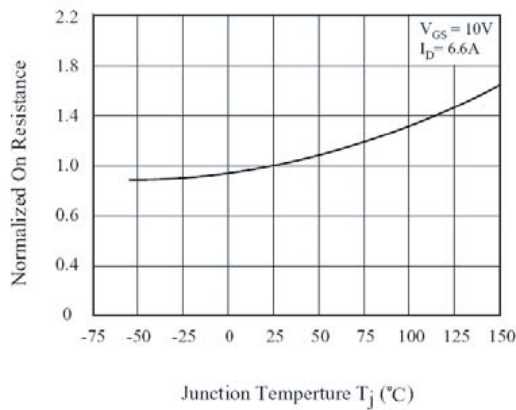
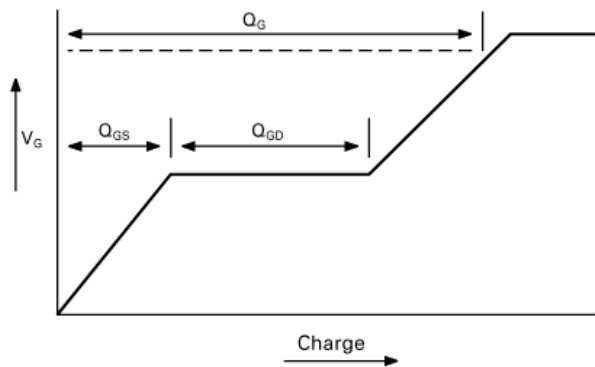


Fig5. $R_{DS(ON)} - T_J$

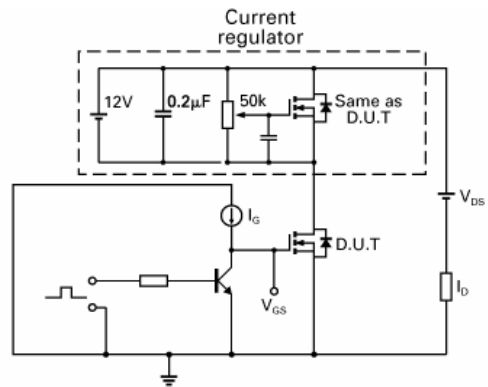


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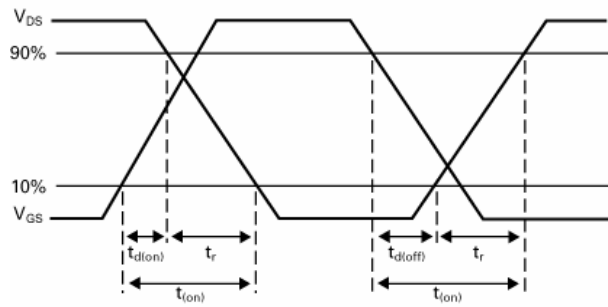
Test circuits



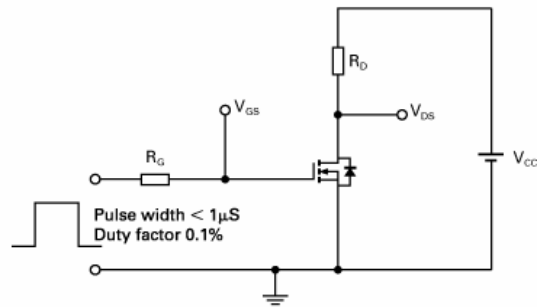
Basic gate charge waveform



Gate charge test circuit



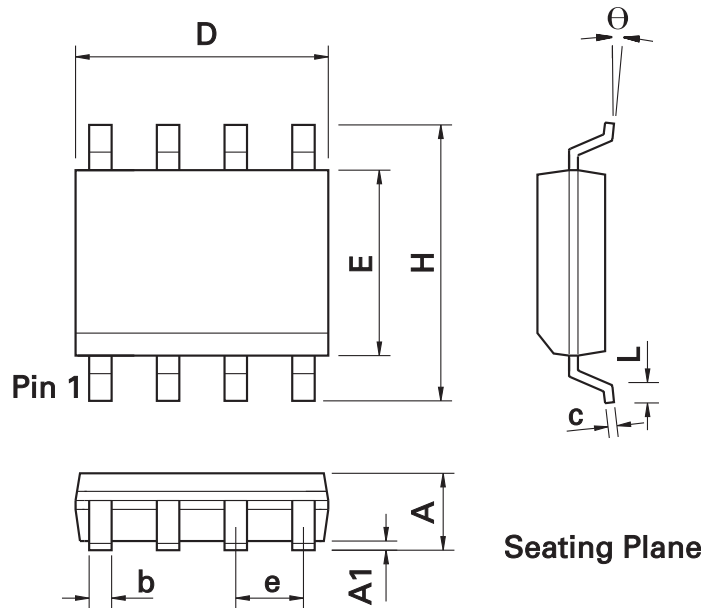
Switching time waveforms



Switching time test circuit

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Package outline - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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