



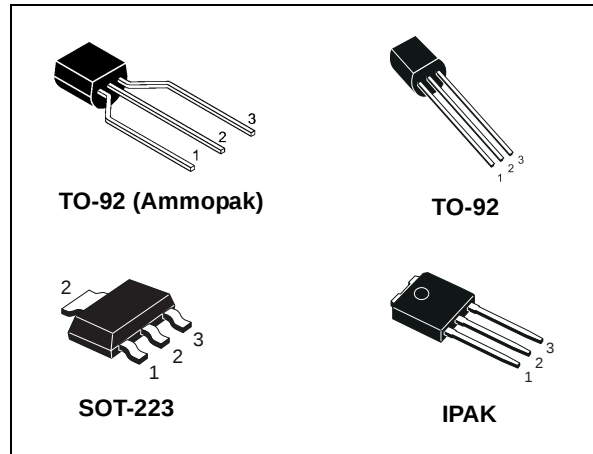
STD1LNK60Z-1 STQ1NK60ZR - STN1NK60Z

N-CHANNEL 600V - 13Ω - 0.8A - TO-92 - IPAK - SOT-223
Zener-Protected SuperMESH™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _W
STD1LNK60Z-1	600V	<15Ω	0.8A	25W
STQ1NK60ZR	600V	<15Ω	0.3A	3W
STN1NK60Z	600V	<15Ω	0.3A	3.3W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- ESD improved capability
- New high voltage benchmark



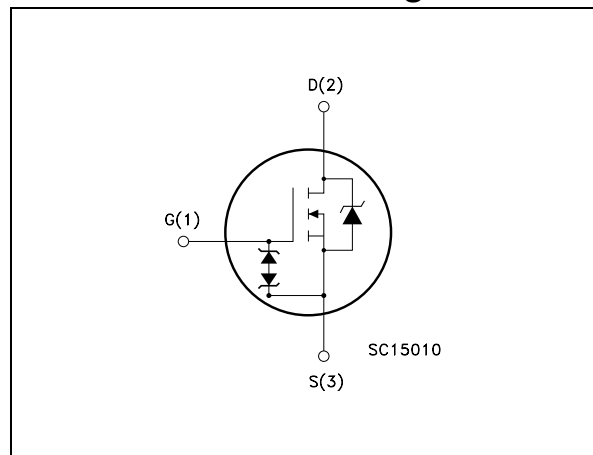
Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Applications

- Switching application

Internal schematic diagram



Order codes

Sales Type	Marking	Package	Packaging
STD1LNK60Z-1	D1LNK60Z	IPAK	TUBE
STQ1NK60ZR	Q1NK60ZR	TO-92	BULK
STQ1NK60ZR-AP	Q1NK60ZR	TO-92	AMMOPAK
STN1NK60Z	1NK60Z	SOT-223	TAPE & REEL

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		IPAK	TO-92	SOT-223	
V_{DS}	Drain-Source Voltage ($V_{GS} = 0$)	600			V
V_{DGR}	Drain-Gate Voltage ($R_{GS} = 20K\Omega$)	600			V
V_{GS}	Gate-Source Voltage	± 30			V
I_D	Drain Current (continuous) at $T_C = 25^\circ C$	0.8	0.3	0.3	A
I_D	Drain Current (continuous) at $T_C = 100^\circ C$	0.5	0.189		A
$I_{DM}^{(1)}$	Drain Current (pulsed)	3.2	1.2		A
P_{TOT}	Total Dissipation at $T_C = 25^\circ C$	25	3	3.3	W
	Derating Factor	0.24	0.25	0.26	W/°C
$V_{ESD(G-D)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	800			V
$dv/dt^{(2)}$	Peak Diode Recovery voltage slope	4.5			V/ns
T_J T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150			°C

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 0.3A$, $di/dt \leq 200A/\mu s$, $V_{DD} = 80\%V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value			Unit
		IPAK	TO-92	SOT-223	
$R_{thj-case}$	Thermal resistance junction-case Max	5	--	--	°C/W
R_{thj-a}	Thermal resistance junction-ambient Max	100	120	37.87 ⁽¹⁾	°C/W
$R_{thj-lead}$	Thermal resistance junction-lead Max	--	40	--	°C/W
T_I	Maximum lead temperature for soldering purpose	275	260		°C

1. When mounted on 1 inch² FR-4 board, 2 Oz Cu

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche Current, Repetitive or Noy-Repetitive (pulse width limited by T_J Max)	0.8	A
E_{AS}	Single pulse avalanche Energy (starting $T_J = 25^\circ C$, $I_d = I_{AR}$, $V_{dd} = 50V$)	60	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 1mA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating, V _{DS} = MaxRating @125°C			1 50	μA μA
I _{GSS}	Gate Body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 50μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10V, I _D = 0.4A		13	15	Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward Transconductance	V _{DS} = 15V, I _D = 0.4A		0.5		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		94 17.6 2.8		pF pF pF
C _{oss eq} ⁽²⁾	Equivalent Output Capacitance	V _{GS} = 0, V _{DS} = 0V to 480V		11		pF
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 480V, I _D = 0.8A V _{GS} = 10V (see Figure 11)		4.9 1 2.7	6.9	nC nC nC

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

2. C_{oss eq} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=300\text{ V}$, $I_D=0.4\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 19)		5.5		ns
t_r	Rise Time			5		ns
$t_{d(off)}$	Turn-off Delay Time			13		ns
t_f	Fall Time			28		ns

Table 7. Source drain diode

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain Current				0.8	A
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)				2.4	A
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=0.8\text{ A}$, $V_{GS}=0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD}=0.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=25^\circ\text{C}$		135		ns
Q_{rr}	Reverse Recovery Charge			216		nC
I_{RRM}	Reverse Recovery Current			3.2		A
t_{rr}	Reverse Recovery Time	$I_{SD}=0.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150^\circ\text{C}$		140		ns
Q_{rr}	Reverse Recovery Charge			224		nC
I_{RRM}	Reverse Recovery Current			3.2		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 8. Gate-source zener diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source Breakdown Voltage	$I_{GS}=\pm 1\text{ mA}$ (Open Drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for IPAK

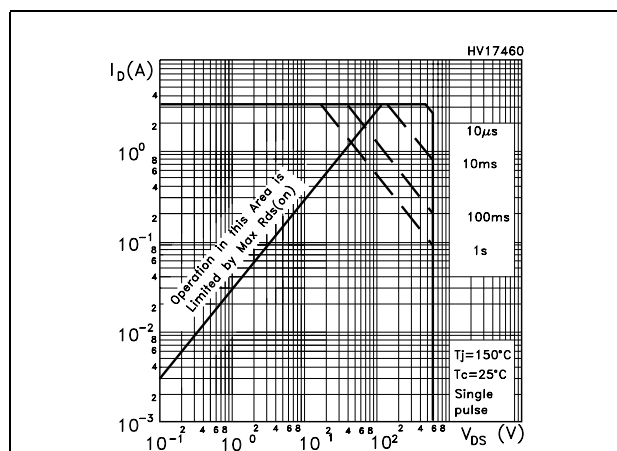


Figure 2. Thermal impedance for IPAK

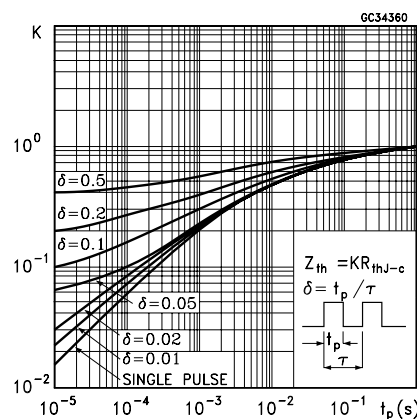


Figure 3. Safe operating area for TO-92

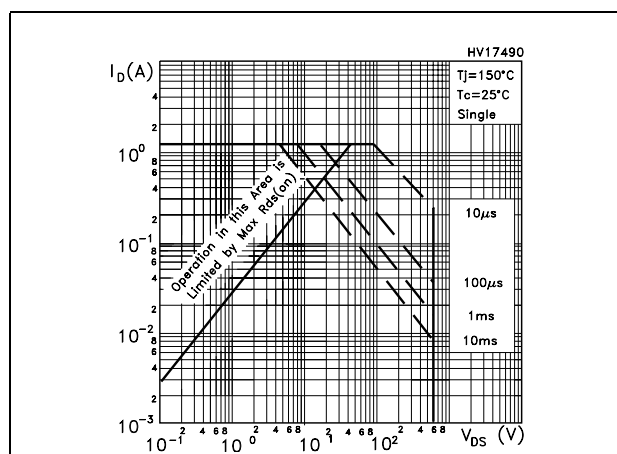


Figure 4. Thermal impedance for TO-92

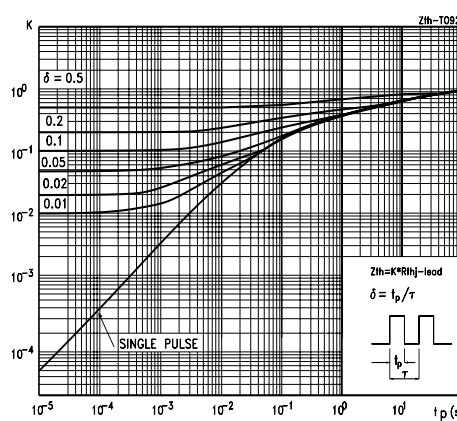


Figure 5. Safe operating area for SOT-223

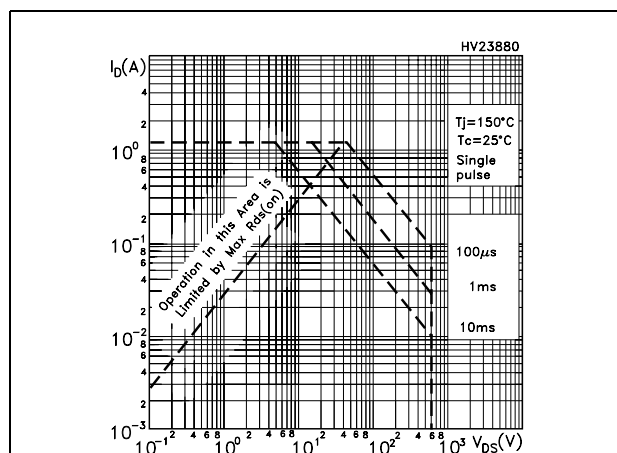


Figure 6. Thermal impedance for SOT-223

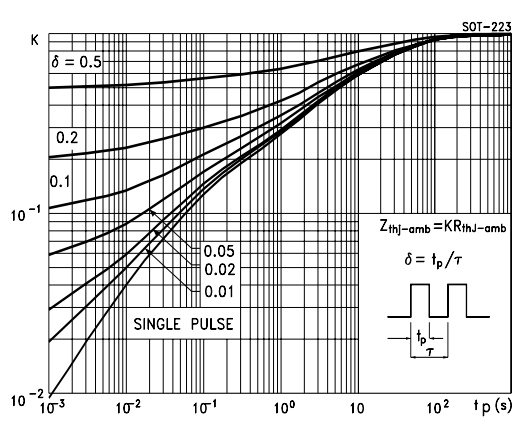


Figure 7. Output characteristics

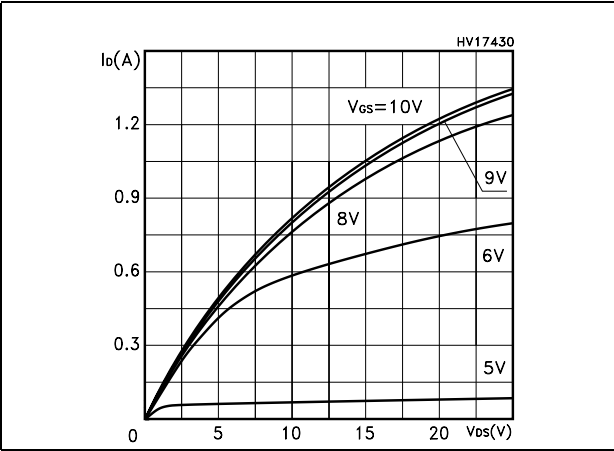


Figure 8. Transfer characteristics

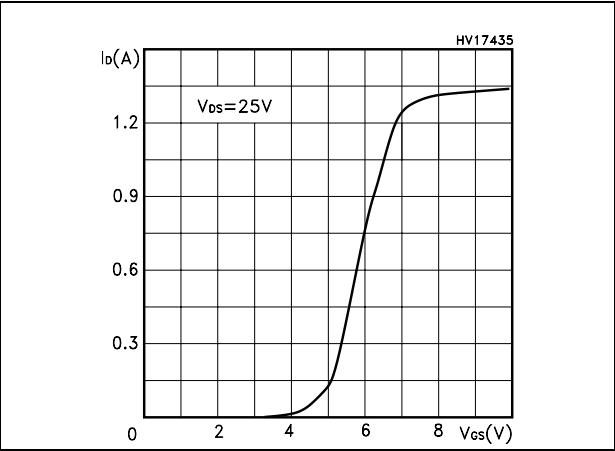


Figure 9. Transconductance

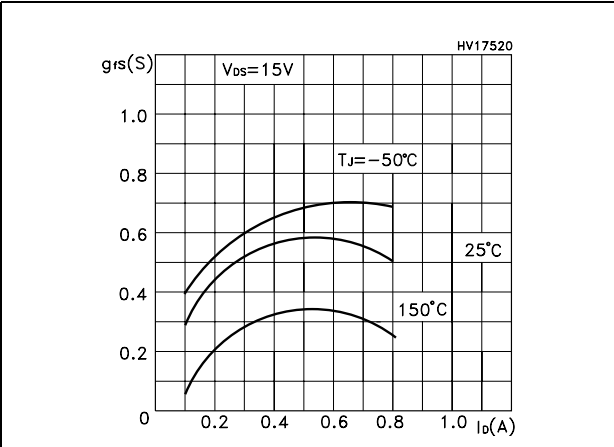


Figure 10. Static drain-source on resistance

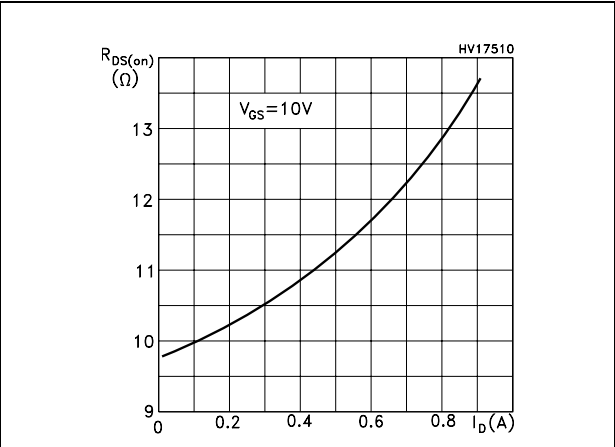


Figure 11. Gate charge vs gate-source voltage

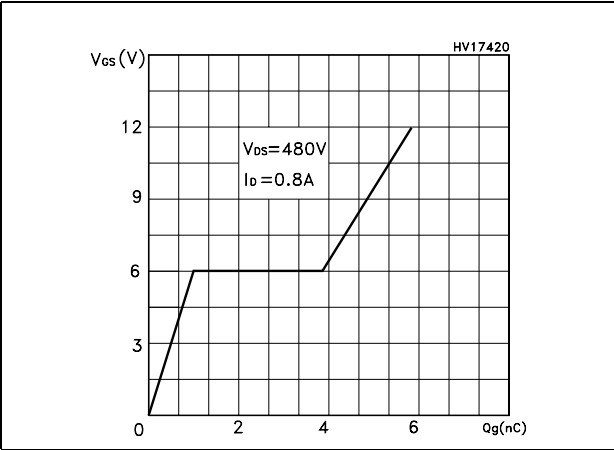


Figure 12. Capacitance variations

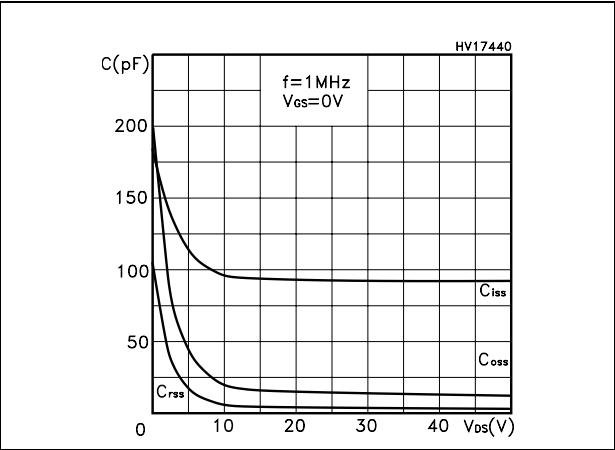


Figure 13. Normalized gate threshold voltage vs temperature

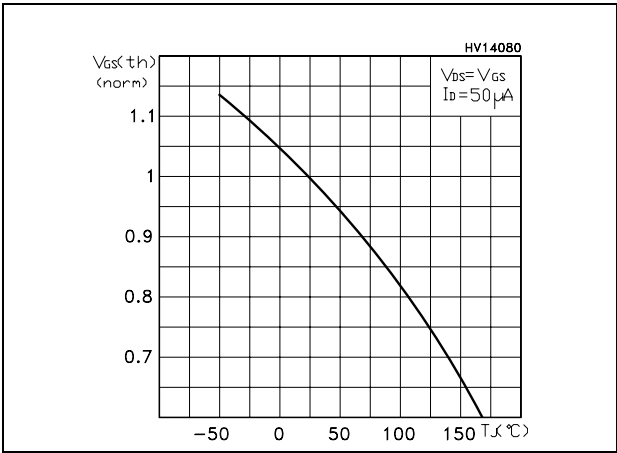


Figure 14. Normalized on resistance vs temperature

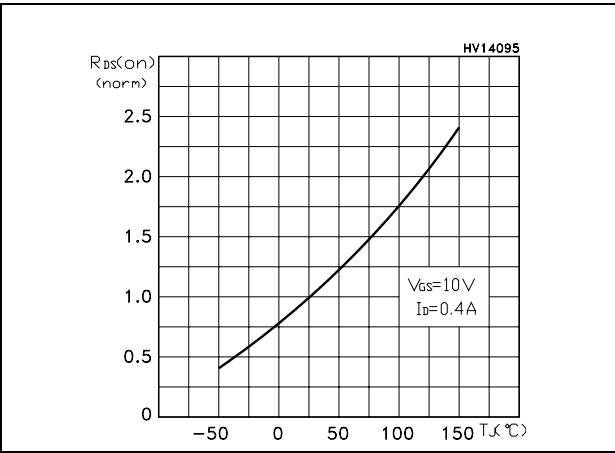


Figure 15. Source-drain diode forward characteristics

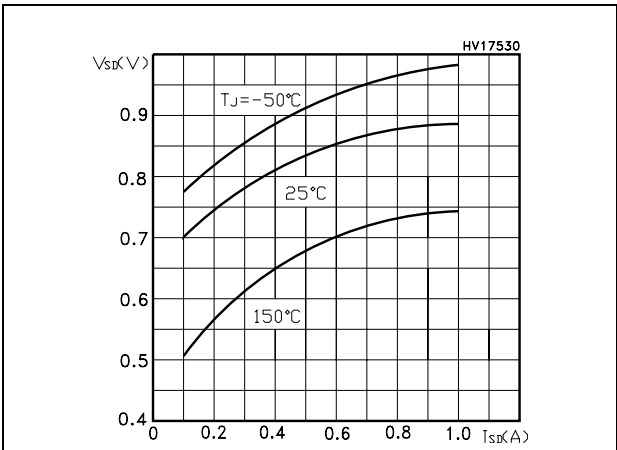


Figure 16. Normalized $B_{V_{DSS}}$ vs temperature

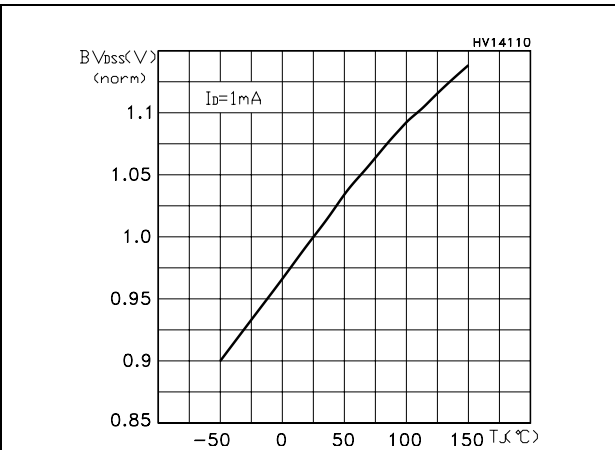


Figure 17. Maximum avalanche energy vs temperature

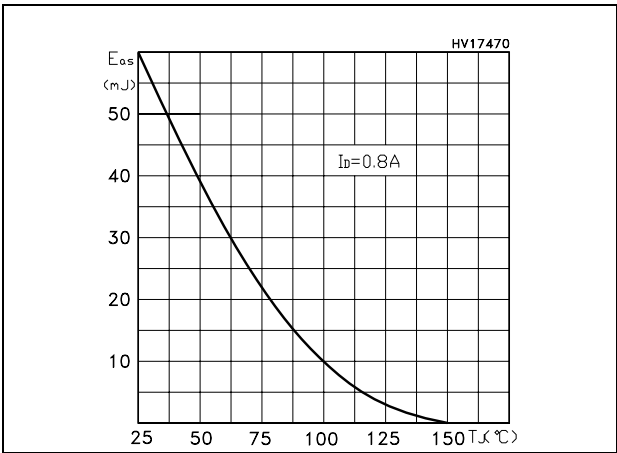
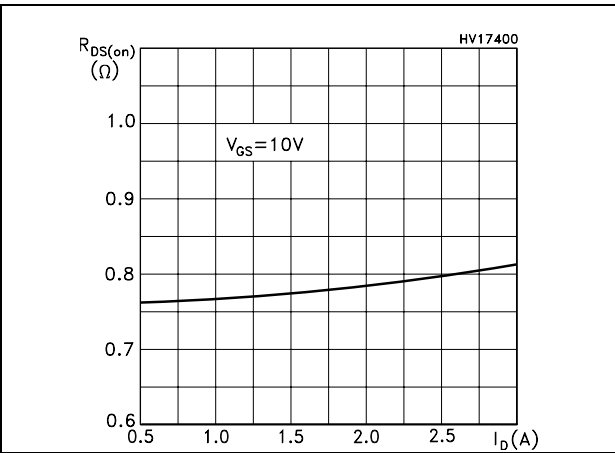


Figure 18. Max Id Current vs T_c



3 Test circuit

Figure 19. Switching times test circuit for resistive load

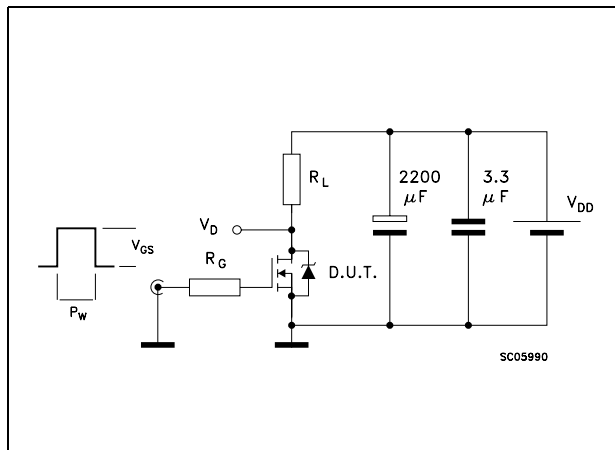


Figure 20. Gate charge test circuit

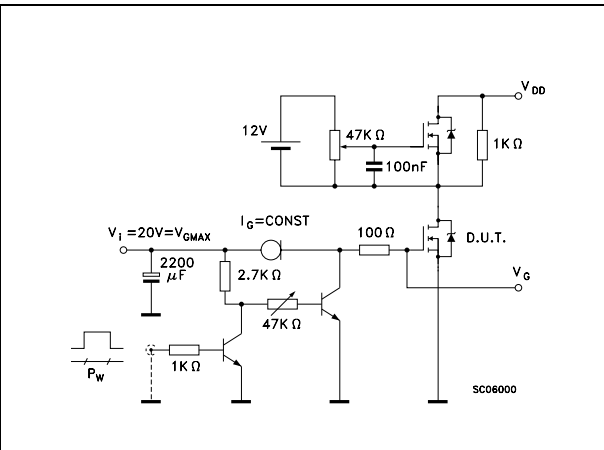


Figure 21. Test circuit for inductive load switching and diode recovery times

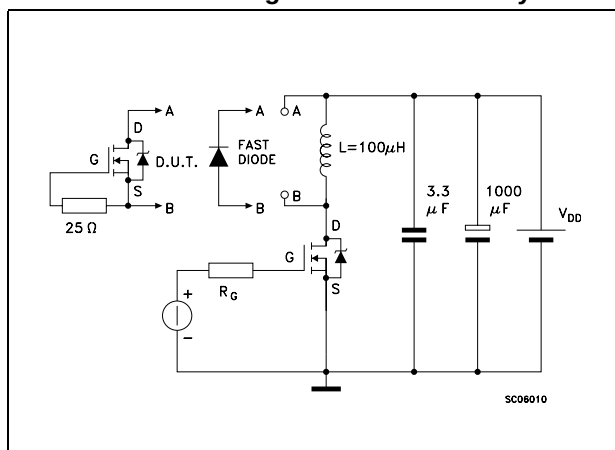


Figure 22. Unclamped Inductive load test circuit

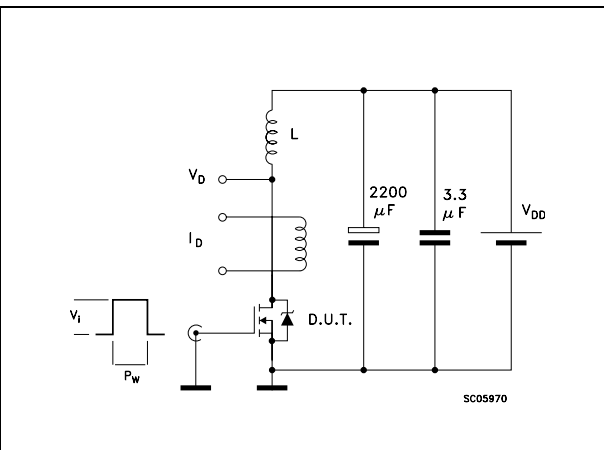


Figure 23. Unclamped inductive waveform

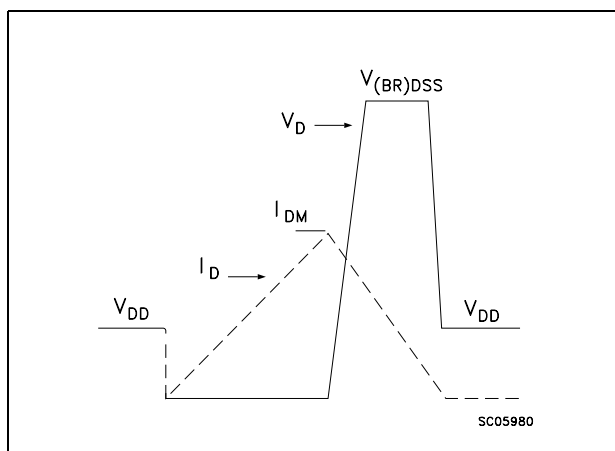
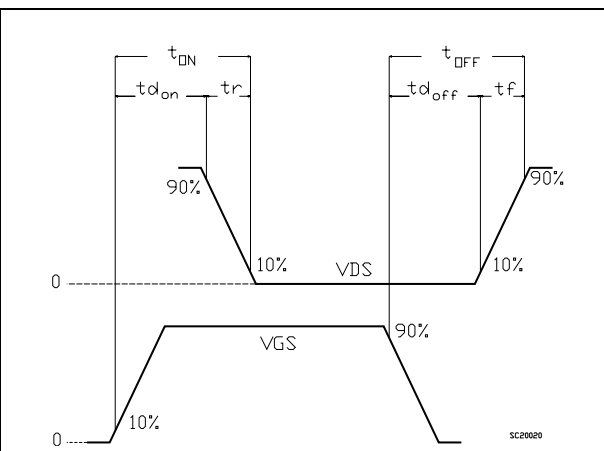


Figure 24. Switching time waveform

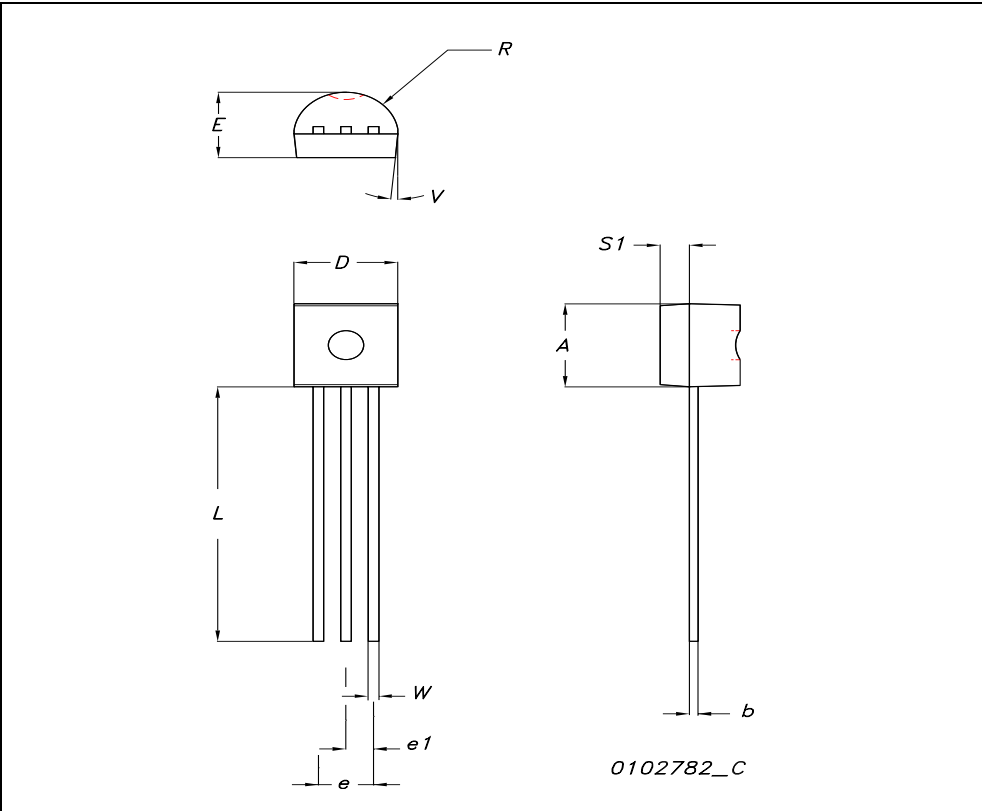


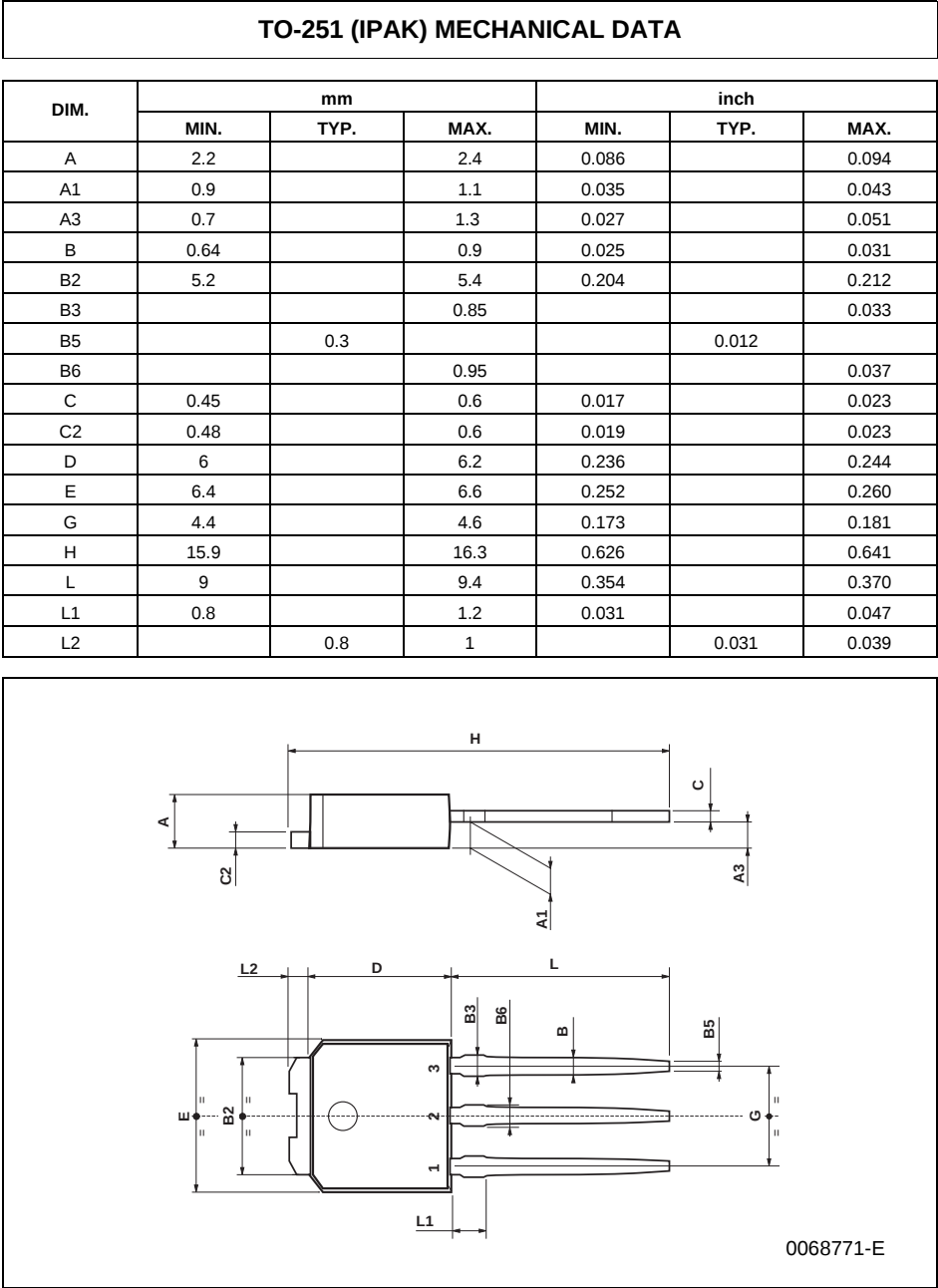
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	





SOT-223 MECHANICAL DATA						
DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a	2.27	2.3	2.33	89.4	90.6	91.7
b	4.57	4.6	4.63	179.9	181.1	182.3
c	0.2	0.4	0.6	7.9	15.7	23.6
d	0.63	0.65	0.67	24.8	25.6	26.4
e1	1.5	1.6	1.7	59.1	63	66.9
e4			0.32			12.6
f	2.9	3	3.1	114.2	118.1	122.1
g	0.67	0.7	0.73	26.4	27.6	28.7
l1	6.7	7	7.3	263.8	275.6	287.4
l2	3.5	3.5	3.7	137.8	137.8	145.7
L	6.3	6.5	6.7	248	255.9	263.8

The diagram illustrates the mechanical specifications of the SOT-223 package through three views: top, side, and bottom. The top view shows the overall length L and the distance from the lead edge to the center of the leads, labeled as a and b. The side view shows the package height e1, the lead thickness d, the lead width c, and the lead separation e4. The bottom view shows the lead spacing g, the lead length f, and the overall length l1. The package body is labeled with B, C, and E.

P008B

5 Revision history

Table 9. Revision history

Date	Revision	Changes
19-Mar-2003	1	First Release
15-May-2003	2	Removed DPAK
09-Jun-2003	3	Final datasheet
17-Nov-2004	4	Inserted SOT-223
15-Feb-2005	5	Modified Figure 3.
07-Sep-2005	6	Inserted ecopak indication
22-Feb-2006	7	New template

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