



IS61NW6432

64K x 32 SYNCHRONOUS STATIC RAM WITH NO-WAIT STATE BUS FEATURE

FEATURES

- Fast access time:
 - 5 ns-100 MHz; 6 ns-83 MHz;
 - 7 ns-75 MHz; 8ns-66 MHz;
- No wait cycles between Read and write
- Internal self-timed write cycle
- Individual byte write Control
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-pin LQFP and PQFP package
- Single +3.3V power supply
- Optional data strobe pin (#80) for latching data (See page 12 for detailed timing)

DESCRIPTION

The IS61NW6432 is a high-speed, low-power synchronous static RAM designed to provide a burstable, high-performance, no-wait bus, secondary cache for the Pentium, 680X0, and Power PC microprocessors. It is organized as 65,536 words by 32 bits, fabricated with ICSI's advanced CMOS technology.

Incorporating a no-wait bus, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

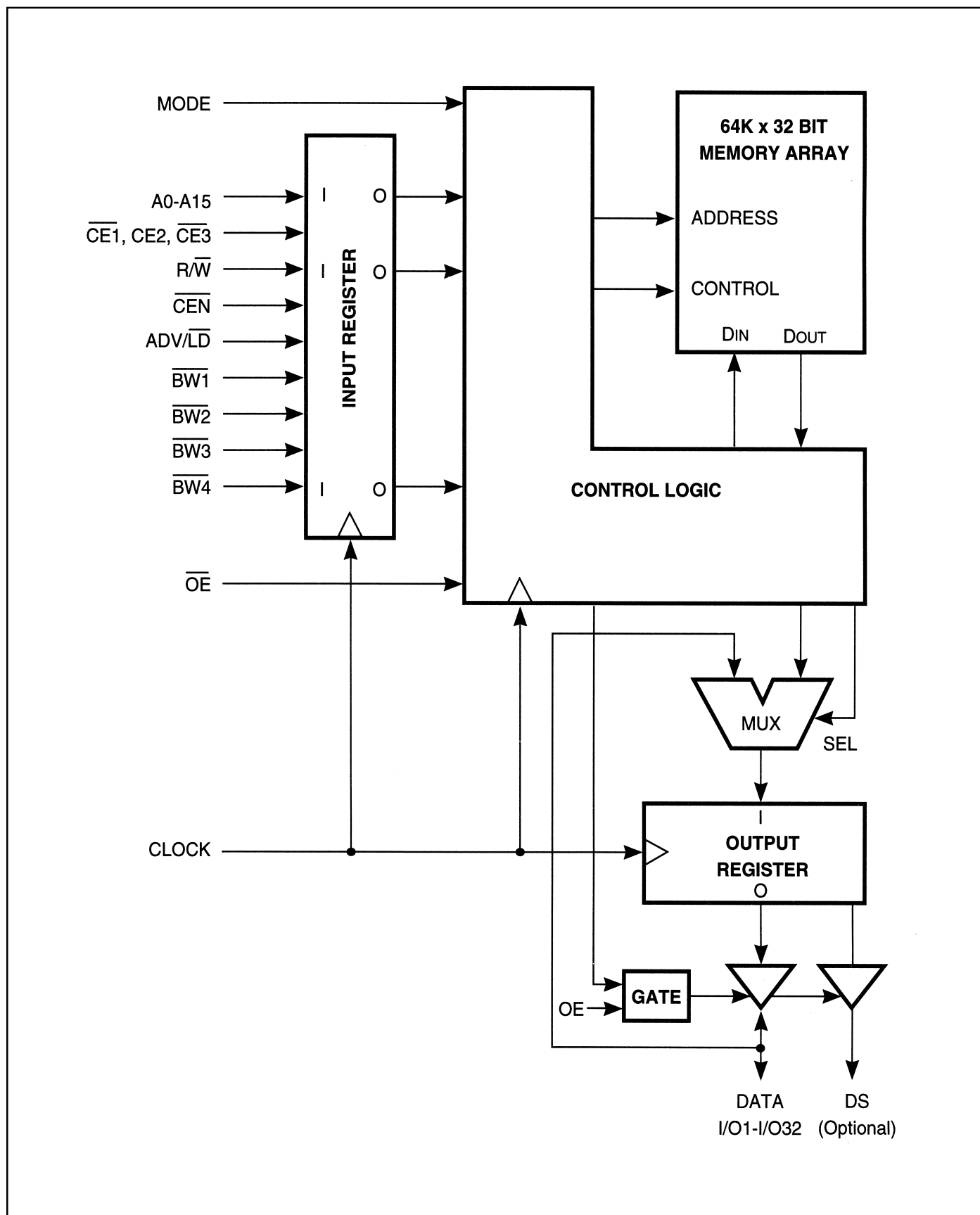
All synchronous inputs pass through registers controlled by a Positive-edge-triggered clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{CEN}$ is HIGH. In this state the internal device will hold their previous values.

When the $ADV/\overline{LD}$ is HIGH the internal burst counter is incremented. New external addresses can be loaded when $ADV/\overline{LD}$ is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $RD/\overline{WE}$ is LOW. Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls I/O1-I/P8; $\overline{BW2}$ controls I/O9-I/O16; $\overline{BW3}$ controls I/O17-I/O24; $\overline{BW4}$ controls I/O25-I/O32. All Bytes are written when $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, and $\overline{BW4}$ are LOW.

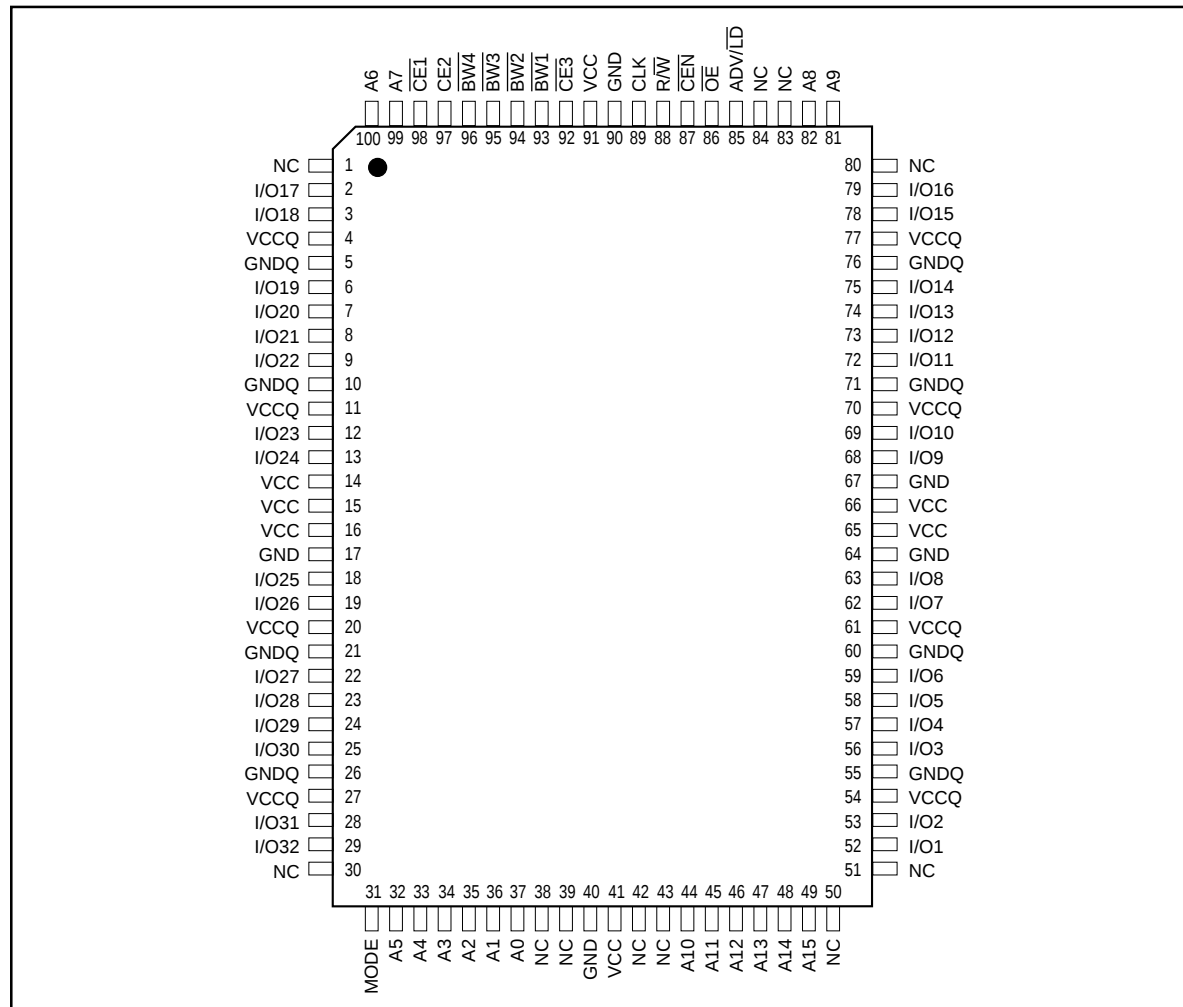
MODE pin upon power up is in interleave burst mode. It can be connected to GND or Vccq to alter power up state.

BLOCK DIAGRAM



PIN CONFIGURATION

100-Pin LQFP and PQFP (Top View)



PIN DESCRIPTIONS

A0-A15	Address Inputs
CLK	Clock
$\overline{\text{CEN}}$	Clock Enale
ADV/ $\overline{\text{CD}}$	Advance Load
$\overline{\text{BW1}}\text{-}\overline{\text{BW4}}$	Synchronous Byte Write Enable
R / $\overline{\text{W}}$	Read / Write
$\overline{\text{CE1}}$, $\overline{\text{CE2}}$, $\overline{\text{CE3}}$	Synchronous Chip Enable
$\overline{\text{OE}}$	Output Enable
DS ⁽¹⁾	Data Strobe

I/O-I/O32	Data Input/Output
MODE	Burst Sequence Mode
V _{CC}	+3.3V Power Supply
GND	Ground
V _{CCQ}	Isolated Output Buffer Supply: +3.3V
GND _Q	Isolated Output Buffer Ground
NC	No Connect

Notes:

1. Optional, NC or DS.

TRUTH TABLE⁽¹⁾

Operation	Address Used	R/ $\overline{W}$	$\overline{CE_x}$	ADV/ $\overline{LD}$	$\overline{CEN}$	$\overline{BW_x}$	CLK
Begin New Write Cycle	External	L	L	L	L	Valid	L-H
Begin New Read Cycle	External	H	L	L	L	X	L-H
Advance Burst Counter ⁽²⁾ (Burst Write)	Internal	X	X	H	L	Valid	L-H
Advance Burst Counter (BurstRead)	Internal	X	X	H	L	X	L-H
Deselect (2 Cycle)	X	X	H	L	L	X	L-H
Hold/NOOP ⁽⁴⁾	X	X	X	X	H	X	L-H

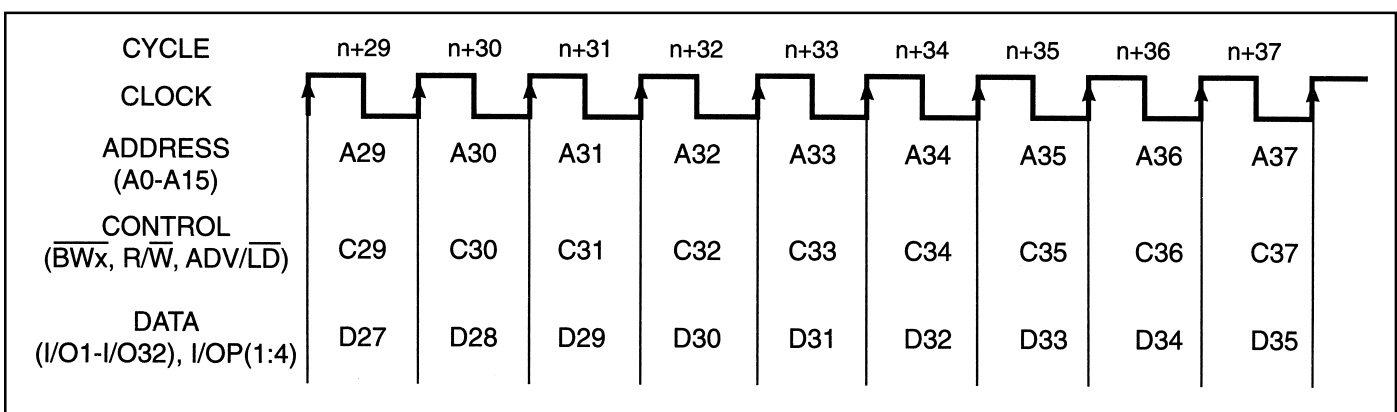
Notes:

1. "X" Means don't care.
2. When ADV/ $\overline{LD}$ signal is sampled HIGH, the internal burst counter is incremented. The R/ $\overline{W}$ signal is ignored when the counter is advanced, Therefore, the nature of the burst cycle (Read or Write) is determined by the status of the R/ $\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when $\overline{CE_x}$ is sampled HIGH and ADV/ $\overline{LD}$ sampled LOW at rising edge of clock. The data bus will tristate two cycles after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers remains unchanged.

PARTIAL TRUTH TABLE(Non-burst)

Function	$\overline{GW}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$	$\overline{CE_x}$	ADV/ $\overline{LD}$
READ	H	X	X	X	X	L	L
WRITE Byte 1	L	L	H	H	H	L	L
WRITE Byte 2	L	H	L	H	H	L	L
WRITE Byte 3	L	H	H	L	H	L	L
WRITE Byte 4	L	H	H	H	L	L	L
WRITE All Bytes	L	L	L	L	L	X	L

FUNCTIONAL TIMING DIAGRAM



TYPICAL OPERATION

CE1, CE3 and CEN are LOW, CE2 is HIGH, Non-Burst Operation

Cycle	Address	R/W	ADV/LD	CEX	CEN	BWX	OE	I/O	Comments
n	A0	H	L	L	L	X	?	D-2	?
n+1	A1	L	L	L	L	L	?	D-1	?
n+2	A2	H	L	L	L	X	L	D0	Data Out
n+3	A3	L	L	L	L	L	X	D1	Data In
n+4	A4	H	L	L	L	X	L	D2	Data Out
n+5	A5	L	L	L	L	L	X	D3	Data In
n+6	A6	H	L	L	L	X	L	D4	Data Out
n+7	A7	L	L	L	L	L	X	D5	Data In
n+8	A8	H	L	L	L	X	L	D6	Data Out
n+9	A9	L	L	L	L	L	X	D7	Data In
n+10	A10	H	L	L	L	X	L	D8	Data Out
n+11	A11	H	L	L	L	X	X	D9	Data In
n+12	A12	L	L	L	L	L	L	D10	Data Out
n+13	A13	L	L	L	L	L	L	D11	Data Out
n+14	A14	H	L	L	L	X	X	D12	Data In
n+15	A15	H	L	L	L	X	X	D13	Data In
n+16	A16	H	L	L	L	X	L	D14	Data Out
n+17	A17	L	L	L	L	L	L	D15	Data Out
n+18	A18	L	L	L	L	L	L	D16	Data Out
n+19	A19	L	L	L	L	L	x	D17	Data In
n+20	A20	H	L	L	L	X	X	D18	Data In
n+21	A21	H	L	L	L	X	X	D19	Data In

Notes:

1. H=High; L=Low; X=Don't Care;?=Don't Know; Z=High Impedance

READ OPERATION

Cycle	Address	R/W	ADV/LD	CEX	CEN	BWX	OE	I/O	Comments
n	A0	H	L	L	X	X	X	X	Address and Control meet setup
n+1	X	X	X	L	L	X	X	X	Clock Setup valid
n+2	X	X	X	X	X	X	L	D0	Contents of Address A0 Read Out

BURST READ OPERATION

Cycle	Address	R/W	ADV/LD	CEX	CEN	BWX	OE	I/O	Comments
n	A0	H	L	L	X	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup valid, Advance Counter
n+2	X	X	H	X	L	X	L	D0	Address A0 Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	D0+1	Address A0+1 Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	D0+2	Address A0+2 Read Out, Inc. Count
n+5	A1	H	L	L	L	X	L	D0+3	Address A0+3 Read Out, Load A1
n+6	X	X	H	X	L	X	L	D0	Address A0 Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	D1	Address A1 Read Out, Inc. Count
n+8	A2	H	L	L	L	X	L	D0+1	Address A0+1 Read Out, Load A2

WRITE OPERATION

Cycle	Address	R/W	ADV/LD	CEX	CEN	BWX	OE	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	L	L	X	X	X	Clock Setup valid
n+2	X	X	X	X	L	X	X	D0	Write D0 to Address A0

BURST WRITE OPERATION

Cycle	Address	R/W	ADV/LD	CEX	CEN	BWX	OE	I/O	Comments
n	A0	H	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup valid, Inc. Count
n+2	X	X	H	X	L	L	X	D0	Address A0 Write Out, Inc. Count
n+3	X	H	H	L	L	X	L	D0+1	Address A0+1 Write Out, Inc. Count
n+4	X	X	H	X	L	L	X	D0+2	Address A0+2 Write Out, Inc. Count
n+5	A1	L	L	L	L	L	X	D0+3	Address A0+3 Write Out, Load A1
n+6	X	X	H	X	L	L	X	D0	Address A0 Write Out, Inc. Count
n+7	X	X	H	X	L	L	X	D1	Address A1 Write Out, Inc. Count
n+8	A2	L	L	L	L	L	X	D0+1	Address A0+1 Write Out, Load A2

Notes:

1. H=High; L=Low; X=Don't Care;?=Don't Know; Z=High Impedance

READ OPERATION WITH CLOCK ENABLE USED

Cycle	Address	R/W	ADV/LD	CEX	CEN	BWX	OE	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	D0	Clock Ignored, Data D0 is on the bus
n+4	X	X	X	X	H	X	L	D0	Clock Ignored, Data D0 is on the bus
n+5	A2	H	L	L	L	X	L	D0	Address A0 Read Out (bus trans.)
n+6	A3	?	L	L	L	X	L	D1	Address A1 Read Out (bus trans.)
n+7	A4	?	L	L	L	X	L	D2	Address A2 Read Out (bus trans.)

READ OPERATION WITH CLOCK ENABLE USED

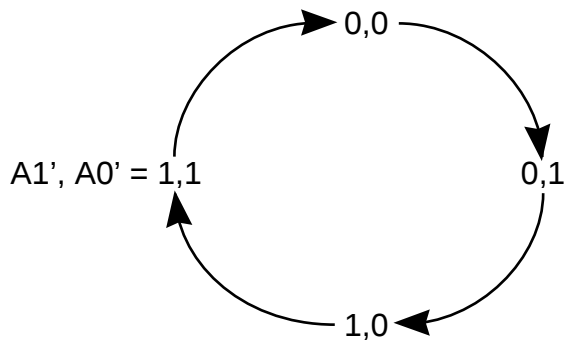
Cycle	Address	R/W	ADV/LD	CEX	CEN	BWX	OE	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A1	L	L	L	L	L	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	di	Clock Ignored.
n+4	X	X	X	X	H	X	L	di	Clock Ignored.
n+5	A2	L	L	L	L	L	L	D0	Write data D0 (bus trans.)
n+6	A3	?	L	L	L	L	L	D1	Write data D1 (bus trans.)
n+7	A4	?	L	L	L	L	L	D2	Write data D2 (bus trans.)

Notes:

1. H=High; L=Low; X=Don't Care;?=Don't Know; Z=High Impedance

INTERLEAVED BURST ADDRESS TABLE (MODE=V_{CCQ} or No connect)

External Address		1st Burst Address		2nd Burst Address		3rd Burst Address	
A1	A0	A1	A0	A1	A0	A1	A0
00		01		10		11	
01		00		11		10	
10		11		00		01	
11		10		01		00	

LINEAR BURST ADDRESS TABLE (MODE=GND_Q)ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
T _{BIAS}	Temperature Under Bias	−10 to +85	°C
T _{STG}	Storage Temperature	−55 to +150	°C
P _D	Power Dissipation	1.8	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for I/O Pins	−0.5 to V _{CCQ} + 0.3	V
V _{IN}	Voltage Relative to GND for for Address and Control Inputs	−0.5 to 5.5	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V +10%, -5%

DC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -5.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 5.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		1.7	V _{CCQ} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CCQ} ⁽²⁾	Com.	-5	5 μA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CCQ} , $\overline{OE} = V_{IH}$	Com.	-5	5 μA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		-5 Min.Typ. Max.	-6 Min.Typ. Max.	-7 Min.Typ. Max.	-8 Min.Typ. Max.	Unit
I _{CC}	AC Operating Supply Current	Device Selected, All Inputs = V _{IL} or V _{IH} $\overline{OE} = V_{IH}$, Cycle Time ≥ t _{CC} min.	Com.	— — 230	— — 220	— — 210	— — 200	mA
I _{SB}	Standby Current	Device Deselected, V _{CC} = Max., All Inputs = V _{IH} or V _{IL} CLK Cycle Time ≥ t _{CC} min. $\overline{CEN} = V_{IH}$	Com.	— — 60	— — 60	— — 60	— — 60	mA

Note:

1. MODE pin has an internal pull up. This pin may be a No Connect, tied to GND, or tied to V_{CCQ}.
2. MODE pin should be tied to V_{CC} or GND. It exhibit ±30 μA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{CC} - 0.2V.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

- 1. Tested initially and after any design or process changes that may affect these parameters.
- 2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1

AC TEST LOADS

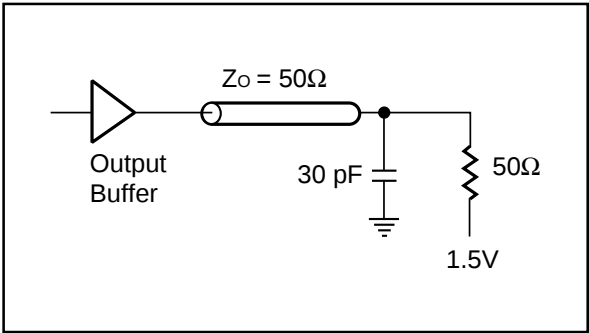


Figure 1

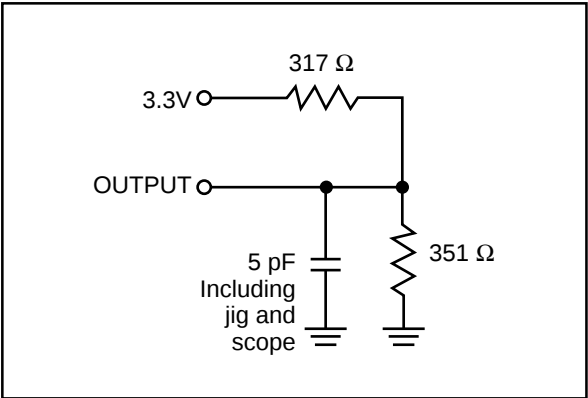


Figure 2

READ /WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-5		-6		-7		-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fmax	Clock Frequency	—	100	—	83	—	75	—	66	MHz
tkc	Cycle Time	10	—	12	—	13	—	15	—	ns
tkH	Clock High Time	4	—	4	—	6	—	6	—	ns
tkL	Clock Low Time	4	—	4	—	6	—	6	—	ns
tkQ	Clock Access Time	—	5	—	6	—	7	—	8	ns
tkQX ⁽²⁾	Clock High to Output Invalid	1.5	—	1.5	—	1.5	—	1.5	—	ns
tkQLZ ⁽²⁾	Clock High to Output Low-Z	2.0	—	2.0	—	2.0	—	2.0	—	ns
tkQHZ ⁽²⁾	Clock High to Output High-Z	1.5	3.5	2	3.5	2	3.5	2	3.5	ns
toEQ	Output Enable to Output Valid	—	5	—	6	—	6	—	6	ns
toEQX ⁽²⁾	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	ns
toELZ ⁽²⁾	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
toEHZ ⁽²⁾	Output Disable to Output High-Z	—	3.5	—	3.5	—	3.5	—	3.5	ns
tas	Address Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
tws	Read/Write Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
tCES	Chip Enable Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
tSE	Clock Enable Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
tAVS	Address Advance Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
tAE	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
tHE	Clock EnableHold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
tWH	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
tCEH	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
tALS	Advance/Load (ADV/ $\overline{LD}$) Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
tALH	Advance/Load (ADV/ $\overline{LD}$) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
tds	Data Setup Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
tdh	Data Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
tzp	I/O From Tri-State to Valid	1.5	—	1.5	2.5	1.5	2.5	1.5	2.5	ns

Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.

The timing diagram illustrates the operation of the 64K16020 across four main phases: Single Read, Single Write, Burst Read, and Unselected. The signals and their timing parameters are as follows:

- CLK**: Clock signal with parameters t_{SE} , t_{HE} , t_{KH} , and t_{KL} .
- CEN**: Chip Enable signal with parameters t_{ALS} and t_{ALH} .
- ADV/LD**: Address/Load signal with parameter t_{AVS} .
- A15-A0**: Address bus showing RD1, RD2, RD3, WR1, RD4, and RD5 operations. Parameters t_{AS} and t_{AH} are indicated.
- R/W**: Read/Write signal with parameters t_{WS} and t_{WH} .
- BW4-BW1**: Bank/Word select signal with parameter t_{WS} and t_{WH} .
- CE1**, **CE2**, **CE3**: Column Enable signals with parameters t_{CES} and t_{CEH} . CE3 is noted as "Unselected with CE3".
- OE**: Output Enable signal with parameters t_{OEQ} and t_{OEZH} .
- DATAOUT**: Data output bus showing data words 1a, 2a, 3a, 4a, 4b, 4c, and 4d. Parameters t_{OELZ} , t_{ZQ} , t_{KQ} , and t_{KQHZ} are indicated.
- DATA STROBE**: Data strobe signal with parameter t_{KQ} .
- DATAIN**: Data input bus showing data word 1a. Parameters t_{DS} and t_{DH} are indicated.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency (MHz)	Order Part Number	Package
5	IS61NW6432-5TQ	14*20*1.4mm LQFP
	IS61NW6432-5PQ	14*20*2.7mm PQFP
6	IS61NW6432-6TQ	14*20*1.4mm LQFP
	IS61NW6432-6PQ	14*20*2.7mm PQFP
7	IS61NW6432-7TQ	14*20*1.4mm LQFP
	IS61NW6432-7PQ	14*20*2.7mm PQFP
8	IS61NW6432-8TQ	14*20*1.4mm LQFP
	IS61NW6432-8PQ	14*20*2.7mm PQFP

*Integrated Circuit Solution Inc.*

HEADQUARTER:

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