

## 100 MHz Differential Buffer for PCI Express and SATA

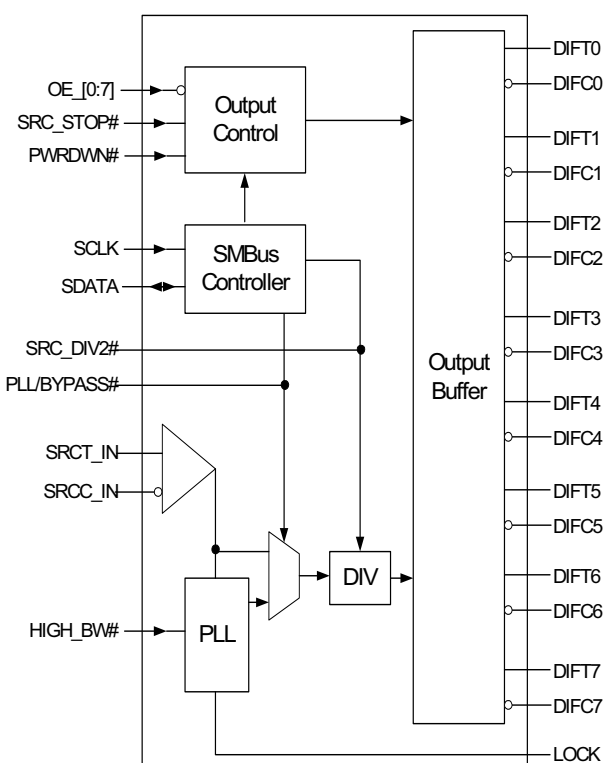
### Features

- CK409 or CK410 companion buffer
- Eight differential 0.7V clock pairs
- Individual OE controls
- Low CTC jitter (< 50 ps)
- Programmable bandwidth
- SRC\_STOP# power management control
- SMBus Block/Byte/Word Read and Write support
- 3.3V operation
- PLL Bypass-configurable
- Divide by 2 programmable
- 48-pin SSOP package

### Functional Description

The CY28401 is a differential buffer and serves as a companion device to the CK409 or CK410 clock generator. The device is capable of distributing the Serial Reference Clock (SRC) in PCI Express and SATA implementations.

### Block Diagram



### Pin Configuration

|             |    |    |           |
|-------------|----|----|-----------|
| SRC_DIV2#   | 1  | 48 | VDD_A     |
| VDD         | 2  | 47 | VSS_A     |
| VSS         | 3  | 46 | IREF      |
| SRCT_IN     | 4  | 45 | LOCK      |
| SRCC_IN     | 5  | 44 | OE_7      |
| OE_0        | 6  | 43 | OE_4      |
| OE_3        | 7  | 42 | DIFT7     |
| DIFT0       | 8  | 41 | DIFC7     |
| DIFC0       | 9  | 40 | VSS       |
| VSS         | 10 | 39 | VDD       |
| VDD         | 11 | 38 | DIFT6     |
| DIFT1       | 12 | 37 | DIFC6     |
| DIFC1       | 13 | 36 | OE_6      |
| OE_1        | 14 | 35 | OE_5      |
| OE_2        | 15 | 34 | DIFT5     |
| DIFT2       | 16 | 33 | DIFC5     |
| DIFC2       | 17 | 32 | VSS       |
| VSS         | 18 | 31 | VDD       |
| VDD         | 19 | 30 | DIFT4     |
| DIFT3       | 20 | 29 | DIFC4     |
| DIFC3       | 21 | 28 | HIGH_BW#  |
| PLL/BYPASS# | 22 | 27 | SRC_STOP# |
| SCLK        | 23 | 26 | PWRDWN#   |
| SDATA       | 24 | 25 | VSS       |

48 SSOP

## Pin Description

| Pin                                           | Name             | Type   | Description                                                                                |
|-----------------------------------------------|------------------|--------|--------------------------------------------------------------------------------------------|
| 4,5                                           | SRCT_IN, SRCC_IN | I,DIF  | <b>0.7V Differential SRC inputs from the clock synthesizer</b>                             |
| 8,9,12,13,16,17,20,21,29,30,33,34,37,38,41,42 | DIFT/C(7:0)      | O,DIF  | <b>0.7V Differential Clock Outputs</b>                                                     |
| 6,7,14,15,35,36,43,44                         | OE_(7:0)         | I,SE   | <b>3.3V LVTTTL active LOW input for three-stating differential outputs</b>                 |
| 28                                            | HIGH_BW#         | I,SE   | <b>3.3V LVTTTL input for selecting PLL bandwidth</b>                                       |
| 45                                            | LOCK             | O,SE   | <b>3.3V LVTTTL output, transitions high when PL lock is achieved (latched output)</b>      |
| 26                                            | PWRDWN#          | I,SE   | <b>3.3V LVTTTL input for Power-down, active LOW</b>                                        |
| 1                                             | SRC_DIV/2#       | I,SE   | <b>3.3V LVTTTL input for selecting input frequency divided by two, active LOW</b>          |
| 27                                            | SRC_STOP#        | I,SE   | <b>3.3V LVTTTL input for SRC_Stop#, active LOW</b>                                         |
| 23                                            | SCLK             | I,SE   | <b>SMBus Slave Clock Input</b>                                                             |
| 24                                            | SDATA            | I/O,OC | <b>Open collector SMBus data</b>                                                           |
| 46                                            | IREF             | I      | <b>A precision resistor is attached to this pin to set the differential output current</b> |
| 22                                            | PLL/BYPASS#      | I      | <b>3.3V LVTTTL input for selecting fan-out or PLL operation</b>                            |
| 48                                            | VDD_A            | 3.3V   | <b>3.3V Power Supply for PLL</b>                                                           |
| 47                                            | VSS_A            | GND    | <b>Ground for PLL</b>                                                                      |
| 3,10,18,25,32,40                              | VSS              | I      | <b>Ground for outputs</b>                                                                  |
| 2,11,19,31,39                                 | VDD              | I      | <b>3.3V power supply for outputs</b>                                                       |

## Serial Data Interface

To enhance the flexibility and function of the clock buffer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11011100 (DCh).

**Table 1. Command Code Definition**

| Bit   | Description                                                                                                                 |
|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 7     | 0 = Block read or block write operation<br>1 = Byte read or byte write operation                                            |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000' |

**Table 2. Block Read and Block Write Protocol**

| Block Write Protocol |                        | Block Read Protocol |                        |
|----------------------|------------------------|---------------------|------------------------|
| Bit                  | Description            | Bit                 | Description            |
| 1                    | Start                  | 1                   | Start                  |
| 2:8                  | Slave address – 7 bits | 2:8                 | Slave address – 7 bits |
| 9                    | Write = 0              | 9                   | Write = 0              |

**Table 2. Block Read and Block Write Protocol (continued)**

| Block Write Protocol |                                                                | Block Read Protocol |                                                                |
|----------------------|----------------------------------------------------------------|---------------------|----------------------------------------------------------------|
| Bit                  | Description                                                    | Bit                 | Description                                                    |
| 10                   | Acknowledge from slave                                         | 10                  | Acknowledge from slave                                         |
| 11:18                | Command Code – 8 bits<br>'00000000' stands for block operation | 11:18               | Command Code – 8 bits<br>'00000000' stands for block operation |
| 19                   | Acknowledge from slave                                         | 19                  | Acknowledge from slave                                         |
| 20:27                | Byte Count from master – 8 bits                                | 20                  | Repeat start                                                   |
| 28                   | Acknowledge from slave                                         | 21:27               | Slave address – 7 bits                                         |
| 29:36                | Data byte 0 from master – 8 bits                               | 28                  | Read = 1                                                       |
| 37                   | Acknowledge from slave                                         | 29                  | Acknowledge from slave                                         |
| 38:45                | Data byte 1 from master – 8 bits                               | 30:37               | Byte count from slave – 8 bits                                 |
| 46                   | Acknowledge from slave                                         | 38                  | Acknowledge from host                                          |
| ....                 | Data bytes from master/Acknowledge                             | 39:46               | Data byte 0 from slave – 8 bits                                |
| ....                 | Data Byte N – 8 bits                                           | 47                  | Acknowledge from host                                          |
| ....                 | Acknowledge from slave                                         | 48:55               | Data byte 1 from slave – 8 bits                                |
| ....                 | Stop                                                           | 56                  | Acknowledge from host                                          |
|                      |                                                                | ....                | Data bytes from slave/Acknowledge                              |
|                      |                                                                | ....                | Data byte N from slave – 8 bits                                |
|                      |                                                                | ....                | Acknowledge from host                                          |
|                      |                                                                | ....                | Stop                                                           |

**Table 3. Byte Read and Byte Write Protocol**

| Byte Write Protocol |                                                                                                                                               | Byte Read Protocol |                                                                                                                                               |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                 | Description                                                                                                                                   | Bit                | Description                                                                                                                                   |
| 1                   | Start                                                                                                                                         | 1                  | Start                                                                                                                                         |
| 2:8                 | Slave address – 7 bits                                                                                                                        | 2:8                | Slave address – 7 bits                                                                                                                        |
| 9                   | Write = 0                                                                                                                                     | 9                  | Write = 0                                                                                                                                     |
| 10                  | Acknowledge from slave                                                                                                                        | 10                 | Acknowledge from slave                                                                                                                        |
| 11:18               | Command Code – 8 bits<br>'100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed | 11:18              | Command Code – 8 bits<br>'100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed |
| 19                  | Acknowledge from slave                                                                                                                        | 19                 | Acknowledge from slave                                                                                                                        |
| 20:27               | Data byte from master – 8 bits                                                                                                                | 20                 | Repeat start                                                                                                                                  |
| 28                  | Acknowledge from slave                                                                                                                        | 21:27              | Slave address – 7 bits                                                                                                                        |
| 29                  | Stop                                                                                                                                          | 28                 | Read = 1                                                                                                                                      |
|                     |                                                                                                                                               | 29                 | Acknowledge from slave                                                                                                                        |
|                     |                                                                                                                                               | 30:37              | Data byte from slave – 8 bits                                                                                                                 |
|                     |                                                                                                                                               | 38                 | Acknowledge from master                                                                                                                       |
|                     |                                                                                                                                               | 39                 | Stop                                                                                                                                          |

**Byte 0: Control Register 0**

| Bit | @pup | Name | Description                                                      |
|-----|------|------|------------------------------------------------------------------|
| 7   | 0    |      | PWRDWN# drive mode<br>0 = Driven when stopped, 1 = Three-state   |
| 6   | 0    |      | SRC_STOP# drive mode<br>0 = Driven when stopped, 1 = Three-state |

**Byte 0: Control Register 0** (continued)

| Bit | @pup | Name | Description                                                     |
|-----|------|------|-----------------------------------------------------------------|
| 5   | 0    |      | Reserved                                                        |
| 4   | 0    |      | Reserved                                                        |
| 3   | 0    |      | Reserved                                                        |
| 2   | 1    |      | HIGH_BW#<br>0 = High Bandwidth, 1 = Low bandwidth               |
| 1   | 1    |      | PLL/Bypass#<br>0 = Fanout buffer, 1 = PLL mode                  |
| 0   | 1    |      | SRC_DIV/2<br>0 = Divided by 2 mode, 1 = Normal (output = input) |

**Byte 1: Control Register 1**

| Bit | @pup | Name | Description                                                      |
|-----|------|------|------------------------------------------------------------------|
| 7   | 1    |      | DIF_7 Output Enable<br>0 = Disabled (three-state)<br>1 = Enabled |
| 6   | 1    |      | DIF_6 Output Enable<br>0 = Disabled (three-state)<br>1 = Enabled |
| 5   | 1    |      | DIF_5 Output Enable<br>0 = Disabled (three-state)<br>1 = Enabled |
| 4   | 1    |      | DIF_4 Output Enable<br>0 = Disabled (three-state)<br>1 = Enabled |
| 3   | 1    |      | DIF_3 Output Enable<br>0 = Disabled (three-state)<br>1 = Enabled |
| 2   | 1    |      | DIF_2 Output Enable<br>0 = Disabled (three-state)<br>1 = Enabled |
| 1   | 1    |      | DIF_1 Output Enable<br>0 = Disabled (three-state)<br>1 = Enabled |
| 0   | 1    |      | DIF_0 Output Enable<br>0 = Disabled (three-state)<br>1 = Enabled |

**Byte 2: Control Register 2**

| Bit | @pup | Name | Description                                                                                       |
|-----|------|------|---------------------------------------------------------------------------------------------------|
| 7   | 0    |      | Allow Control DIF_7 with assertion of SRC_STOP#<br>0 = Free-running<br>1 = Stopped with SRC_STOP# |
| 6   | 0    |      | Allow Control DIF_6 with assertion of SRC_STOP#<br>0 = Free-running<br>1 = Stopped with SRC_STOP# |
| 5   | 0    |      | Allow Control DIF_5 with assertion of SRC_STOP#<br>0 = Free-running<br>1 = Stopped with SRC_STOP# |
| 4   | 0    |      | Allow Control DIF_4 with assertion of SRC_STOP#<br>0 = Free-running<br>1 = Stopped with SRC_STOP# |

**Byte 2: Control Register 2 (continued)**

| Bit | @pup | Name | Description                                                                                       |
|-----|------|------|---------------------------------------------------------------------------------------------------|
| 3   | 0    |      | Allow Control DIF_3 with assertion of SRC_STOP#<br>0 = Free-running<br>1 = Stopped with SRC_STOP# |
| 2   | 0    |      | Allow Control DIF_2 with assertion of SRC_STOP#<br>0 = Free-running<br>1 = Stopped with SRC_STOP# |
| 1   | 0    |      | Allow Control DIF_1 with assertion of SRC_STOP#<br>0 = Free-running<br>1 = Stopped with SRC_STOP# |
| 0   | 0    |      | Allow Control DIF_0 with assertion of SRC_STOP#<br>0 = Free-running<br>1 = Stopped with SRC_STOP# |

**Byte 3: Control Register 3**

| Bit | @pup | Name | Description |
|-----|------|------|-------------|
| 7   | 0    |      | Reserved    |
| 6   | 0    |      | Reserved    |
| 5   | 0    |      | Reserved    |
| 4   | 0    |      | Reserved    |
| 3   | 0    |      | Reserved    |
| 2   | 0    |      | Reserved    |
| 1   | 0    |      | Reserved    |
| 0   | 0    |      | Reserved    |

**Byte 4: Vendor ID Register**

| Bit | @Pup | Name | Description         |
|-----|------|------|---------------------|
| 7   | 0    |      | Revision Code Bit 3 |
| 6   | 0    |      | Revision Code Bit 2 |
| 5   | 0    |      | Revision Code Bit 1 |
| 4   | 0    |      | Revision Code Bit 0 |
| 3   | 1    |      | Vendor ID Bit 3     |
| 2   | 0    |      | Vendor ID Bit 2     |
| 1   | 0    |      | Vendor ID Bit 1     |
| 0   | 0    |      | Vendor ID Bit 0     |

**Byte 5: Control Register 5**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7   | 0    |      | Reserved    |
| 6   | 0    |      | Reserved    |
| 5   | 0    |      | Reserved    |
| 4   | 0    |      | Reserved    |
| 3   | 0    |      | Reserved    |
| 2   | 0    |      | Reserved    |
| 1   | 0    |      | Reserved    |
| 0   | 0    |      | Reserved    |

## PWRDWN# Clarification<sup>[1]</sup>

The PWRDWN# pin is used to shut off all clocks cleanly and instruct the device to evoke power savings mode. Additionally, PWRDWN# should be asserted prior to shutting off the input clock or power to ensure all clocks shut down in a glitch-free manner. PWRDWN# is an asynchronous active LOW input. This signal is synchronized internal to the device prior to powering down the clock buffer. PWRDWN# is an asynchronous input for powering up the system. When PWRDWN# is asserted LOW, all clocks will be held HIGH or three-stated (depending on the state of the control register drive mode and OE bits) prior to turning off the VCO. All clocks will start and stop without any abnormal behavior and must meet all AC and DC parameters. This means no glitches, frequency shifting or amplitude abnormalities among others.

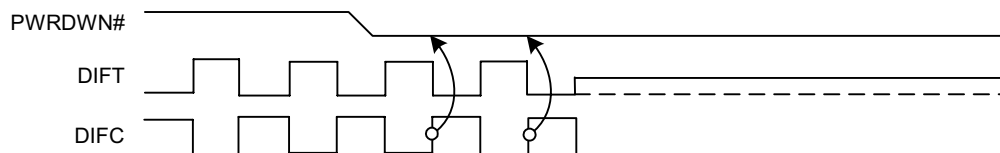
## PWRDWN# Assertion

When PWRDWN# is sampled LOW by two consecutive rising edges of DIFC, all DIFT outputs will be held HIGH or

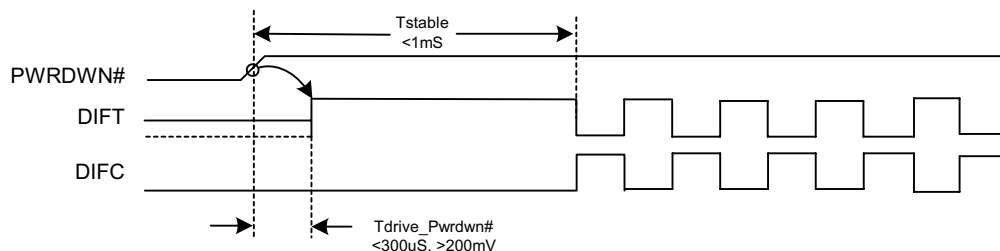
three-stated (depending on the state of the control register drive mode and OE bits) on the next DIFC HIGH-to-LOW transition. When the SMBus power-down drive mode bit is programmed to '0', all clock outputs will be held with the DIFT pin driven high at  $2 \times I_{ref}$  and DIFC three-state. However, if the control register PWRDWN# drive mode bit is programmed to '1', then both DIFT and the DIFC are three-stated.

## PWRDWN# Deassertion

The power-up latency is less than 1 ms. This is the time from the deassertion of the PWRDWN# pin or the ramping of the power supply or the time from valid SRC\_IN input clocks until the time that stable clocks are output from the buffer chip (PLL locked). If the control register PWRDWN# three-state bit is programmed to '1', all differential outputs must be driven high in less than 300  $\mu$ s of PWRDWN# deassertion to a voltage greater than 200 mV.



**Figure 1. PWRDWN# Assertion Diagram**



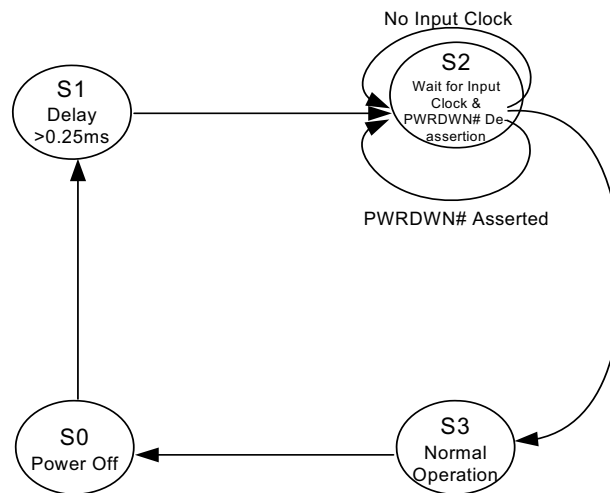
**Figure 2. PWRDWN# Deassertion Diagram**

**Table 4. Buffer Power-up State Machine**

| State                | Description                                                                                                            |
|----------------------|------------------------------------------------------------------------------------------------------------------------|
| 0                    | 3.3V Buffer power off                                                                                                  |
| 1                    | After 3.3V supply is detected to rise above 1.8V - 2.0V, the buffer enters state 1 and initiates a 0.2-ms–0.3-ms delay |
| 2 <sup>[5]</sup>     | Buffer <b>waits for a valid clock on the SRC_IN input</b> and PWRDWN# deassertion                                      |
| 3 <sup>[2,3,4]</sup> | Once the PLL is locked to the SRC_IN input clock, the buffer enters state 3 and enables outputs for normal operation   |

### Notes:

- Disabling of the SRCT\_IN input clock prior to assertion of PWRDWN# is an undefined mode and not recommended. Operation in this mode may result in glitches excessive frequency shifting.
- The total power-up latency from power on to all outputs active is less than 1 ms (assuming a valid clock is present on SRC\_IN input).
- Lock output is a latched signal that is reset with the assertion of PWRDWN# or when VDD < 1.8V.
- Special care must be taken to ensure that no abnormal clock behavior occurs after the assertion PLL LOCK (i.e., overshoot undershoot is allowed).
- If power is valid and PWRDWN# is deasserted but no input clocks are present on the SRC\_IN input, DIF clocks will remain disabled. Only after valid input clocks are detected, valid power, PWRDWN# deasserted with the PLL locked and stable are the DIF outputs enabled.



**Figure 3. Buffer Power-up State Diagram**

### SRC\_STOP# Clarification

The SRC\_STOP# signal is an active LOW input used for clean stopping and starting the DIFT/C outputs (valid clock must be present on SRCT/C\_IN). The SRC\_STOP# signal is a debounced signal in that its state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

**Table 5. SRC\_STOP# Functionality<sup>[6]</sup>**

| SRC_STOP# | DIFT              | DIFC   |
|-----------|-------------------|--------|
| 1         | Normal            | Normal |
| 0         | Iref * 6 or Float | Low    |

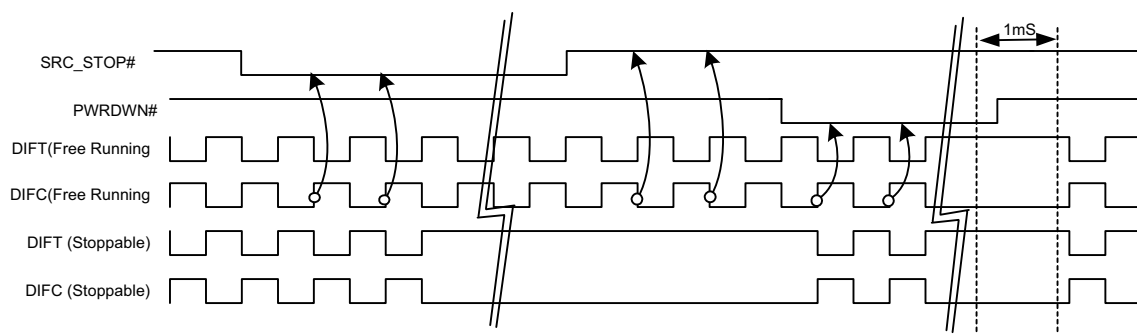
### SRC\_STOP# Assertion

The impact of asserting the SRC\_STOP# pin is that all DIF outputs that are set in the control registers to stoppable via assertion of SRC\_STOP# are stopped after their next

transition. When the control register SRC\_STOP# three-state bit is programmed to '0', the final state of all stopped DIFT/C signals is DIFT clock = HIGH and DIFC = LOW. There will be no change to the output drive current values, DIFT will be driven HIGH with a current value equal  $6 \times I_{ref}$ , and DIFC will not be driven. When the control register SRC\_STOP# three-state bit is programmed to '1', the final state of all stopped DIF signals is LOW, both DIFT clock and DIFC clock outputs will not be driven.

### SRC\_STOP# Deassertion

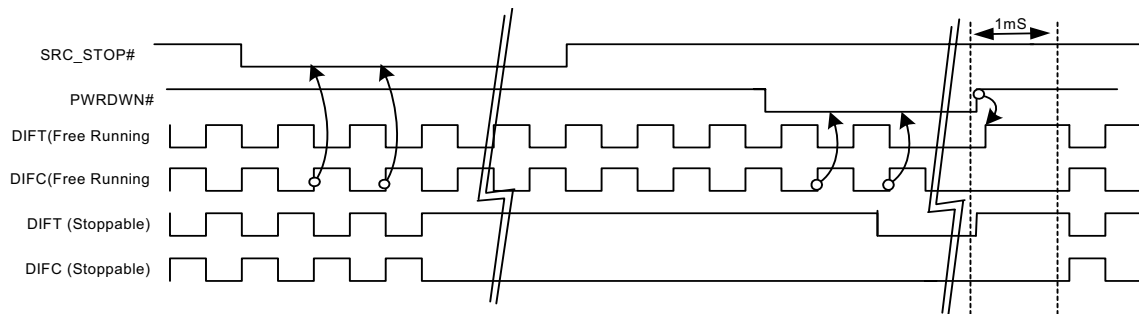
All differential outputs that were stopped will resume normal operation in a glitch-free manner. The maximum latency from the deassertion to active outputs is between 2-6 DIFT/C clock periods (2 clocks are shown) with all DIFT/C outputs resuming simultaneously. If the control register three-state bit is programmed to '1' (three-state), then all stopped DIFT outputs will be driven high within 10 ns of SRC\_STOP# deassertion to a voltage greater than 200 mV.



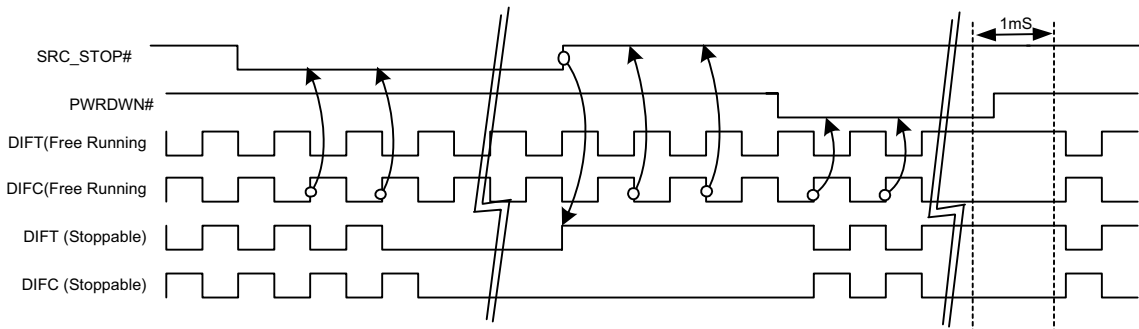
**Figure 4. SRC\_STOP# = Driven, PWRDWN# = Driven**

**Note:**

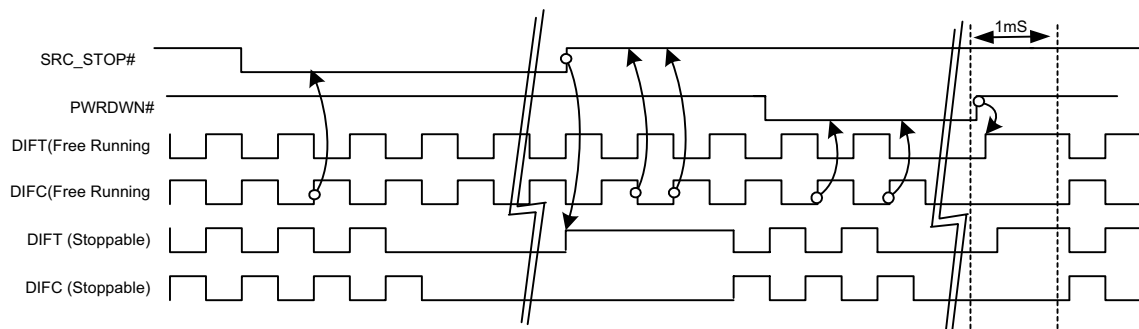
6. In the case where OE is asserted LOW, the output will always be three-stated regardless of SRC\_STOP# drive mode register bit state.



**Figure 5. SRC\_STOP# =Driven, PWRDWN# = Three-state**



**Figure 6. SRC\_STOP# =Three-state, PWRDWN# = Driven**



**Figure 7. SRC\_STOP# =Three-state, PWRDWN# = Three-state**

## Output Enable Clarification

The OE function may be implemented in two ways, via writing a '0' to SMBus register bit corresponding to output of interest or by asserting an OE input pin LOW. In both methods, if SMBus registered bit has been written LOW or the OE pin is LOW or both, the output of interest will be three-stated. (The assertion and deassertion of this signal is absolutely asynchronous.)

**Table 6. OE Functionality**

| OE (Pin)# | OE (SMBus Bit) | DIFT        | DIFC   |
|-----------|----------------|-------------|--------|
| 1         | 1              | Normal      | Normal |
| 1         | 0              | Three-state | Low    |
| 0         | 1              | Three-state | Low    |
| 0         | 0              | Three-state | Low    |

### OE Assertion (Transition from '0' to '1')

All differential outputs that were three-stated will resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2–6 DIF clock periods. In addition, DIFT clocks will be driven HIGH within 10 ns of OE assertion to a voltage greater than 200 mV.

### OE Deassertion (Transition from '1' to '0')

The impact of deasserting OE is each corresponding output will transition from normal operation to three-state in a glitch-free manner. The maximum latency from the deassertion to three-stated outputs is between 2–6 DIF clock periods.

### LOCK Signal Clarification

The LOCK output signal is intended to provide designers a signal indicating that PLL lock has been achieved and valid clock are available. This can be helpful when cascading multiple buffers that each contribute a 1-ms start-up delay in addition to the start-up time of the clock source. Upon receiving a valid clock on the SRC\_IN input (PWRDWN# deasserted), the buffer will begin ramping the internal PLL until lock is achieved and stable, the clock buffer will assert the LOCK pin HIGH and enable DIF output clocks. In other words, if power is valid and PWRDWN# is deasserted but no input clocks are present on the SRC\_IN input, all DIF clocks remain disabled. Only after valid input clocks are detected, valid power, PWRDWN# deasserted with the PLL locked and stable are LOCK to be asserted and the DIF outputs enabled. The maximum start-up latency from valid clocks on SRC\_IN input to the assertion of LOCK (output clocks are valid) is to be less than 1 ms. Once LOCK has been asserted high, it will remain high (regardless of the actual PLL status) until power is removed or the PWRDWN# pin has been asserted.

### SRC\_DIV2# Clarification

The SRC\_DIV2# input is used to configure the DIF output mode to be equal to the SRC\_IN input frequency or half the input frequency in a glitch-free manner. The SRC\_DIV2#

function may be implemented in two ways, via writing a '0' to SMBus register bit or by asserting the SRC\_DIV2# input pin LOW. In both methods, if the SMBus register bit has been written LOW or the SRC\_DIV2# pin is LOW or both, all DIF outputs will configured for divide by 2 operation.

### SRC\_DIV2# Assertion

The impact of asserting the SRC\_DIV2# is that all DIF outputs will transition cleanly in a glitch-free manner from normal operation (output frequency equal to input) to half the input frequency within 2–6 DIF clock periods.

### SRC\_DIV2# Deassertion

The impact of deasserting the SRC\_DIV2# is that all DIF outputs will transition cleanly in a glitch-free manner from divide by 2 mode to normal (output frequency is equal to the input frequency) operation within 2–6 DIF clock periods.

### PLL/BYPASS# Clarification

The PLL/Bypass# input is used to select between bypass mode (no PLL) and PLL mode. In bypass mode, the input clock is passed directly to the output stage resulting in 50-ps additive jitter (50 ps + input jitter) on DIF outputs. In the case of PLL mode, the input clock is pass through a PLL to reduce high-frequency jitter. The BYPASS# mode may be selected in two ways, via writing a '0' to SMBus register bit or by asserting the PLL/BYPASS# pin LOW. In both methods, if the SMBus register bit has been written LOW or PLL/BYPASS# pin is LOW or both, the device will be configured for BYPASS operation.

### HIGH\_BW# Clarification

The HIGH\_BW# input is used to set the PLL bandwidth. This mode is intended to minimize PLL peaking when two or more buffers are cascaded by staggering device bandwidths. The PLL low-bandwidth mode may be selected in two ways, via writing a '0' to SMBus register bit or by asserting the HIGH\_BW# pin is LOW or both; the device will be configured for low-bandwidth operation.

**Absolute Maximum Conditions**

| Parameter          | Description                       | Condition                   | Min. | Max.                  | Unit |
|--------------------|-----------------------------------|-----------------------------|------|-----------------------|------|
| V <sub>DD</sub>    | Core Supply Voltage               |                             | −0.5 | 4.6                   | V    |
| V <sub>DD_A</sub>  | Analog Supply Voltage             |                             | −0.5 | 4.6                   | V    |
| V <sub>IN</sub>    | Input Voltage                     | Relative to V <sub>SS</sub> | −0.5 | V <sub>DD</sub> + 0.5 | VDC  |
| T <sub>S</sub>     | Temperature, Storage              | Non-functional              | −65  | +150                  | °C   |
| T <sub>A</sub>     | Temperature, Operating Ambient    | Functional                  | 0    | 70                    | °C   |
| T <sub>J</sub>     | Temperature, Junction             | Functional                  |      | 150                   | °C   |
| Ø <sub>JC</sub>    | Dissipation, Junction to Case     | Mil-Spec 883E Method 1012.1 |      | TBD                   | °C/W |
| Ø <sub>JA</sub>    | Dissipation, Junction to Ambient  | JEDEC (JESD 51)             |      | TBD                   | °C/W |
| ESD <sub>HBM</sub> | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015    | 2000 |                       | V    |
| UL-94              | Flammability Rating               | At 1/8 in.                  | V-0  |                       |      |
| MSL                | Moisture Sensitivity Level        |                             | 1    |                       |      |

**Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Electrical Specifications**

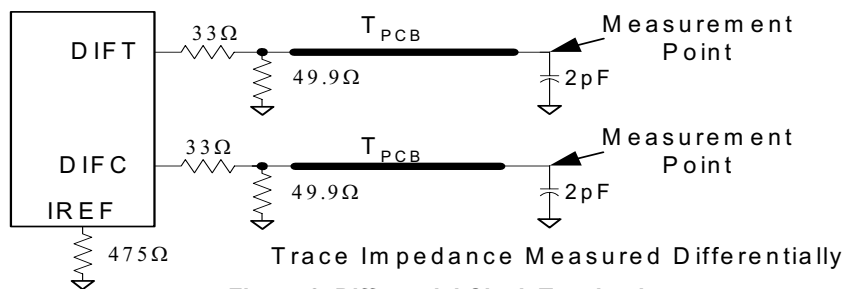
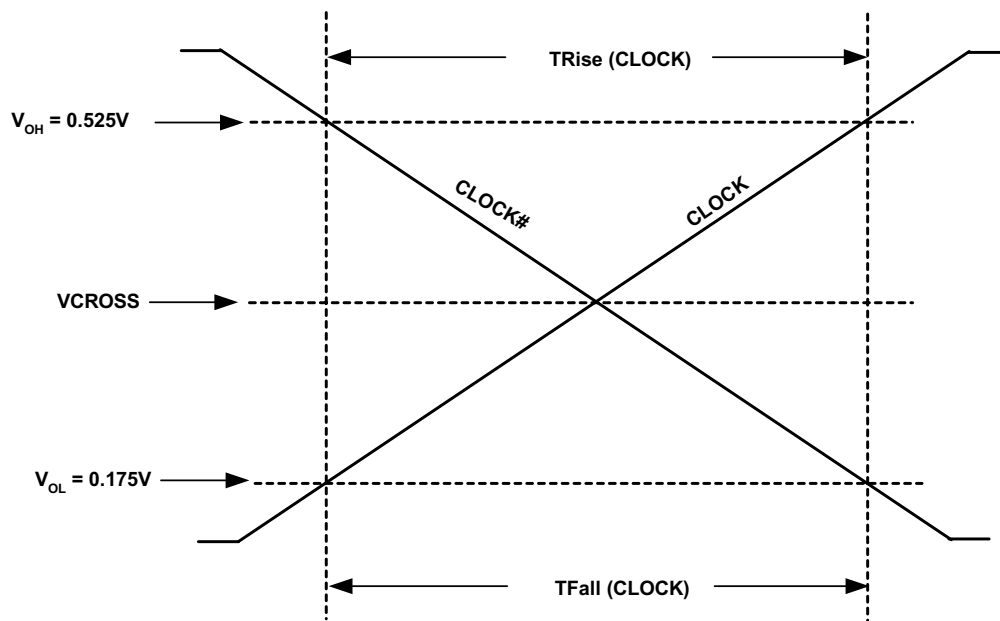
| Parameter                           | Description                   | Condition                                                                  | Min.                  | Max.                  | Unit |
|-------------------------------------|-------------------------------|----------------------------------------------------------------------------|-----------------------|-----------------------|------|
| V <sub>DD_A</sub> , V <sub>DD</sub> | 3.3V Operating Voltage        | 3.3 ± 5%                                                                   | 3.135                 | 3.465                 | V    |
| V <sub>IL12C</sub>                  | Input Low Voltage             | SDATA, SCLK                                                                | –                     | 1.0                   | V    |
| V <sub>IH12C</sub>                  | Input High Voltage            | SDATA, SCLK                                                                | 2.2                   | –                     | V    |
| V <sub>IL</sub>                     | 3.3V Input Low Voltage        |                                                                            | V <sub>SS</sub> – 0.5 | 0.8                   | V    |
| V <sub>IH</sub>                     | 3.3V Input High Voltage       |                                                                            | 2.0                   | V <sub>DD</sub> + 0.5 | V    |
| V <sub>OL</sub>                     | 3.3V Output Low Voltage       | I <sub>OL</sub> = 1 mA                                                     | –                     | 0.4                   | V    |
| V <sub>OH</sub>                     | 3.3V Output High Voltage      | I <sub>OH</sub> = –1 mA                                                    | 2.4                   | –                     | V    |
| I <sub>IL</sub>                     | Input Low Leakage Current     | Except internal pull-up resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>   | –5                    |                       | µA   |
| I <sub>IH</sub>                     | Input High Leakage Current    | Except internal pull-down resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub> |                       | 5                     | µA   |
| I <sub>OZ</sub>                     | High-impedance Output Current |                                                                            | –10                   | 10                    | µA   |
| C <sub>IN</sub>                     | Input Pin Capacitance         |                                                                            | 2                     | 5                     | pF   |
| C <sub>OUT</sub>                    | Output Pin Capacitance        |                                                                            | 3                     | 6                     | pF   |
| L <sub>IN</sub>                     | Pin Inductance                |                                                                            | –                     | 7                     | nH   |
| I <sub>DD3.3V</sub>                 | Dynamic Supply Current        | At max. load and 100 MHz                                                   | –                     | 300                   | mA   |
| I <sub>PD3.3V</sub>                 | Power-down Supply Current     | PD asserted, Outputs driven                                                | –                     | 65                    | mA   |
| I <sub>PD3.3V</sub>                 | Power-down Supply Current     | PD asserted, Outputs Three-stated                                          | –                     | 5                     | mA   |

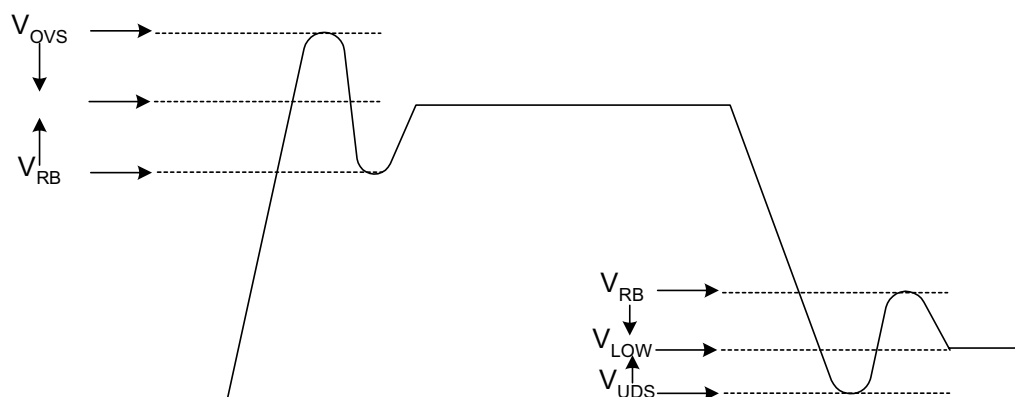
**AC Electrical Specifications**

| Parameter                       | Description                          | Condition                                                                                           | Min.   | Max.    | Unit |
|---------------------------------|--------------------------------------|-----------------------------------------------------------------------------------------------------|--------|---------|------|
| <b>DIF at 0.7V</b>              |                                      |                                                                                                     |        |         |      |
| T <sub>DC</sub>                 | DIFT and DIFC Duty Cycle             | Measured at crossing point V <sub>OX</sub>                                                          | 45     | 55      | %    |
| T <sub>SKEW</sub>               | Any DIFT/C to DIFT/C Clock Skew, SSC | Measured at crossing point V <sub>OX</sub>                                                          | –      | 200     | ps   |
| T <sub>PERIOD</sub>             | Average Period                       | Measured at crossing point V <sub>OX</sub> at 100 MHz                                               | 9.9970 | 10.0533 | ns   |
| T <sub>CCJ</sub>                | DIFT/C Cycle to Cycle Jitter         | Measured at crossing point V <sub>OX</sub>                                                          | –      | 50      | ps   |
| T <sub>R</sub> / T <sub>F</sub> | DIFT and DIFC Rise and Fall Times    | Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V                                   | 175    | 700     | ps   |
| T <sub>RFM</sub>                | Rise/Fall Matching                   | Determined as a fraction of 2*(T <sub>R</sub> – T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> ) | –      | 20      | %    |
| ΔT <sub>R</sub>                 | Rise Time Variation                  |                                                                                                     | –      | 125     | ps   |
| ΔT <sub>F</sub>                 | Fall Time Variation                  |                                                                                                     | –      | 125     | ps   |
| V <sub>HIGH</sub>               | Voltage High                         | Measured SE                                                                                         | 660    | 850     | mv   |

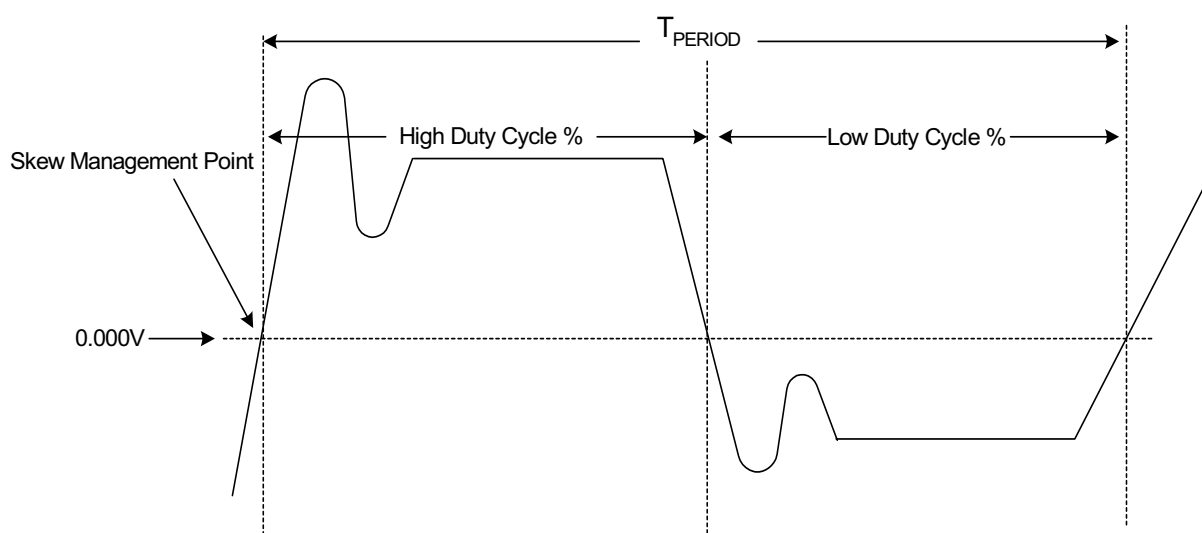
**AC Electrical Specifications** (continued)

| Parameter        | Description                          | Condition                           | Min. | Max.             | Unit |
|------------------|--------------------------------------|-------------------------------------|------|------------------|------|
| $V_{LOW}$        | Voltage Low                          | Measured SE                         | -150 | -                | mv   |
| $V_{OX}$         | Crossing Point Voltage at 0.7V Swing |                                     | 250  | 550              | mv   |
| $\Delta V_{OX}$  | Vcross Variation over all edges      |                                     | -    | 140              | mV   |
| $V_{OVS}$        | Maximum Overshoot Voltage            |                                     | -    | $V_{HIGH} + 0.3$ | V    |
| $V_{UDS}$        | Minimum Undershoot Voltage           |                                     | -    | -0.3             | V    |
| $V_{RB}$         | Ring Back Voltage                    | Measured SE                         | 0.2  | N/A              | V    |
| $t_{PD(PLL)}$    | Input to output skew in PLL mode     | Measured at crossing point $V_{OX}$ | -    | $\pm 250$        | ps   |
| $t_{PD(NONPLL)}$ | Input to output skew in Non-PLL mode | Measured at crossing point $V_{OX}$ | 2.5  | 6.5              | ns   |


**Figure 8. Differential Clock Termination**
**Switching Waveforms**

**Figure 9. Single-Ended Measurement Points for TRise and TFall**



**Figure 10. Single-ended Measurement Points for  $V_{OVS}$ ,  $V_{UDS}$  and  $V_{RB}$**



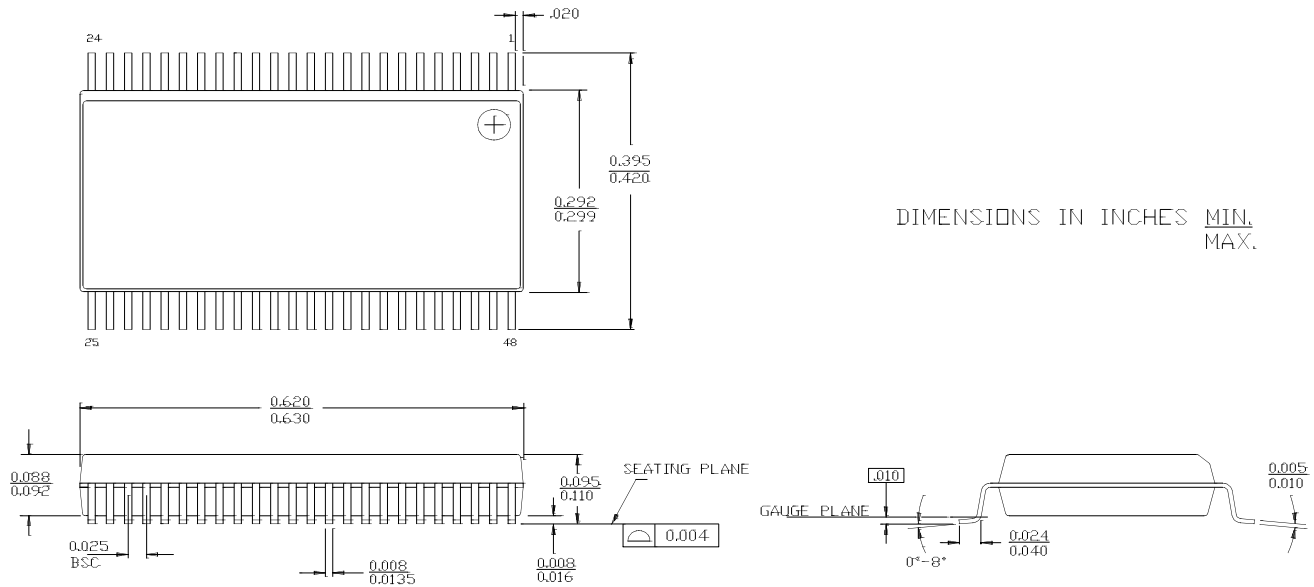
**Figure 11. Differential (Clock-CLock#) Measurement Points (Tperiod, Duty Cycle and Jitter)**

### Ordering Information

| Ordering Code    | Package Type              | Operating Range          |
|------------------|---------------------------|--------------------------|
| CY28401OC        | 48-pin SSOP               | Commercial, 0°C to 70 °C |
| CY28401OCT       | 48-pin SSOP–Tape and Reel | Commercial, 0°C to 70 °C |
| <b>Lead-Free</b> |                           |                          |
| CY28401OXC       | 48-pin SSOP               | Commercial, 0°C to 70 °C |
| CY28401OXCT      | 48-pin SSOP–Tape and Reel | Commercial, 0°C to 70 °C |

## Package Drawing and Dimensions

### 48-Lead Shrunk Small Outline Package O48



51-85061-°C

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