

NTHS4111P

Power MOSFET

–30 V, –6.1 A, Single P–Channel, ChipFET™



ON Semiconductor®

<http://onsemi.com>

Features

- Offers an Ultra Low $R_{DS(on)}$ Solution in the ChipFET Package
- ChipFET Package 40% Smaller Footprint than TSOP–6
- Low Profile (<1.1 mm) for Extremely Thin Environments
- Standard Logic Level Gate Drive
- Pb–Free Package is Available

Applications

- Notebook Computer Load Switch
- Battery and Load Management Applications in Portable Equipment
- Charge Control in Battery Chargers
- Buck and Boost Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating		Symbol	Value	Unit
Drain–to–Source Voltage		V_{DS}	–30	V
Gate–to–Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$ –4.4	A
			$T_A = 85^\circ\text{C}$ –3.2	
	$t \leq 10\text{ s}$		$T_A = 25^\circ\text{C}$ –6.1	
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$ 1.3	W
	$t \leq 10\text{ s}$		2.5	
Continuous Drain Current (Note 2)	Steady State	I_D	$T_A = 25^\circ\text{C}$ –3.3	A
			$T_A = 85^\circ\text{C}$ –2.3	
Power Dissipation (Note 2)		P_D	$T_A = 25^\circ\text{C}$ 0.7	W
Pulsed Drain Current	$tp = 10\text{ }\mu\text{s}$	I_{DM}	–30	A
Operating Junction and Storage Temperature		T_J, T_{STG}	–55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	–2.1	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

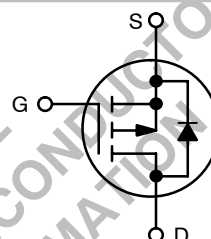
THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	95	$^\circ\text{C/W}$
Junction–to–Ambient – $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	50	
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	175	

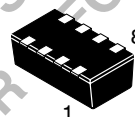
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface–mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface–mounted on FR4 board using the minimum recommended pad size (Cu area = 0.045 in sq).

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
–30 V	33 m Ω @ –10 V	–6.1 A
	52 m Ω @ –4.5 V	

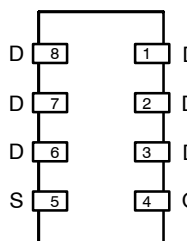


P–Channel MOSFET

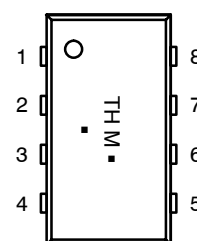


ChipFET
CASE 1206A
STYLE 1

PIN CONNECTIONS



MARKING DIAGRAM



TH = Specific Device Code
M = Date Code
▪ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTHS4111PT1	ChipFET	3000/Tape & Reel
NTHS4111PT1G	ChipFET (Pb–free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			-19		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -24\text{ V}$			-1.0	μA
		$T_J = 25^\circ\text{C}$				
		$T_J = 125^\circ\text{C}$			-100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-1.0	-1.7	-3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.0		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -4.4\text{ A}$		33	45	$\text{m}\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -3.4\text{ A}$		52	75	
Forward Transconductance	g_{FS}	$V_{DS} = -15\text{ V}, I_D = -4.4\text{ A}$		7.7		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -24\text{ V}$		882	1500	pF
Output Capacitance	C_{OSS}			143		
Reverse Transfer Capacitance	C_{RSS}			105		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DD} = -15\text{ V}, I_D = -4.4\text{ A}$		18.2	28	nC
Gate-to-Source Charge	Q_{GS}			2.95		
Gate-to-Drain Charge	Q_{GD}			4.25		

SWITCHING CHARACTERISTICS, $V_{GS} = -10\text{ V}$ (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -10\text{ V}, V_{DD} = -15\text{ V}, I_D = -1.0\text{ A}, R_G = 6.0\text{ }\Omega$		9.0	18	ns
Rise Time	t_r			8.0	16	
Turn-Off Delay Time	$t_{d(OFF)}$			45	90	
Fall Time	t_f			26	52	

SWITCHING CHARACTERISTICS, $V_{GS} = -4.5\text{ V}$ (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -15\text{ V}, I_D = -1.0\text{ A}, R_G = 6.0\text{ }\Omega$		11		ns
Rise Time	t_r			14		
Turn-Off Delay Time	$t_{d(OFF)}$			32		
Fall Time	t_f			23		

DRAIN - SOURCE DIODE CHARACTERISTICS

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.1\text{ A}$		-0.76	-1.2	V
		$T_J = 25^\circ\text{C}$				
		$T_J = 125^\circ\text{C}$		-0.60		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = -1.1\text{ A}$		27	54	ns
Charge Time	t_a			10		
Discharge Time	t_b			17		
Reverse Recovery Charge	Q_{RR}			12		nC

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

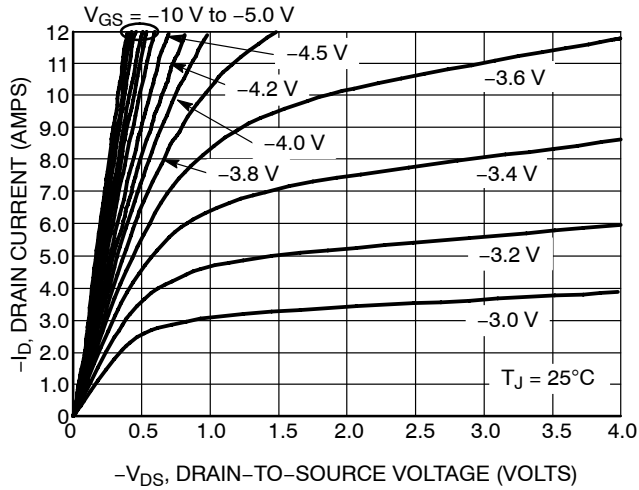


Figure 1. On-Region Characteristics

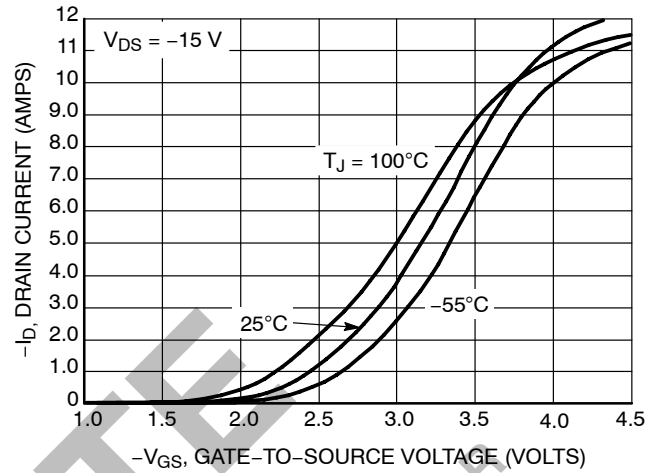


Figure 2. Transfer Characteristics

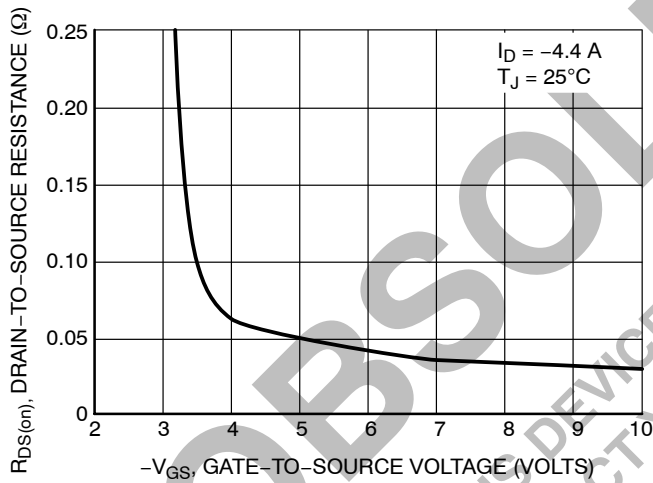


Figure 3. $R_{DS(on)}$ vs. V_{GS}

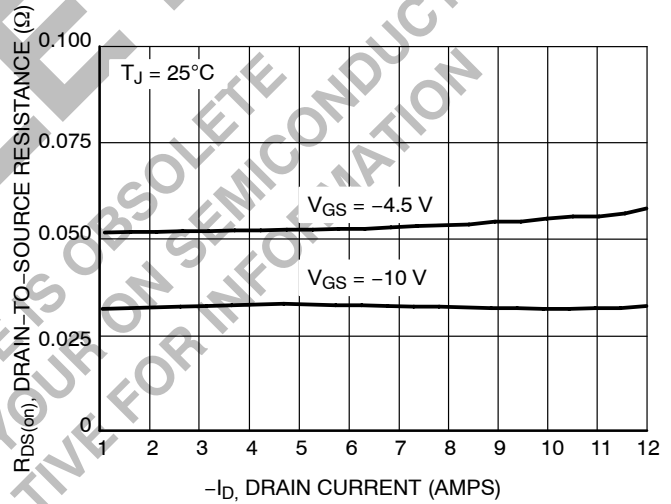


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

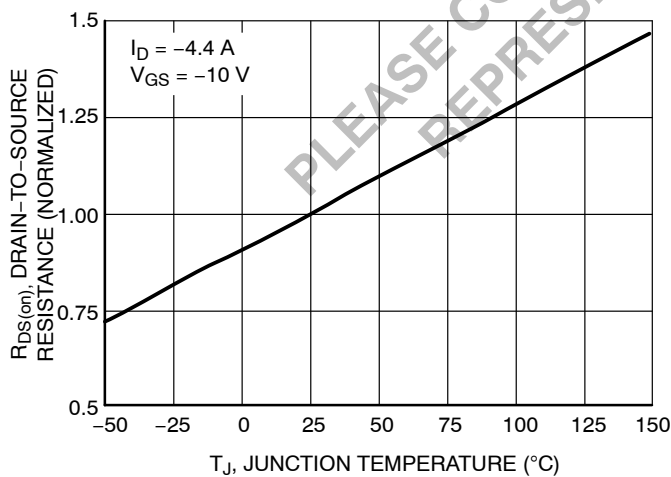


Figure 5. On-Resistance Variation with Temperature

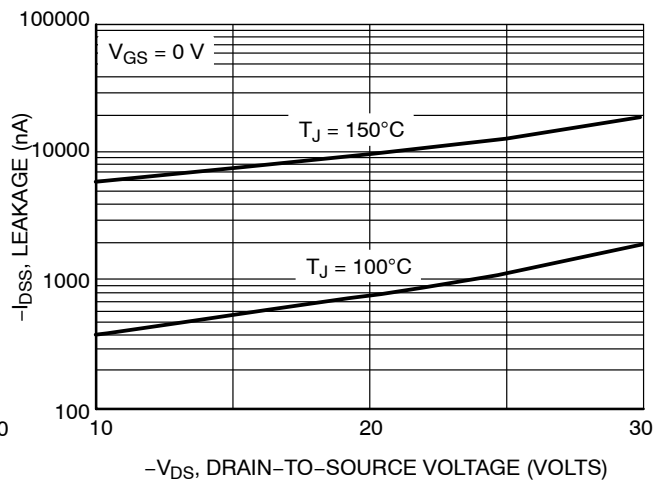
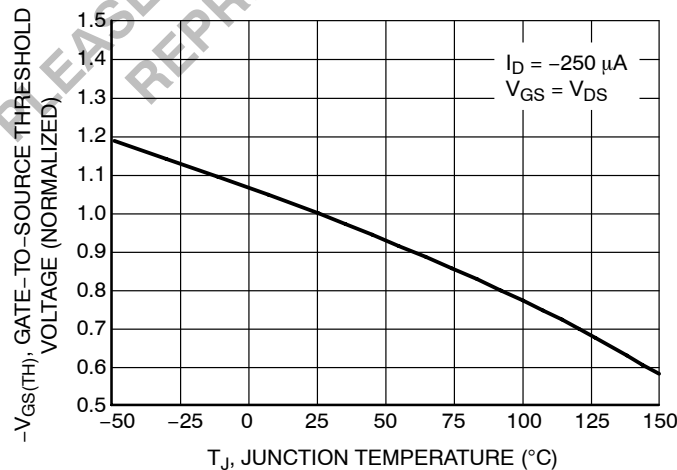
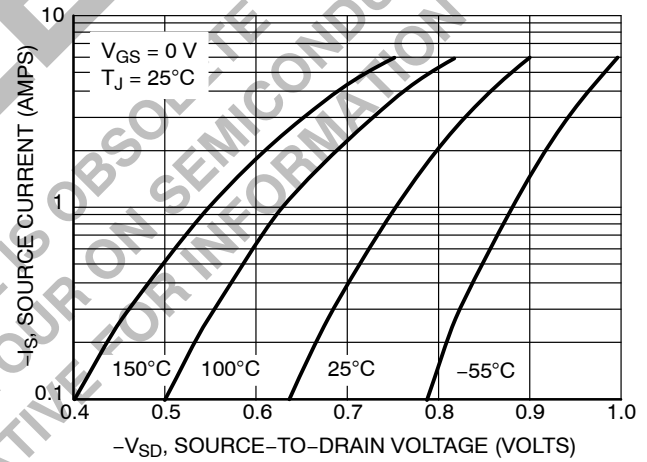
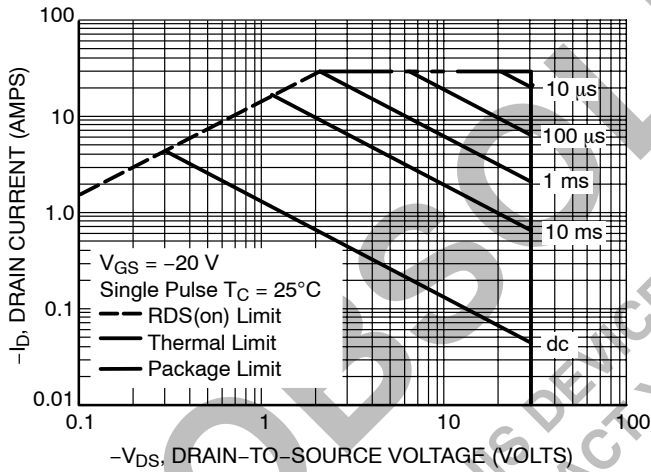
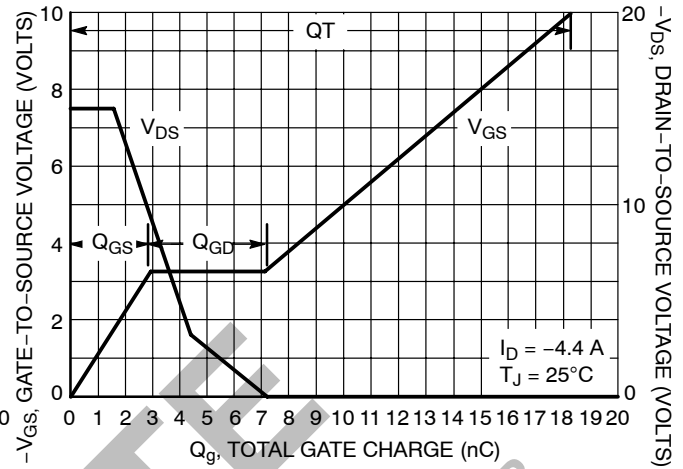
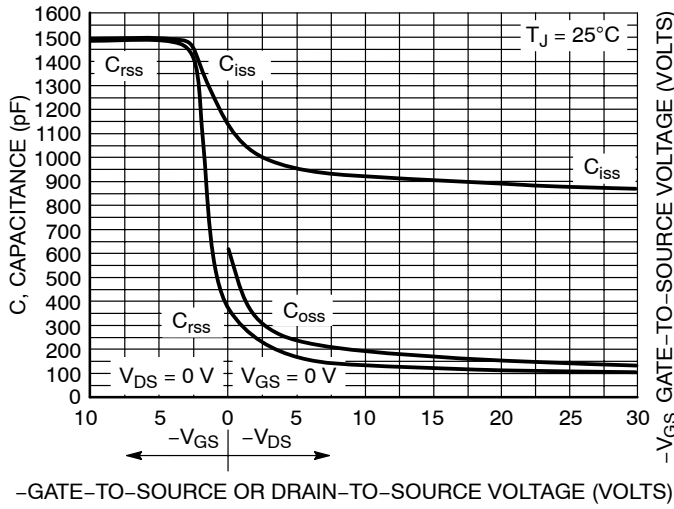
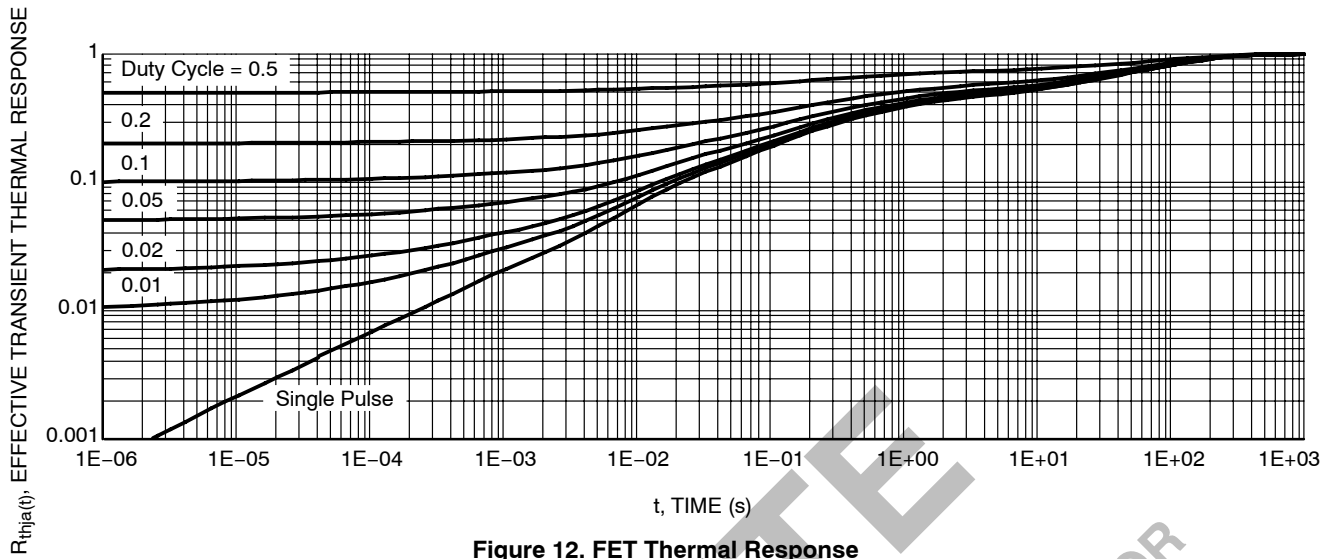


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

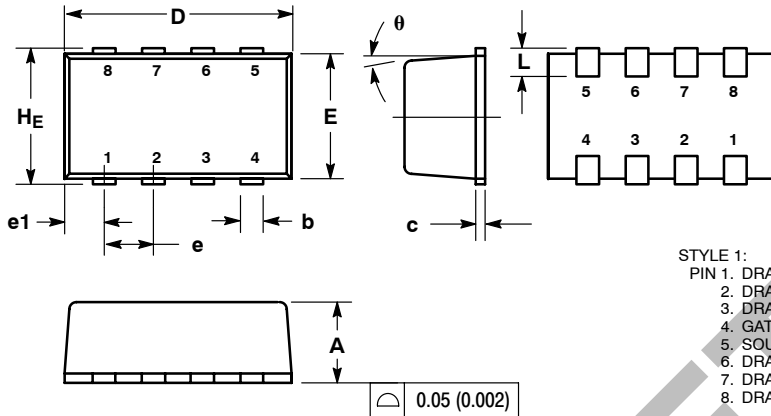




NTHS4111P

PACKAGE DIMENSIONS

ChipFET™ CASE 1206A-03 ISSUE G

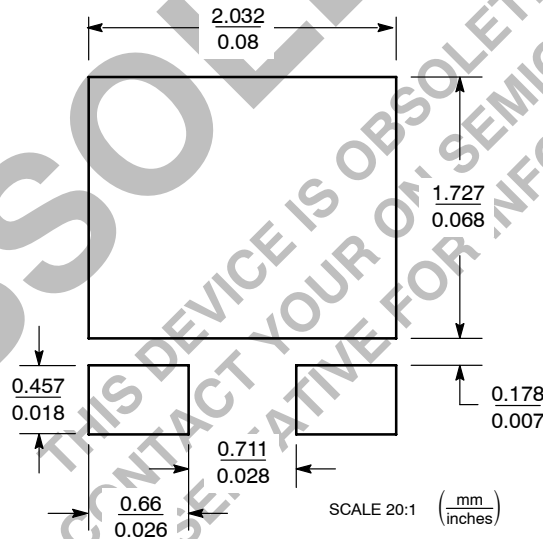


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
 4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
 5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
 6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5°TYP			5°TYP		

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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