

Radiation Hardened 8K x 8 CMOS PROM

The Intersil HS-6664RH is a radiation hardened 64K CMOS PROM, organized in an 8K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and utilizes synchronous circuit design techniques to achieve high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with microprocessors that use a multiplexed address/data bus structure. The output enable control ($\overline{G}$) simplifies system interfacing by allowing output data bus control in addition to the chip enable control ($\overline{E}$). All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Applications for the HS-6664RH CMOS PROM include low power microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, and processor control storage.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95626. A "hot-link" is provided on our homepage for downloading.
www.intersil.com/spacedefense/space.htm

Features

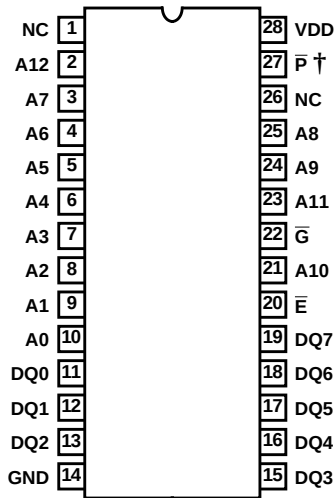
- Electrically Screened to SMD # 5962-95626
- QML Qualified per MIL-PRF-38535 Requirements
- 1.2 Micron Radiation Hardened Bulk CMOS
- Total Dose 300 krad(Si) (Max)
- Transient Output Upset. $>5 \times 10^8$ rad(Si)/s
- LET >100 MEV-cm²/mg
- Fast Access Time. 35ns (Typ)
- Single 5V Power Supply
- Single Pulse 10V Field Programmable
- Synchronous Operation
- On-Chip Address Latches
- Three-State Outputs
- NiCr Fuses
- Low Standby Current $<500\mu\text{A}$ (Pre-Rad)
- Low Operating Current. $<15\text{mA/MHz}$
- Military Temperature Range -55°C to 125°C

Ordering Information

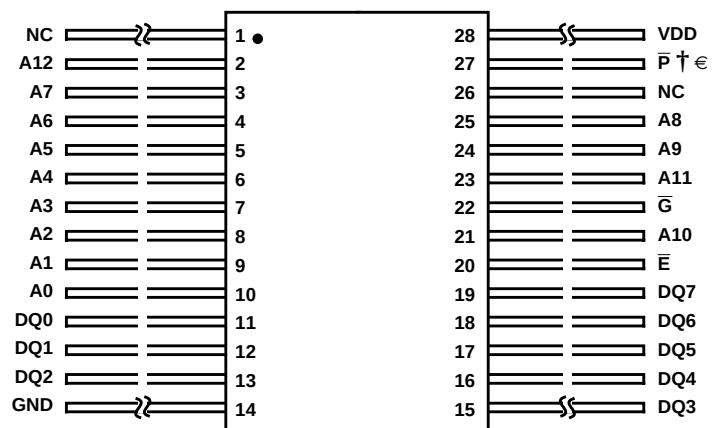
ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962F9562601QXC	HS1-6664RH-8	-55 to 125
5962F9562601QYC	HS9-6664RH-8	-55 to 125
5962F9562601VXC	HS1-6664RH-Q	-55 to 125
5962F9562601VYC	HS9-6664RH-Q	-55 to 125
HS1-6664RH/PROTO	HS1-6664RH/PROTO	-55 to 125
HS9-6664RH/PROTO	HS9-6664RH/PROTO	-55 to 125

Pinouts

28 LEAD CERAMIC (SBDIP)
CASE OUTLINE D28.6 MIL-STD-1835, CDIP2-T28
TOP VIEW

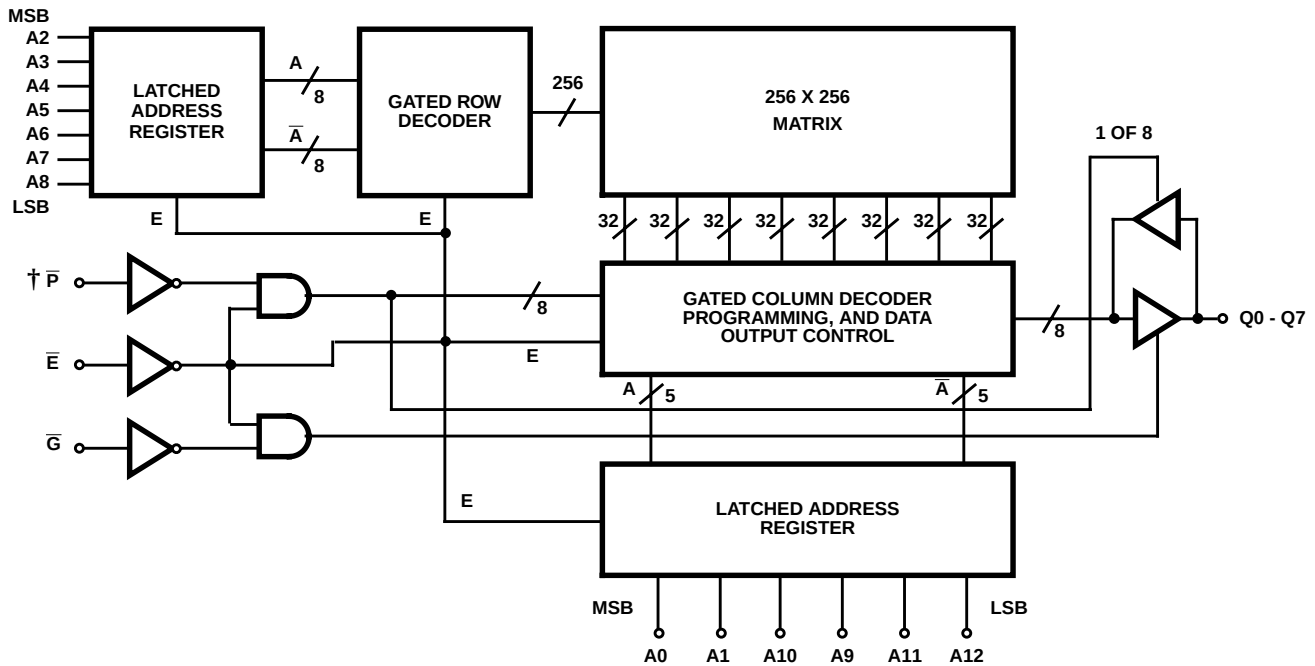


28 LEAD FLATPACK
CASE OUTLINE K28.A MIL-STD-1835, CDFP3-F28
TOP VIEW



† P must be hardwired at all times to VDD, except during programming.

Functional Diagram



NOTE: † P must be hardwired at all times to VDD, except during programming.

TRUTH TABLE

E	G	MODE
0	0	Enabled
0	1	Output Disabled
1	X	Disabled

Die Characteristics

DIE DIMENSIONS:

271mils x 307mils x 19mils ± 1 mils

INTERFACE MATERIALS:

Glassivation:

Type: SiO_2

Thickness: $8\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Top Metallization:

M1: $6\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$ Si/Al/Cu

$2\text{k}\text{\AA} \pm 500\text{\AA}$ TiW

M2: $10\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$ Si/Al/Cu

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

V_{DD}

ADDITIONAL INFORMATION:

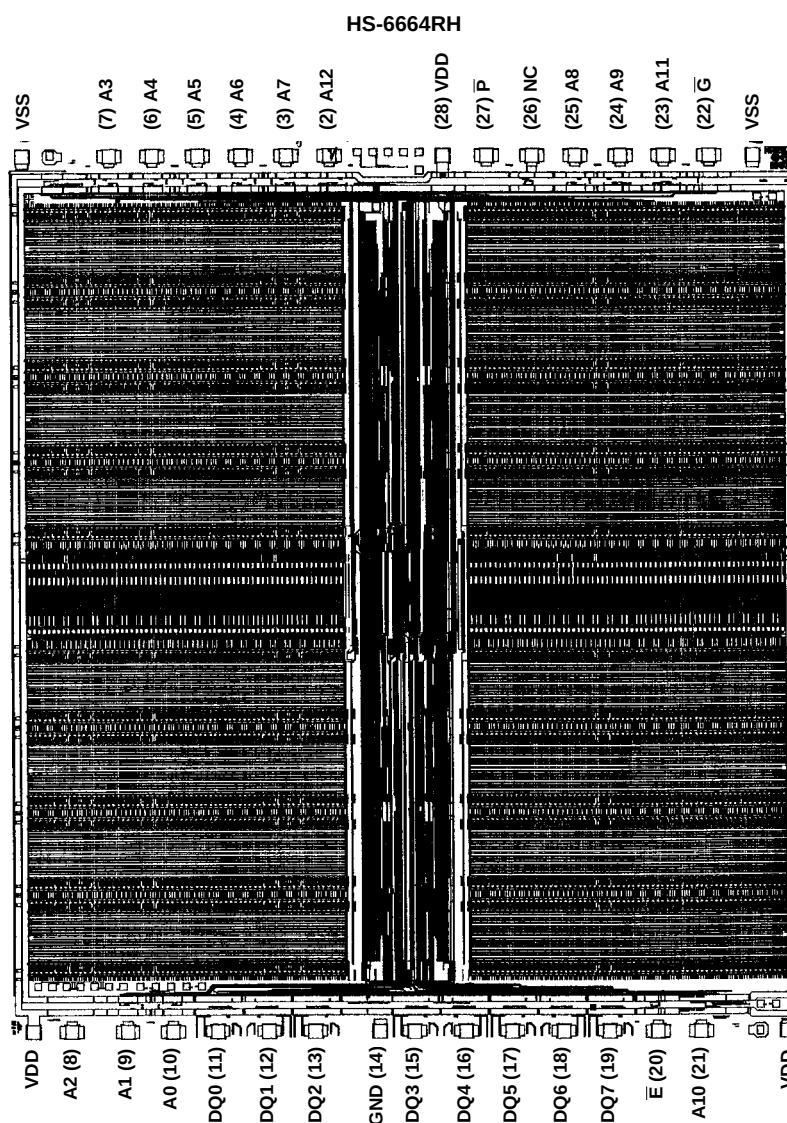
Worst Case Current Density:

$2 \times 10^5 \text{ A/cm}^2$

Transistor Count:

110, 874

Metallization Mask Layout



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