

## FEATURES

- Integrated Dual 12-Bit ADCs
- Sample Rate: 65Mps/40Mps/25Mps
- Single 3V Supply (2.7V to 3.4V)
- Low Power: 400mW/235mW/150mW
- 71dB SNR up to 70MHz Input
- 85dB SFDR up to 70MHz Input
- 110dB Channel Isolation at 100MHz
- Multiplexed or Separate Data Bus
- Flexible Input: 1V<sub>P-P</sub> to 2V<sub>P-P</sub> Range
- 575MHz Full Power Bandwidth S/H
- Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Pin Compatible Family
  - 80Mps: LTC2294 (12-Bit), LTC2299 (14-Bit)
  - 65Mps: LTC2293 (12-Bit), LTC2298 (14-Bit)
  - 40Mps: LTC2292 (12-Bit), LTC2297 (14-Bit)
  - 25Mps: LTC2291 (12-Bit), LTC2296 (14-Bit)
  - 10Mps: LTC2290 (12-Bit), LTC2295 (14-Bit)
- 64-Pin (9mm × 9mm) QFN Package

## APPLICATIONS

- Wireless and Wired Broadband Communication
- Imaging Systems
- Spectral Analysis
- Portable Instrumentation

## DESCRIPTION

The LTC®2293/LTC2292/LTC2291 are 12-bit 65Mps/40Mps/25Mps, low power dual 3V A/D converters designed for digitizing high frequency, wide dynamic range signals. The LTC2293/LTC2292/LTC2291 are perfect for demanding imaging and communications applications with AC performance that includes 71dB SNR and 85dB SFDR for signals well beyond the Nyquist frequency.

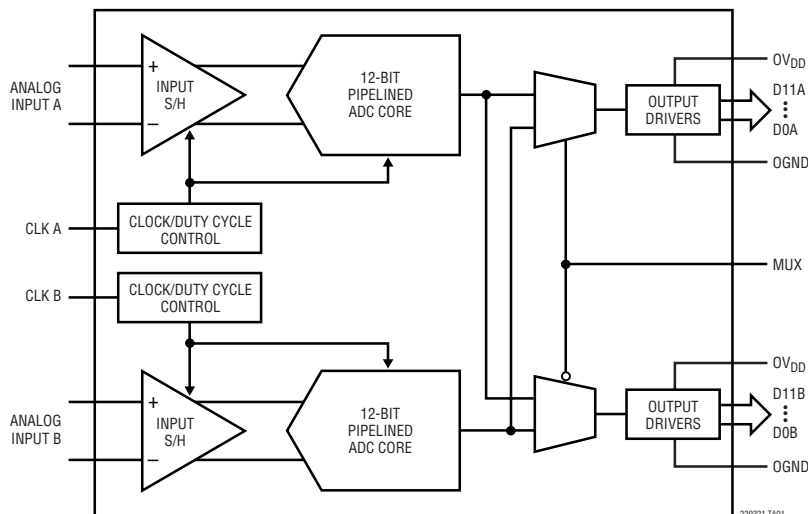
DC specs include  $\pm 0.3\text{LSB}$  INL (typ),  $\pm 0.15\text{LSB}$  DNL (typ) and no missing codes over temperature. The transition noise is a low  $0.25\text{LSB}_{\text{RMS}}$ .

A single 3V supply allows low power operation. A separate output supply allows the outputs to drive 0.5V to 3.3V logic. An optional multiplexer allows both channels to share a digital output bus.

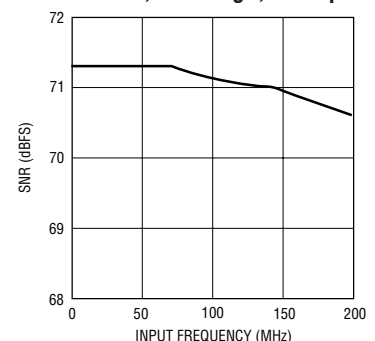
A single-ended CLK input controls converter operation. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

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## TYPICAL APPLICATION



**LTC2293: SNR vs Input Frequency, -1dB, 2V Range, 65Mps**



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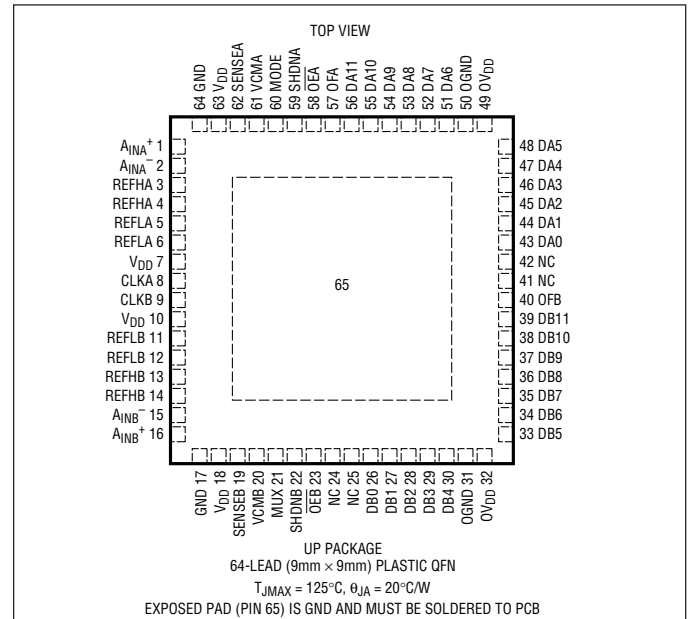
# LTC2293/LTC2292/LTC2291

## ABSOLUTE MAXIMUM RATINGS

$0V_{DD} = V_{DD}$  (Notes 1, 2)

|                                      |                               |
|--------------------------------------|-------------------------------|
| Supply Voltage ( $V_{DD}$ )          | 4V                            |
| Digital Output Ground Voltage (OGND) | –0.3V to 1V                   |
| Analog Input Voltage (Note 3)        | –0.3V to ( $V_{DD} + 0.3V$ )  |
| Digital Input Voltage                | –0.3V to ( $V_{DD} + 0.3V$ )  |
| Digital Output Voltage               | –0.3V to ( $0V_{DD} + 0.3V$ ) |
| Power Dissipation                    | 1500mW                        |
| Operating Temperature Range          |                               |
| LTC2293C, LTC2292C, LTC2291C         | 0°C to 70°C                   |
| LTC2293I, LTC2292I, LTC2291I         | –40°C to 85°C                 |
| Storage Temperature Range            | –65°C to 125°C                |
| Lead Temperature (Soldering, 10 sec) | 300°C                         |

## PACKAGE/ORDER INFORMATION



| ORDER PART NUMBER | QFN PART* MARKING |
|-------------------|-------------------|
| LTC2293CUP        | LTC2293UP         |
| LTC2293IUP        | LTC2292UP         |
| LTC2292CUP        | LTC2291UP         |
| LTC2292IUP        |                   |
| LTC2291CUP        |                   |
| LTC2291IUP        |                   |

Consult LTC Marketing for parts specified with wider operating temperature ranges.  
\*The temperature grade is identified by a label on the shipping container.

## CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ . (Note 4)

| PARAMETER                     | CONDITIONS                         |   | LTC2293 |       |     | LTC2292 |       |     | LTC2291 |       |     | UNITS              |
|-------------------------------|------------------------------------|---|---------|-------|-----|---------|-------|-----|---------|-------|-----|--------------------|
|                               |                                    |   | MIN     | TYP   | MAX | MIN     | TYP   | MAX | MIN     | TYP   | MAX |                    |
| Resolution (No Missing Codes) |                                    | ● | 12      |       |     | 12      |       |     | 12      |       |     | Bits               |
| Integral Linearity Error      | Differential Analog Input (Note 5) | ● | –1.4    | ±0.3  | 1.4 | –1.4    | ±0.3  | 1.4 | –1.3    | ±0.3  | 1.3 | LSB                |
| Differential Linearity Error  | Differential Analog Input          | ● | –0.8    | ±0.15 | 0.8 | –0.7    | ±0.15 | 0.7 | –0.7    | ±0.15 | 0.7 | LSB                |
| Offset Error                  | (Note 6)                           | ● | –12     | ±2    | 12  | –12     | ±2    | 12  | –12     | ±2    | 12  | mV                 |
| Gain Error                    | External Reference                 | ● | –2.5    | ±0.5  | 2.5 | –2.5    | ±0.5  | 2.5 | –2.5    | ±0.5  | 2.5 | %FS                |
| Offset Drift                  |                                    |   |         | ±10   |     |         | ±10   |     |         | ±10   |     | μV/°C              |
| Full-Scale Drift              | Internal Reference                 |   |         | ±30   |     |         | ±30   |     |         | ±30   |     | ppm/°C             |
|                               | External Reference                 |   |         | ±15   |     |         | ±15   |     |         | ±15   |     | ppm/°C             |
| Gain Matching                 | External Reference                 |   |         | ±0.3  |     |         | ±0.3  |     |         | ±0.3  |     | %FS                |
| Offset Matching               |                                    |   |         | ±2    |     |         | ±2    |     |         | ±2    |     | mV                 |
| Transition Noise              | SENSE = 1V                         |   |         | 0.25  |     |         | 0.25  |     |         | 0.25  |     | LSB <sub>RMS</sub> |

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## ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

| SYMBOL       | PARAMETER                                     | CONDITIONS                               |   | MIN      | TYP | MAX | UNITS          |
|--------------|-----------------------------------------------|------------------------------------------|---|----------|-----|-----|----------------|
| $V_{IN}$     | Analog Input Range ( $A_{IN}^+ - A_{IN}^-$ )  | $2.7V < V_{DD} < 3.4V$ (Note 7)          | ● | 1V to 2V |     |     | V              |
| $V_{IN,CM}$  | Analog Input Common Mode                      | Differential Input (Note 7)              | ● | 1        | 1.5 | 1.9 | V              |
| $I_{IN}$     | Analog Input Leakage Current                  | $0V < A_{IN}^+, A_{IN}^- < V_{DD}$       | ● | -1       |     | 1   | $\mu\text{A}$  |
| $I_{SENSE}$  | SENSEA, SENSEB Input Leakage                  | $0V < \text{SENSEA}, \text{SENSEB} < 1V$ | ● | -3       |     | 3   | $\mu\text{A}$  |
| $I_{MODE}$   | MODE Input Leakage Current                    | $0V < \text{MODE} < V_{DD}$              | ● | -3       |     | 3   | $\mu\text{A}$  |
| $t_{AP}$     | Sample-and-Hold Acquisition Delay Time        |                                          |   |          | 0   |     | ns             |
| $t_{JITTER}$ | Sample-and-Hold Acquisition Delay Time Jitter |                                          |   |          | 0.2 |     | $\text{pSRMS}$ |
| CMRR         | Analog Input Common Mode Rejection Ratio      |                                          |   |          | 80  |     | dB             |
|              | Full Power Bandwidth                          | Figure 8 Test Circuit                    |   |          | 575 |     | MHz            |

## DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $A_{IN} = -1\text{dBFS}$ . (Note 4)

| SYMBOL   | PARAMETER                                          | CONDITIONS                                              |   | LTC2293 |      |     | LTC2292 |      |     | LTC2291 |      |     | UNITS |
|----------|----------------------------------------------------|---------------------------------------------------------|---|---------|------|-----|---------|------|-----|---------|------|-----|-------|
|          |                                                    |                                                         |   | MIN     | TYP  | MAX | MIN     | TYP  | MAX | MIN     | TYP  | MAX |       |
| SNR      | Signal-to-Noise Ratio                              | 5MHz Input                                              |   | 71.3    |      |     | 71.4    |      |     | 71.4    |      |     | dB    |
|          |                                                    | 12.5MHz Input                                           | ● |         |      |     |         |      |     | 70.1    | 71.2 |     | dB    |
|          |                                                    | 20MHz Input                                             | ● |         |      |     | 69.6    | 71.3 |     |         |      |     | dB    |
|          |                                                    | 30MHz Input                                             | ● | 69.6    | 71.3 |     |         |      |     |         |      |     | dB    |
|          |                                                    | 70MHz Input                                             |   | 71.3    |      |     | 71.1    |      |     | 70.9    |      |     | dB    |
|          |                                                    | 140MHz Input                                            |   | 71      |      |     | 70.7    |      |     | 70.6    |      |     | dB    |
| SFDR     | Spurious Free Dynamic Range 2nd or 3rd Harmonic    | 5MHz Input                                              |   | 90      |      |     | 90      |      |     | 90      |      |     | dB    |
|          |                                                    | 12.5MHz Input                                           | ● |         |      |     |         |      |     | 75      | 90   |     | dB    |
|          |                                                    | 20MHz Input                                             | ● |         |      |     | 74      | 90   |     |         |      |     | dB    |
|          |                                                    | 30MHz Input                                             | ● | 74      | 90   |     |         |      |     |         |      |     | dB    |
|          |                                                    | 70MHz Input                                             |   | 85      |      |     | 85      |      |     | 85      |      |     | dB    |
|          |                                                    | 140MHz Input                                            |   | 80      |      |     | 80      |      |     | 80      |      |     | dB    |
| SFDR     | Spurious Free Dynamic Range 4th Harmonic or Higher | 5MHz Input                                              |   | 90      |      |     | 90      |      |     | 90      |      |     | dB    |
|          |                                                    | 12.5MHz Input                                           | ● |         |      |     |         |      |     | 80      | 90   |     | dB    |
|          |                                                    | 20MHz Input                                             | ● |         |      |     | 79      | 90   |     |         |      |     | dB    |
|          |                                                    | 30MHz Input                                             | ● | 78      | 90   |     |         |      |     |         |      |     | dB    |
|          |                                                    | 70MHz Input                                             |   | 90      |      |     | 90      |      |     | 90      |      |     | dB    |
|          |                                                    | 140MHz Input                                            |   | 90      |      |     | 90      |      |     | 90      |      |     | dB    |
| S/(N+D)  | Signal-to-Noise Plus Distortion Ratio              | 5MHz Input                                              |   | 71.3    |      |     | 71.4    |      |     | 71.4    |      |     | dB    |
|          |                                                    | 12.5MHz Input                                           | ● |         |      |     |         |      |     | 69.8    | 71.2 |     | dB    |
|          |                                                    | 20MHz Input                                             | ● |         |      |     | 69.4    | 71.2 |     |         |      |     | dB    |
|          |                                                    | 30MHz Input                                             | ● | 69.4    | 71.2 |     |         |      |     |         |      |     | dB    |
|          |                                                    | 70MHz Input                                             |   | 71.1    |      |     | 70.9    |      |     | 70.8    |      |     | dB    |
|          |                                                    | 140MHz Input                                            |   | 69.9    |      |     | 69.9    |      |     | 69.8    |      |     | dB    |
| $I_{MD}$ | Intermodulation Distortion                         | $f_{IN} = \text{Nyquist}, \text{Nyquist} + 1\text{MHz}$ |   | 90      |      |     | 90      |      |     | 90      |      |     | dB    |
|          | Crosstalk                                          | $f_{IN} = \text{Nyquist}$                               |   | -110    |      |     | -110    |      |     | -110    |      |     | dB    |

**INTERNAL REFERENCE CHARACTERISTICS** (Note 4)

| PARAMETER                  | CONDITIONS             | MIN   | TYP   | MAX   | UNITS  |
|----------------------------|------------------------|-------|-------|-------|--------|
| $V_{CM}$ Output Voltage    | $I_{OUT} = 0$          | 1.475 | 1.500 | 1.525 | V      |
| $V_{CM}$ Output Tempco     |                        |       | ±30   |       | ppm/°C |
| $V_{CM}$ Line Regulation   | $2.7V < V_{DD} < 3.3V$ |       | 3     |       | mV/V   |
| $V_{CM}$ Output Resistance | $-1mA < I_{OUT} < 1mA$ |       | 4     |       | Ω      |

**DIGITAL INPUTS AND DIGITAL OUTPUTS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

| SYMBOL                                                           | PARAMETER                 | CONDITIONS                             | MIN | TYP  | MAX           | UNITS  |
|------------------------------------------------------------------|---------------------------|----------------------------------------|-----|------|---------------|--------|
| <b>LOGIC INPUTS (CLK, <math>\overline{OE}</math>, SHDN, MUX)</b> |                           |                                        |     |      |               |        |
| $V_{IH}$                                                         | High Level Input Voltage  | $V_{DD} = 3V$                          | ●   | 2    |               | V      |
| $V_{IL}$                                                         | Low Level Input Voltage   | $V_{DD} = 3V$                          | ●   |      | 0.8           | V      |
| $I_{IN}$                                                         | Input Current             | $V_{IN} = 0V$ to $V_{DD}$              | ●   | -10  | 10            | μA     |
| $C_{IN}$                                                         | Input Capacitance         | (Note 7)                               |     | 3    |               | pF     |
| <b>LOGIC OUTPUTS</b>                                             |                           |                                        |     |      |               |        |
| <b><math>OV_{DD} = 3V</math></b>                                 |                           |                                        |     |      |               |        |
| $C_{OZ}$                                                         | Hi-Z Output Capacitance   | $\overline{OE} = \text{High}$ (Note 7) |     | 3    |               | pF     |
| $I_{SOURCE}$                                                     | Output Source Current     | $V_{OUT} = 0V$                         |     | 50   |               | mA     |
| $I_{SINK}$                                                       | Output Sink Current       | $V_{OUT} = 3V$                         |     | 50   |               | mA     |
| $V_{OH}$                                                         | High Level Output Voltage | $I_O = -10\mu A$<br>$I_O = -200\mu A$  | ●   | 2.7  | 2.995<br>2.99 | V<br>V |
| $V_{OL}$                                                         | Low Level Output Voltage  | $I_O = 10\mu A$<br>$I_O = 1.6mA$       | ●   |      | 0.005<br>0.09 | V<br>V |
| <b><math>OV_{DD} = 2.5V</math></b>                               |                           |                                        |     |      |               |        |
| $V_{OH}$                                                         | High Level Output Voltage | $I_O = -200\mu A$                      |     | 2.49 |               | V      |
| $V_{OL}$                                                         | Low Level Output Voltage  | $I_O = 1.6mA$                          |     | 0.09 |               | V      |
| <b><math>OV_{DD} = 1.8V</math></b>                               |                           |                                        |     |      |               |        |
| $V_{OH}$                                                         | High Level Output Voltage | $I_O = -200\mu A$                      |     | 1.79 |               | V      |
| $V_{OL}$                                                         | Low Level Output Voltage  | $I_O = 1.6mA$                          |     | 0.09 |               | V      |

**POWER REQUIREMENTS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 8)

| SYMBOL     | PARAMETER                     | CONDITIONS                                              |   | LTC2293 |     |     | LTC2292 |     |     | LTC2291 |     |     | UNITS |
|------------|-------------------------------|---------------------------------------------------------|---|---------|-----|-----|---------|-----|-----|---------|-----|-----|-------|
|            |                               |                                                         |   | MIN     | TYP | MAX | MIN     | TYP | MAX | MIN     | TYP | MAX |       |
| $V_{DD}$   | Analog Supply Voltage         | (Note 9)                                                | ● | 2.7     | 3   | 3.4 | 2.7     | 3   | 3.4 | 2.7     | 3   | 3.4 | V     |
| $OV_{DD}$  | Output Supply Voltage         | (Note 9)                                                | ● | 0.5     | 3   | 3.6 | 0.5     | 3   | 3.6 | 0.5     | 3   | 3.6 | V     |
| $I_{VDD}$  | Supply Current                | Both ADCs at $f_{S(MAX)}$                               | ● |         | 133 | 150 |         | 78  | 95  |         | 50  | 60  | mA    |
| $P_{DISS}$ | Power Dissipation             | Both ADCs at $f_{S(MAX)}$                               | ● |         | 400 | 450 |         | 235 | 285 |         | 150 | 180 | mW    |
| $P_{SHDN}$ | Shutdown Power (Each Channel) | $\overline{SHDN} = H$ ,<br>$\overline{OE} = H$ , No CLK |   |         | 2   |     |         | 2   |     |         | 2   |     | mW    |
| $P_{NAP}$  | Nap Mode Power (Each Channel) | $\overline{SHDN} = H$ ,<br>$\overline{OE} = L$ , No CLK |   |         | 15  |     |         | 15  |     |         | 15  |     | mW    |

**TIMING CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

| SYMBOL           | PARAMETER                                         | CONDITIONS                        |   | LTC2293 |     |     | LTC2292 |      |     | LTC2291 |     |     | UNITS  |
|------------------|---------------------------------------------------|-----------------------------------|---|---------|-----|-----|---------|------|-----|---------|-----|-----|--------|
|                  |                                                   |                                   |   | MIN     | TYP | MAX | MIN     | TYP  | MAX | MIN     | TYP | MAX |        |
| $f_s$            | Sampling Frequency                                | (Note 9)                          | ● | 1       |     | 65  | 1       |      | 40  | 1       |     | 25  | MHz    |
| $t_L$            | CLK Low Time                                      | Duty Cycle Stabilizer Off         | ● | 7.3     | 7.7 | 500 | 11.8    | 12.5 | 500 | 18.9    | 20  | 500 | ns     |
|                  |                                                   | Duty Cycle Stabilizer On (Note 7) | ● | 5       | 7.7 | 500 | 5       | 12.5 | 500 | 5       | 20  | 500 | ns     |
| $t_H$            | CLK High Time                                     | Duty Cycle Stabilizer Off         | ● | 7.3     | 7.7 | 500 | 11.8    | 12.5 | 500 | 18.9    | 20  | 500 | ns     |
|                  |                                                   | Duty Cycle Stabilizer On (Note 7) | ● | 5       | 7.7 | 500 | 5       | 12.5 | 500 | 5       | 20  | 500 | ns     |
| $t_{AP}$         | Sample-and-Hold Aperture Delay                    |                                   |   |         | 0   |     |         | 0    |     |         | 0   |     | ns     |
| $t_D$            | CLK to DATA Delay                                 | $C_L = 5\text{pF}$ (Note 7)       | ● | 1.4     | 2.7 | 5.4 | 1.4     | 2.7  | 5.4 | 1.4     | 2.7 | 5.4 | ns     |
| $t_{MD}$         | MUX to DATA Delay                                 | $C_L = 5\text{pF}$ (Note 7)       | ● | 1.4     | 2.7 | 5.4 | 1.4     | 2.7  | 5.4 | 1.4     | 2.7 | 5.4 | ns     |
|                  | Data Access Time After $\overline{OE} \downarrow$ | $C_L = 5\text{pF}$ (Note 7)       | ● |         | 4.3 | 10  |         | 4.3  | 10  |         | 4.3 | 10  | ns     |
|                  | BUS Relinquish Time                               | (Note 7)                          | ● |         | 3.3 | 8.5 |         | 3.3  | 8.5 |         | 3.3 | 8.5 | ns     |
| Pipeline Latency |                                                   |                                   |   |         | 6   |     |         | 6    |     |         | 6   |     | Cycles |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

**Note 3:** When these pin voltages are taken below GND or above  $V_{DD}$ , they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above  $V_{DD}$  without latchup.

**Note 4:**  $V_{DD} = 3\text{V}$ ,  $f_{SAMPLE} = 65\text{MHz}$  (LTC2293), 40MHz (LTC2292), or 25MHz (LTC2291), input range =  $2V_{P-P}$  with differential drive, unless otherwise noted.

**Note 5:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 6:** Offset error is the offset voltage measured from  $-0.5\text{ LSB}$  when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

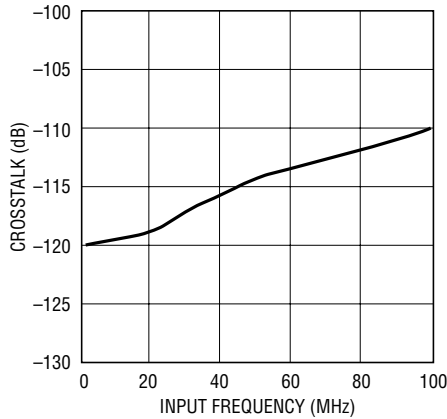
**Note 7:** Guaranteed by design, not subject to test.

**Note 8:**  $V_{DD} = 3\text{V}$ ,  $f_{SAMPLE} = 65\text{MHz}$  (LTC2293), 40MHz (LTC2292), or 25MHz (LTC2291), input range =  $1V_{P-P}$  with differential drive. The supply current and power dissipation are the sum total for both channels with both channels active.

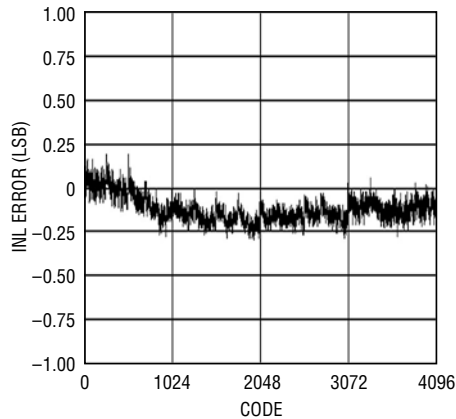
**Note 9:** Recommended operating conditions.

## TYPICAL PERFORMANCE CHARACTERISTICS

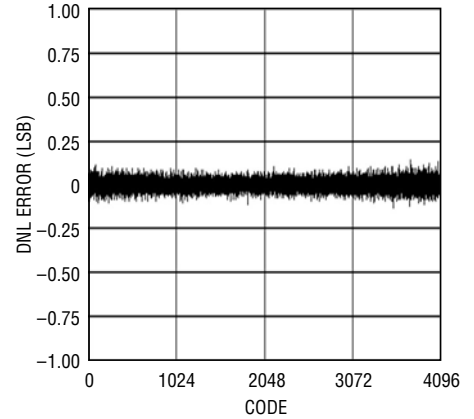
**LTC2293/LTC2292/LTC2291:  
Crosstalk vs Input Frequency**



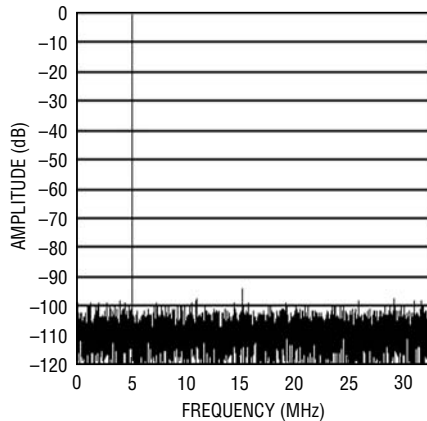
**LTC2293: Typical INL,  
2V Range, 65Msps**



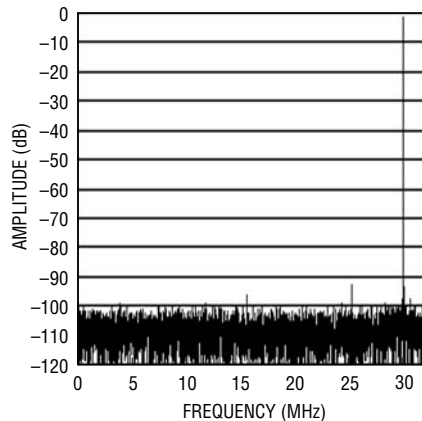
**LTC2293: Typical DNL,  
2V Range, 65Msps**



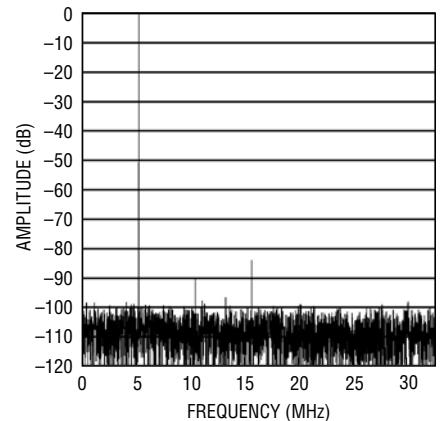
**LTC2293: 8192 Point FFT,  
 $f_{IN} = 5\text{MHz}$ , -1dB, 2V Range,  
65Msps**



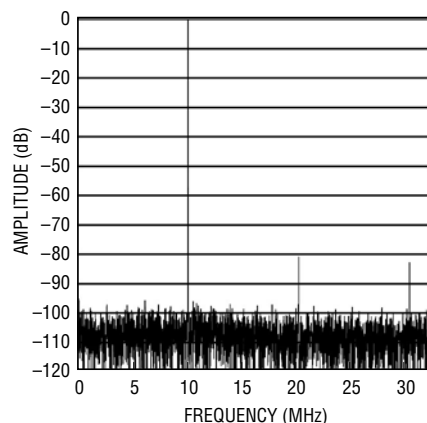
**LTC2293: 8192 Point FFT,  
 $f_{IN} = 30\text{MHz}$ , -1dB, 2V Range,  
65Msps**



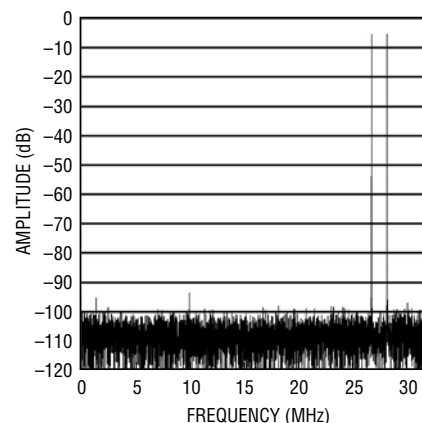
**LTC2293: 8192 Point FFT,  
 $f_{IN} = 70\text{MHz}$ , -1dB, 2V Range,  
65Msps**



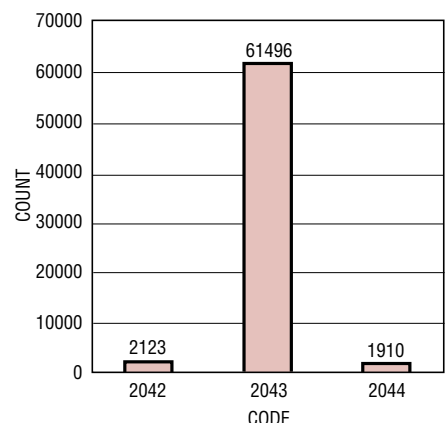
**LTC2293: 8192 Point FFT,  
 $f_{IN} = 140\text{MHz}$ , -1dB, 2V Range,  
65Msps**



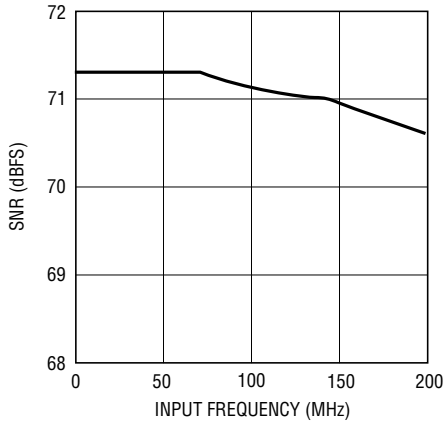
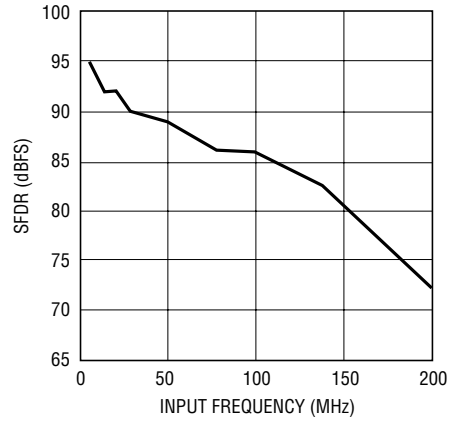
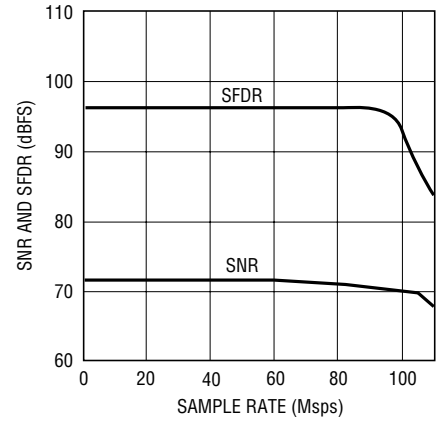
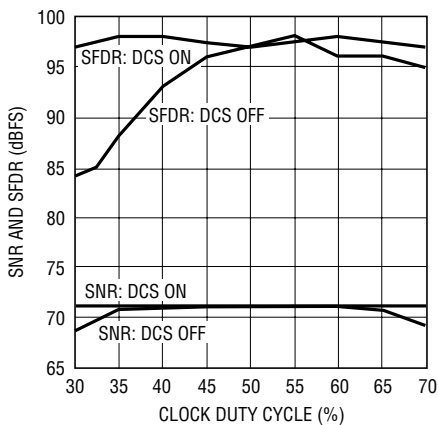
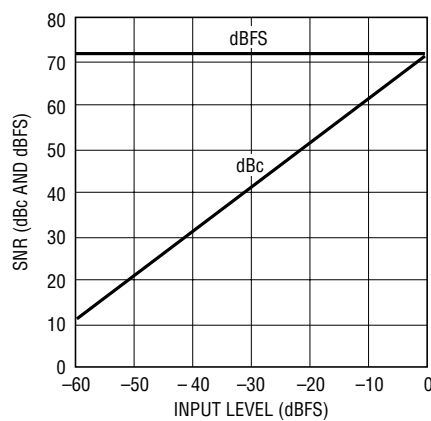
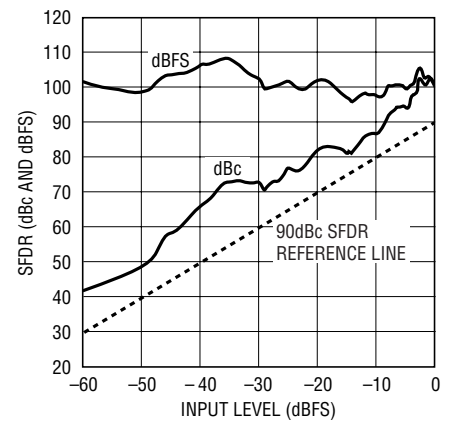
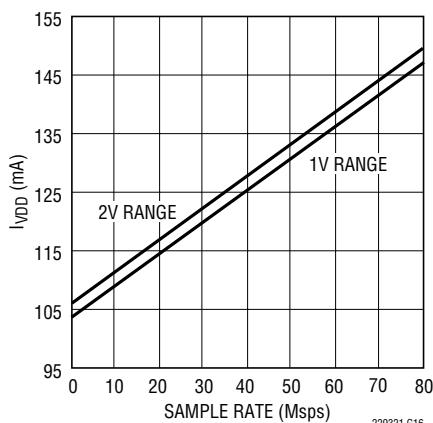
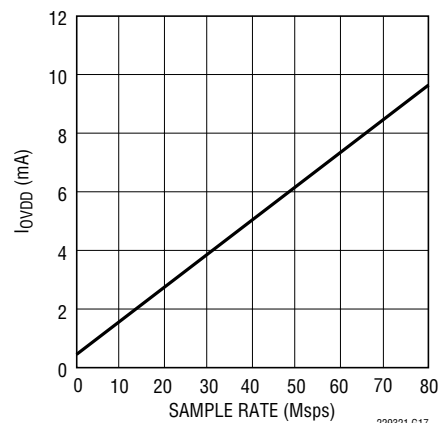
**LTC2293: 8192 Point 2-Tone FFT,  
 $f_{IN} = 28.2\text{MHz}$  and  $26.8\text{MHz}$ , -1dB,  
2V Range 65Msps**



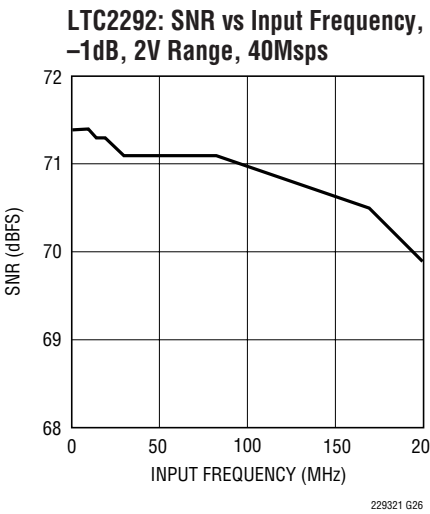
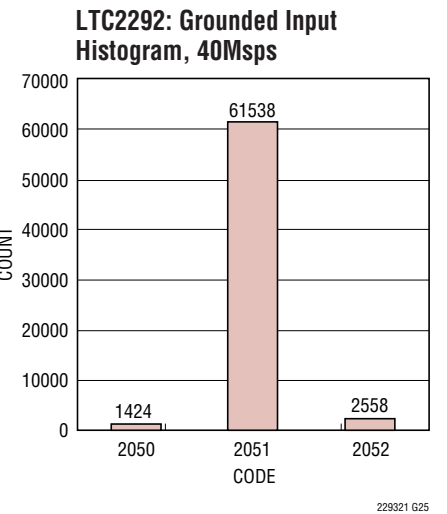
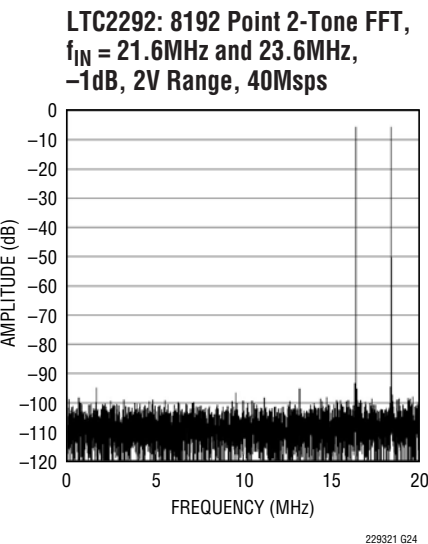
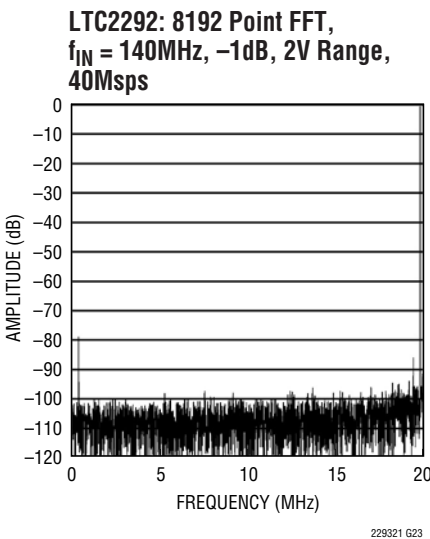
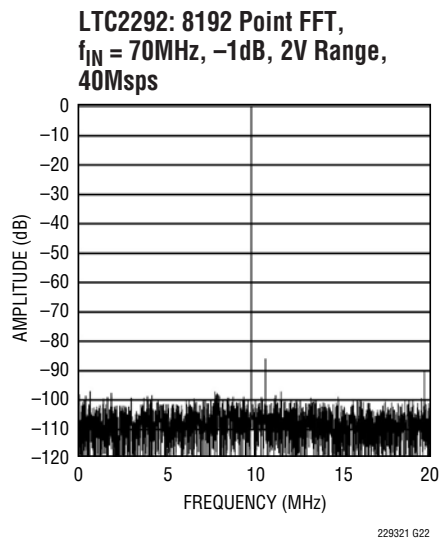
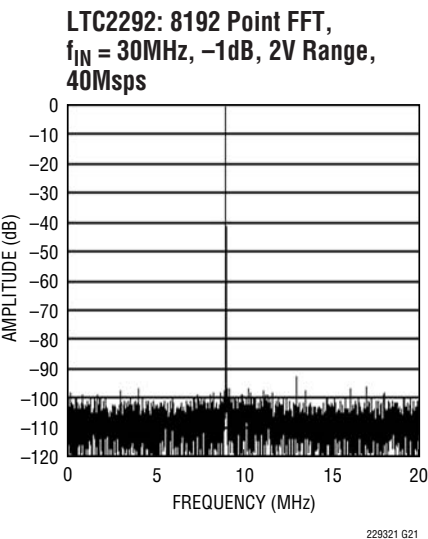
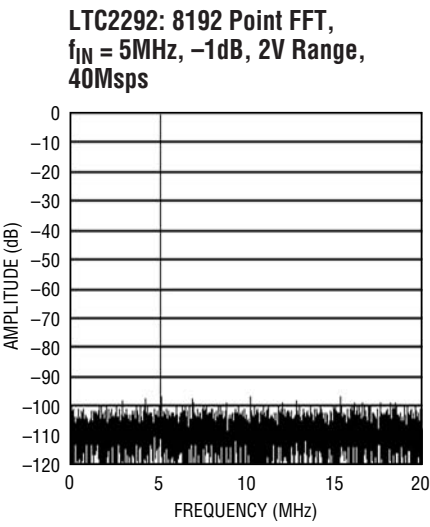
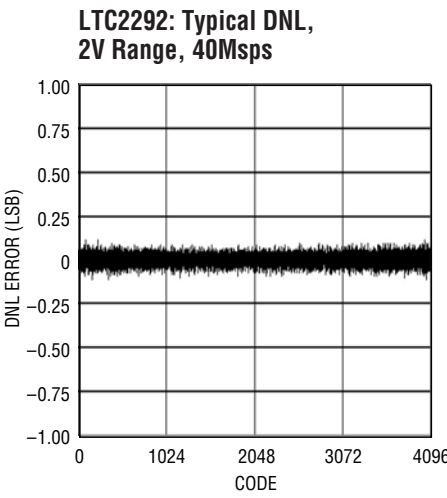
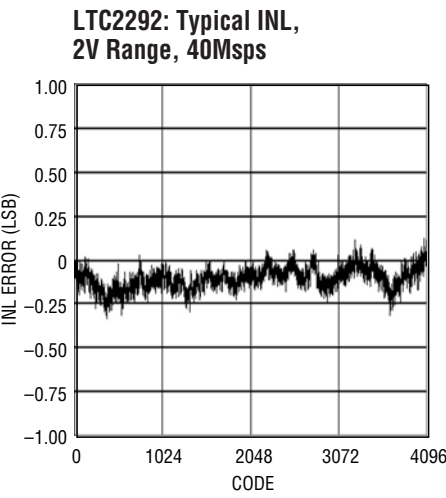
**LTC2293: Grounded Input  
Histogram, 65Msps**



## TYPICAL PERFORMANCE CHARACTERISTICS

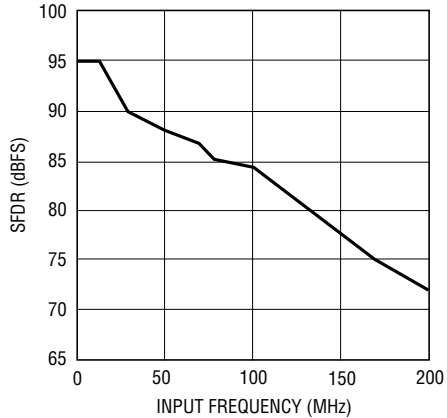
LTC2293: SNR vs Input Frequency,  
-1dB, 2V Range, 65MpsLTC2293: SFDR vs Input Frequency,  
-1dB, 2V Range, 65MpsLTC2293: SNR and SFDR vs  
Sample Rate, 2V Range,  
 $f_{IN} = 5\text{MHz}$ , -1dBLTC2293: SNR and SFDR vs  
Clock Duty Cycle, 65MpsLTC2293: SNR vs Input Level,  
 $f_{IN} = 30\text{MHz}$ , 2V Range, 65MpsLTC2293: SFDR vs Input Level,  
 $f_{IN} = 30\text{MHz}$ , 2V Range, 65MpsLTC2293:  $I_{VDD}$  vs Sample Rate,  
5MHz Sine Wave Input, -1dBLTC2293:  $I_{OVD}$  vs Sample Rate,  
5MHz Sine Wave Input, -1dB,  
 $O_{VDD} = 1.8\text{V}$ 

TYPICAL PERFORMANCE CHARACTERISTICS

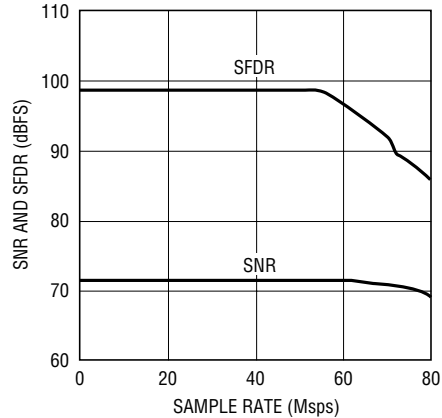


# TYPICAL PERFORMANCE CHARACTERISTICS

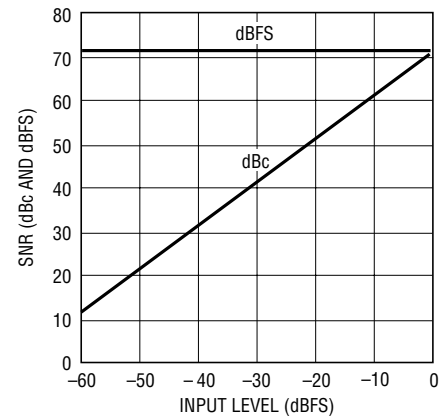
**LTC2292: SFDR vs Input Frequency,**  
-1dB, 2V Range, 40Mpsps



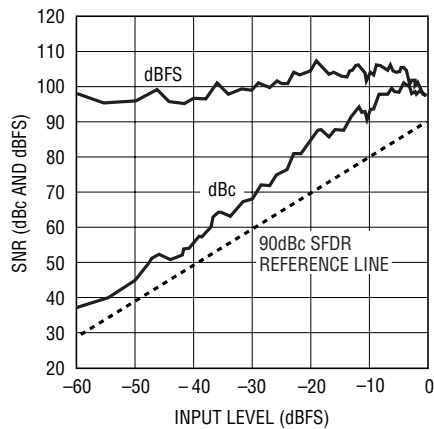
**LTC2292: SNR and SFDR vs**  
Sample Rate, 2V Range,  
 $f_{IN} = 5\text{MHz}$ , -1dB



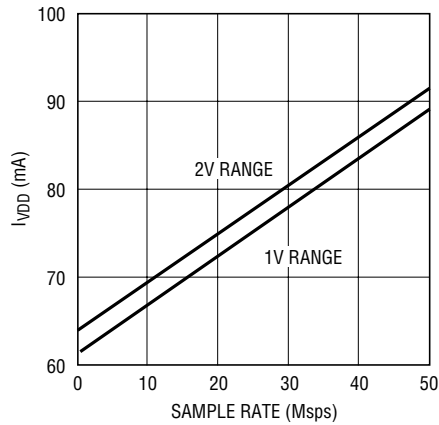
**LTC2292: SNR vs Input Level,**  
 $f_{IN} = 5\text{MHz}$ , 2V Range, 40Mpsps



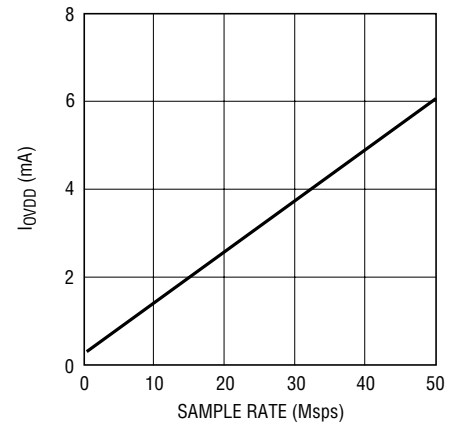
**LTC2292: SFDR vs Input Level,**  
 $f_{IN} = 5\text{MHz}$ , 2V Range, 40Mpsps



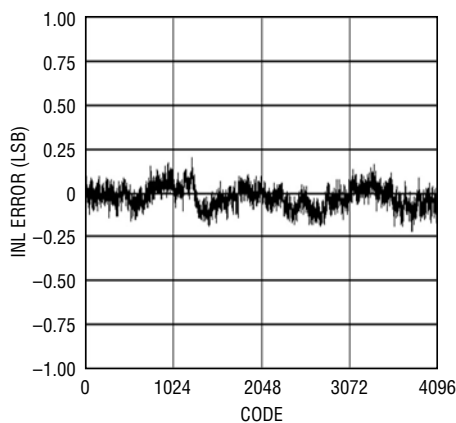
**LTC2292:  $I_{VDD}$  vs Sample Rate,**  
5MHz Sine Wave Input, -1dB



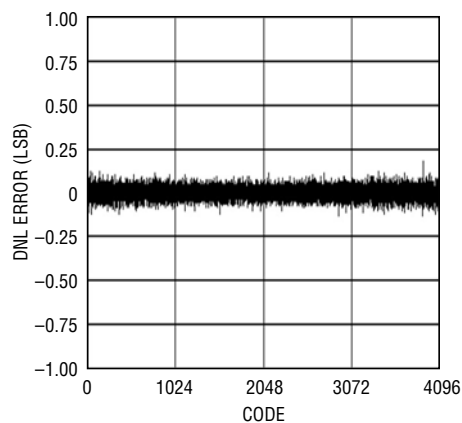
**LTC2292:  $I_{OVD}$  vs Sample Rate,**  
5MHz Sine Wave Input, -1dB,  
 $V_{DD} = 1.8\text{V}$



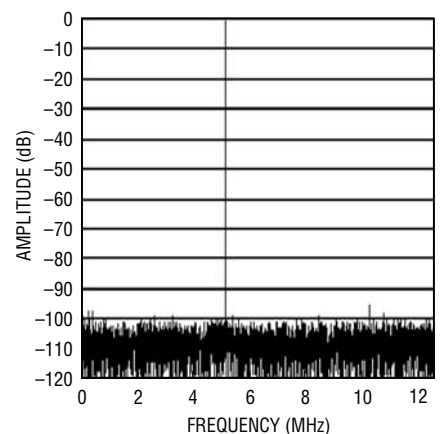
**LTC2291: Typical INL,**  
2V Range, 25Mpsps



**LTC2291: Typical DNL,**  
2V Range, 25Mpsps

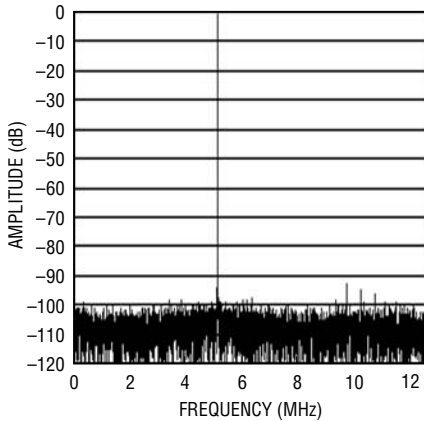


**LTC2291: 8192 Point FFT,**  
 $f_{IN} = 5\text{MHz}$ , -1dB, 2V Range,  
25Mpsps

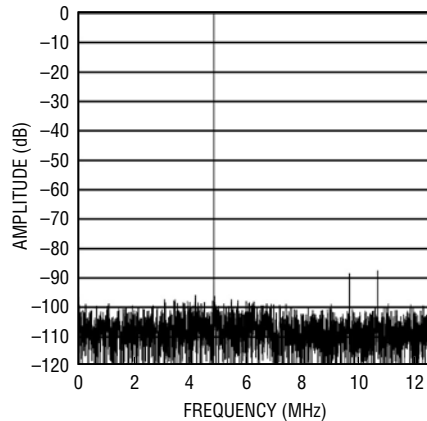


## TYPICAL PERFORMANCE CHARACTERISTICS

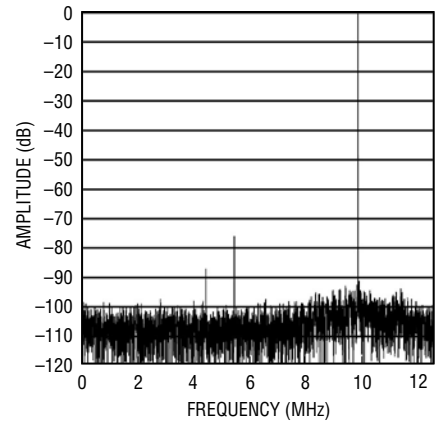
**LTC2291: 8192 Point FFT,  
 $f_{IN} = 30\text{MHz}$ ,  $-1\text{dB}$ ,  $2\text{V}$  Range,  
 $25\text{Mpsps}$**



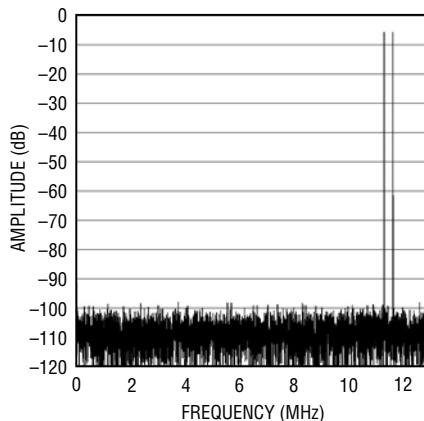
**LTC2291: 8192 Point FFT,  
 $f_{IN} = 70\text{MHz}$ ,  $-1\text{dB}$ ,  $2\text{V}$  Range,  
 $25\text{Mpsps}$**



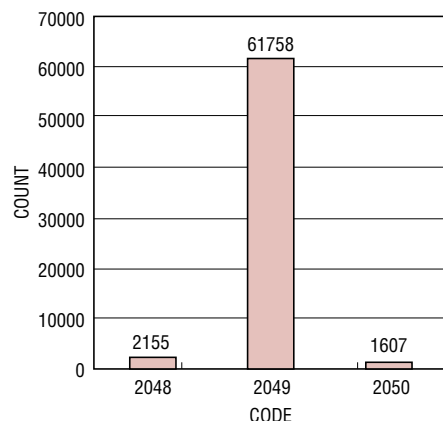
**LTC2291: 8192 Point FFT,  
 $f_{IN} = 140\text{MHz}$ ,  $-1\text{dB}$ ,  $2\text{V}$  Range,  
 $25\text{Mpsps}$**



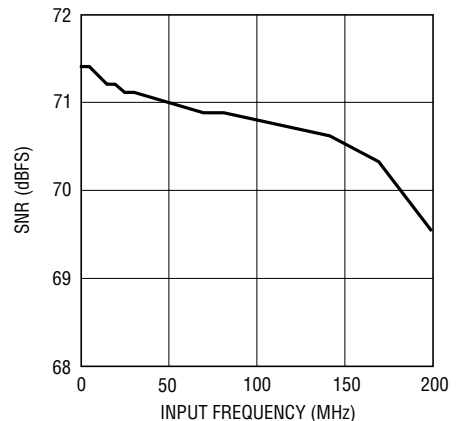
**LTC2291: 8192 Point 2-Tone FFT,  
 $f_{IN} = 10.9\text{MHz}$  and  $13.8\text{MHz}$ ,  
 $-1\text{dB}$ ,  $2\text{V}$  Range,  $25\text{Mpsps}$**



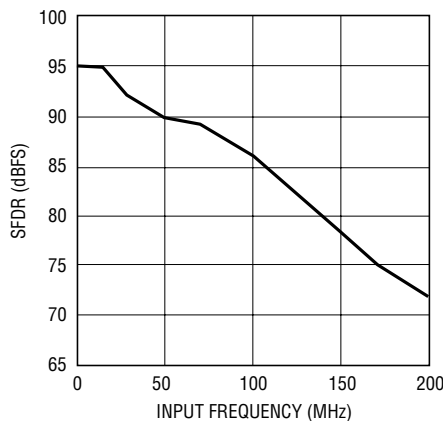
**LTC2291: Grounded Input  
Histogram,  $25\text{Mpsps}$**



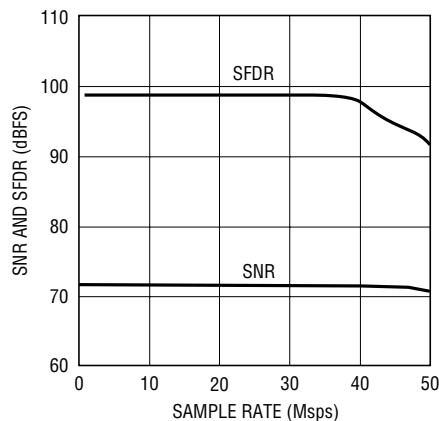
**LTC2291: SNR vs Input Frequency,  
 $-1\text{dB}$ ,  $2\text{V}$  Range,  $25\text{Mpsps}$**



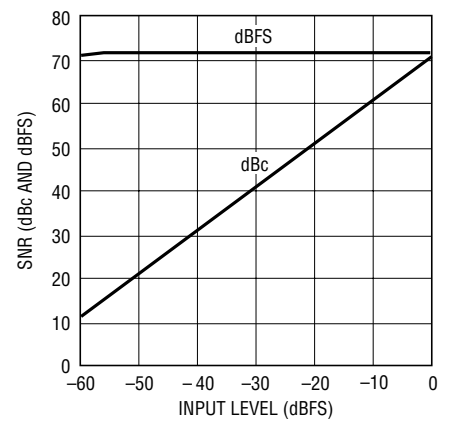
**LTC2291: SFDR vs Input  
Frequency,  $-1\text{dB}$ ,  $2\text{V}$  Range,  
 $25\text{Mpsps}$**



**LTC2291: SNR and SFDR vs  
Sample Rate,  $2\text{V}$  Range,  
 $f_{IN} = 5\text{MHz}$ ,  $-1\text{dB}$**

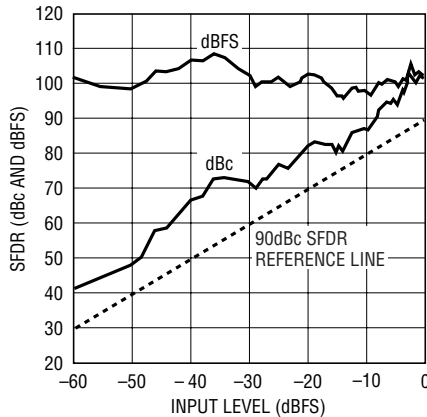


**LTC2291: SNR vs Input Level,  
 $f_{IN} = 5\text{MHz}$ ,  $2\text{V}$  Range,  $25\text{Mpsps}$**

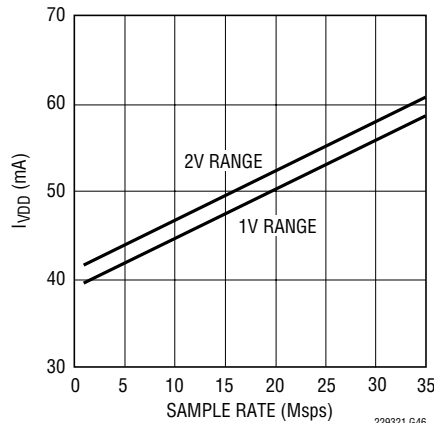


## TYPICAL PERFORMANCE CHARACTERISTICS

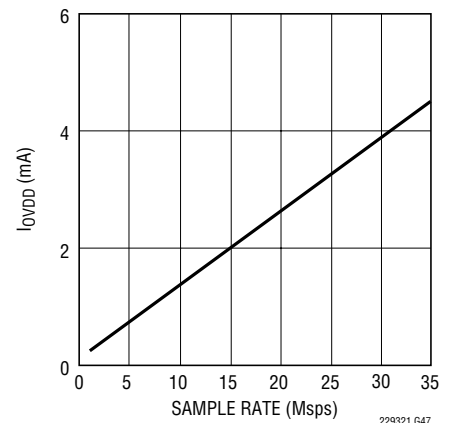
LTC2291: SFDR vs Input Level,  
 $f_{IN} = 5\text{MHz}$ , 2V Range, 25Mps



LTC2291:  $I_{VDD}$  vs Sample Rate,  
5MHz Sine Wave Input, -1dB



LTC2291:  $I_{VDD}$  vs Sample Rate,  
5MHz Sine Wave Input, -1dB,  
 $V_{VDD} = 1.8\text{V}$



## PIN FUNCTIONS

**$A_{INA}^+$  (Pin 1):** Channel A Positive Differential Analog Input.

**$A_{INA}^-$  (Pin 2):** Channel A Negative Differential Analog Input.

**REFHA (Pins 3, 4):** Channel A High Reference. Short together and bypass to Pins 5, 6 with a  $0.1\mu\text{F}$  ceramic chip capacitor as close to the pin as possible. Also bypass to Pins 5, 6 with an additional  $2.2\mu\text{F}$  ceramic chip capacitor and to ground with a  $1\mu\text{F}$  ceramic chip capacitor.

**REFLA (Pins 5, 6):** Channel A Low Reference. Short together and bypass to Pins 3, 4 with a  $0.1\mu\text{F}$  ceramic chip capacitor as close to the pin as possible. Also bypass to Pins 3, 4 with an additional  $2.2\mu\text{F}$  ceramic chip capacitor and to ground with a  $1\mu\text{F}$  ceramic chip capacitor.

**$V_{DD}$  (Pins 7, 10, 18, 63):** Analog 3V Supply. Bypass to GND with  $0.1\mu\text{F}$  ceramic chip capacitors.

**CLKA (Pin 8):** Channel A Clock Input. The input sample starts on the positive edge.

**CLKB (Pin 9):** Channel B Clock Input. The input sample starts on the positive edge.

**REFLB (Pins 11, 12):** Channel B Low Reference. Short together and bypass to Pins 13, 14 with a  $0.1\mu\text{F}$  ceramic

chip capacitor as close to the pin as possible. Also bypass to Pins 13, 14 with an additional  $2.2\mu\text{F}$  ceramic chip capacitor and to ground with a  $1\mu\text{F}$  ceramic chip capacitor.

**REFHB (Pins 13, 14):** Channel B High Reference. Short together and bypass to Pins 11, 12 with a  $0.1\mu\text{F}$  ceramic chip capacitor as close to the pin as possible. Also bypass to Pins 11, 12 with an additional  $2.2\mu\text{F}$  ceramic chip capacitor and to ground with a  $1\mu\text{F}$  ceramic chip capacitor.

**$A_{INB}^-$  (Pin 15):** Channel B Negative Differential Analog Input.

**$A_{INB}^+$  (Pin 16):** Channel B Positive Differential Analog Input.

**GND (Pins 17, 64):** ADC Power Ground.

**SENSEB (Pin 19):** Channel B Reference Programming Pin. Connecting SENSEB to  $V_{CMB}$  selects the internal reference and a  $\pm 0.5\text{V}$  input range.  $V_{DD}$  selects the internal reference and a  $\pm 1\text{V}$  input range. An external reference greater than  $0.5\text{V}$  and less than  $1\text{V}$  applied to SENSEB selects an input range of  $\pm V_{SENSEB}$ .  $\pm 1\text{V}$  is the largest valid input range.

**$V_{CMB}$  (Pin 20):** Channel B 1.5V Output and Input Common Mode Bias. Bypass to ground with  $2.2\mu\text{F}$  ceramic chip capacitor. Do not connect to  $V_{CMA}$ .

## PIN FUNCTIONS

**MUX (Pin 21):** Digital Output Multiplexer Control. If MUX is High, Channel A comes out on DA0-DA13, OFA; Channel B comes out on DB0-DB13, OFB. If MUX is Low, the output busses are swapped and Channel A comes out on DB0-DB13, OFB; Channel B comes out on DA0-DA13, OFA. To multiplex both channels onto a single output bus, connect MUX, CLKA and CLKB together.

**SHDNB (Pin 22):** Channel B Shutdown Mode Selection Pin. Connecting SHDNB to GND and  $\overline{OEB}$  to GND results in normal operation with the outputs enabled. Connecting SHDNB to GND and  $\overline{OEB}$  to  $V_{DD}$  results in normal operation with the outputs at high impedance. Connecting SHDNB to  $V_{DD}$  and  $\overline{OEB}$  to GND results in nap mode with the outputs at high impedance. Connecting SHDNB to  $V_{DD}$  and  $\overline{OEB}$  to  $V_{DD}$  results in sleep mode with the outputs at high impedance.

**$\overline{OEB}$  (Pin 23):** Channel B Output Enable Pin. Refer to SHDNB pin function.

**NC (Pins 24, 25, 41, 42):** Do Not Connect These Pins.

**DB0 – DB11 (Pins 26 to 30, 33 to 39):** Channel B Digital Outputs. DB11 is the MSB.

**OGND (Pins 31, 50):** Output Driver Ground.

**$OV_{DD}$  (Pins 32, 49):** Positive Supply for the Output Drivers. Bypass to ground with 0.1 $\mu$ F ceramic chip capacitor.

**OFB (Pin 40):** Channel B Overflow/Underflow Output. High when an overflow or underflow has occurred.

**DA0 – DA11 (Pins 43 to 48, 51 to 56):** Channel A Digital Outputs. DA11 is the MSB.

**OFA (Pin 57):** Channel A Overflow/Underflow Output. High when an overflow or underflow has occurred.

**OEA (Pin 58):** Channel A Output Enable Pin. Refer to SHDNA pin function.

**SHDNA (Pin 59):** Channel A Shutdown Mode Selection Pin. Connecting SHDNA to GND and  $\overline{OEA}$  to GND results in normal operation with the outputs enabled. Connecting SHDNA to GND and  $\overline{OEA}$  to  $V_{DD}$  results in normal operation with the outputs at high impedance. Connecting SHDNA to  $V_{DD}$  and  $\overline{OEA}$  to GND results in nap mode with the outputs at high impedance. Connecting SHDNA to  $V_{DD}$  and  $\overline{OEA}$  to  $V_{DD}$  results in sleep mode with the outputs at high impedance.

**MODE (Pin 60):** Output Format and Clock Duty Cycle Stabilizer Selection Pin. Note that MODE controls both channels. Connecting MODE to GND selects straight binary output format and turns the clock duty cycle stabilizer off.  $1/3 V_{DD}$  selects straight binary output format and turns the clock duty cycle stabilizer on.  $2/3 V_{DD}$  selects 2's complement output format and turns the clock duty cycle stabilizer on.  $V_{DD}$  selects 2's complement output format and turns the clock duty cycle stabilizer off.

**$V_{CMA}$  (Pin 61):** Channel A 1.5V Output and Input Common Mode Bias. Bypass to ground with 2.2 $\mu$ F ceramic chip capacitor. Do not connect to  $V_{CMB}$ .

**SENSEA (Pin 62):** Channel A Reference Programming Pin. Connecting SENSEA to  $V_{CMA}$  selects the internal reference and a  $\pm 0.5V$  input range.  $V_{DD}$  selects the internal reference and a  $\pm 1V$  input range. An external reference greater than 0.5V and less than 1V applied to SENSEA selects an input range of  $\pm V_{SENSEA}$ .  $\pm 1V$  is the largest valid input range.

**GND (Exposed Pad) (Pin 65):** ADC Power Ground. The Exposed Pad on the bottom of the package needs to be soldered to ground.

## FUNCTIONAL BLOCK DIAGRAM

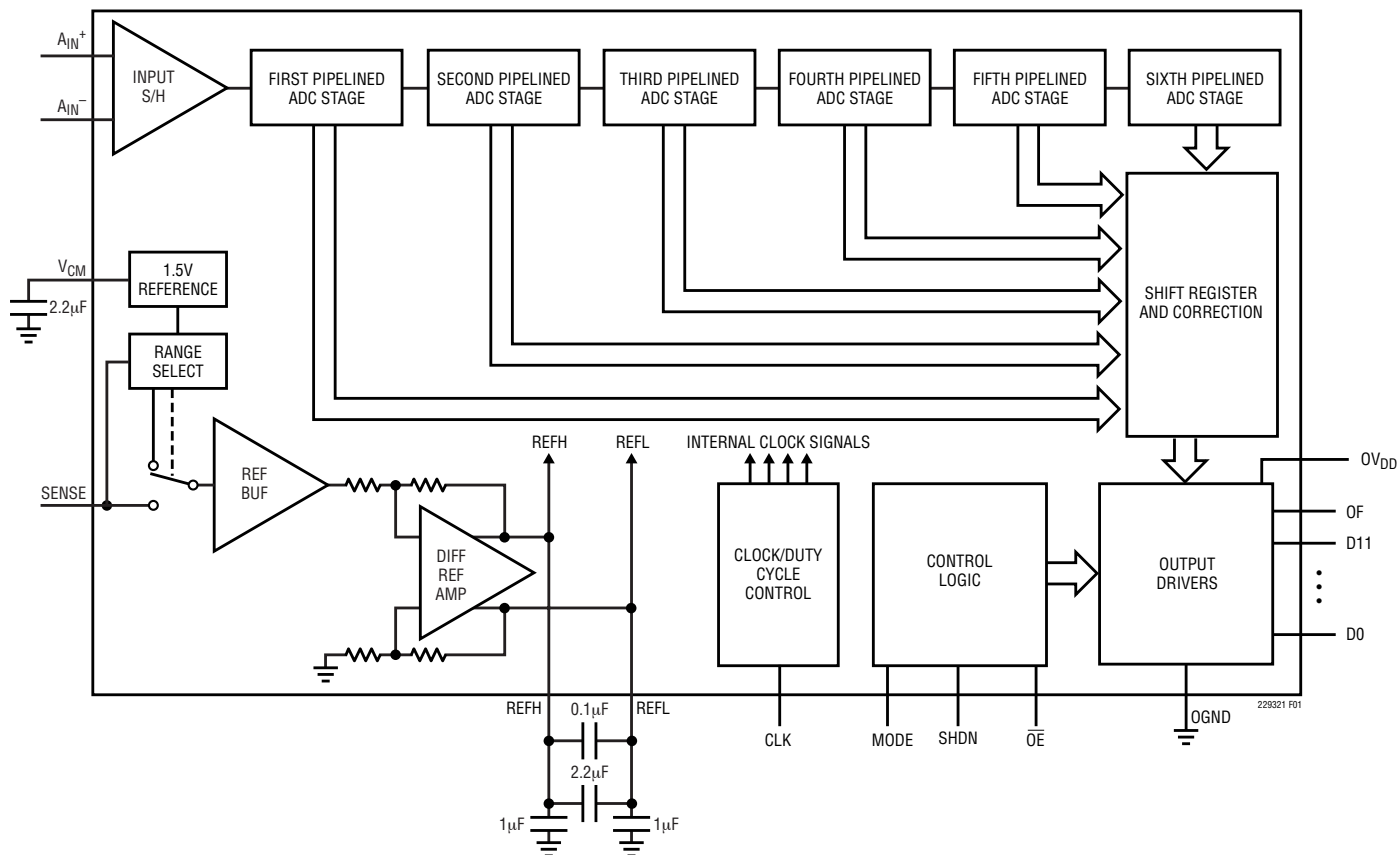
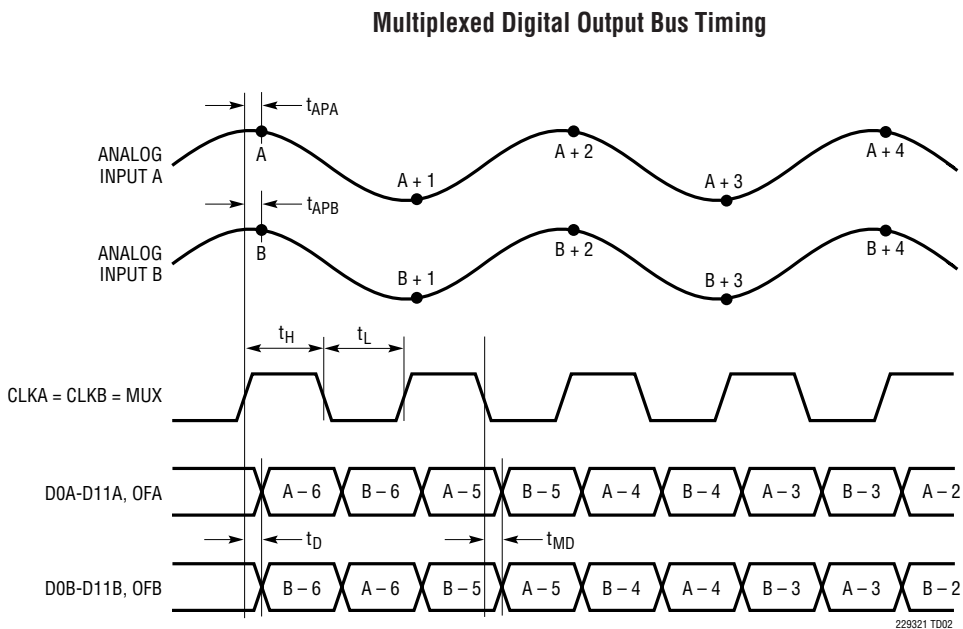
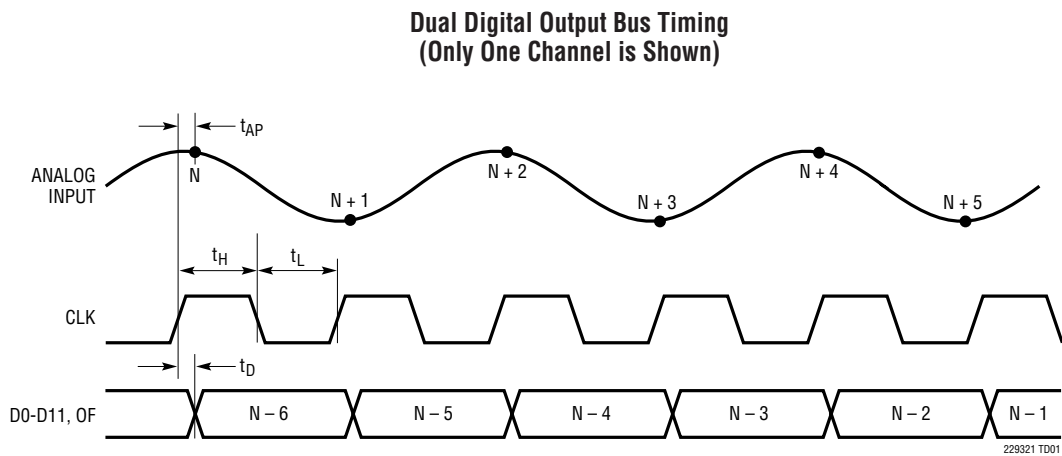


Figure 1. Functional Block Diagram (Only One Channel is Shown)

TIMING DIAGRAMS



## APPLICATIONS INFORMATION

### DYNAMIC PERFORMANCE

#### Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio  $[S/(N + D)]$  is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

#### Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

#### Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log \sqrt{(V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2)}/V_1$$

where  $V_1$  is the RMS amplitude of the fundamental frequency and  $V_2$  through  $V_n$  are the amplitudes of the second through  $n$ th harmonics. The THD calculated in this data sheet uses all the harmonics up to the fifth.

#### Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies  $f_a$  and  $f_b$  are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of  $m f_a \pm n f_b$ , where  $m$  and  $n = 0, 1, 2, 3$ , etc. The 3rd order intermodulation products are  $2f_a + f_b$ ,

$2f_b + f_a$ ,  $2f_a - f_b$  and  $2f_b - f_a$ . The intermodulation distortion is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order intermodulation product.

#### Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

#### Input Bandwidth

The input bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

#### Aperture Delay Time

The time from when CLK reaches midsupply to the instant that the input signal is held by the sample and hold circuit.

#### Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20\log (2\pi) \cdot f_{IN} \cdot t_{JITTER}$$

#### Crosstalk

Crosstalk is the coupling from one channel (being driven by a full-scale signal) onto the other channel (being driven by a  $-1$ dBFS signal).

### CONVERTER OPERATION

As shown in Figure 1, the LTC2293/LTC2292/LTC2291 are dual CMOS pipelined multistep converters. The converters have six pipelined ADC stages; a sampled analog input will result in a digitized value six cycles later (see the Timing Diagram section). For optimal AC performance the analog inputs should be driven differentially. For cost

## APPLICATIONS INFORMATION

sensitive applications, the analog inputs can be driven single-ended with slightly worse harmonic distortion. The CLK input is single-ended. The LTC2293/LTC2292/LTC2291 have two phases of operation, determined by the state of the CLK input pin.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When CLK is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the “Input S/H” shown in the block diagram. At the instant that CLK transitions from low to high, the sampled input is held. While CLK is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of CLK. When CLK goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When CLK goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the

third, fourth and fifth stages, resulting in a fifth stage residue that is sent to the sixth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

### SAMPLE/HOLD OPERATION AND INPUT DRIVE

#### Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2293/LTC2292/LTC2291 CMOS differential sample-and-hold. The analog inputs are connected to the sampling capacitors ( $C_{\text{SAMPLE}}$ ) through NMOS transistors. The capacitors shown attached to each input ( $C_{\text{PARASITIC}}$ ) are the summation of all other capacitance associated with each input.

During the sample phase when CLK is low, the transistors connect the analog inputs to the sampling capacitors and they charge to and track the differential input voltage. When CLK transitions from low to high, the sampled input voltage is held on the sampling capacitors. During the hold phase when CLK is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As CLK transitions from high to low, the inputs are reconnected to the sampling

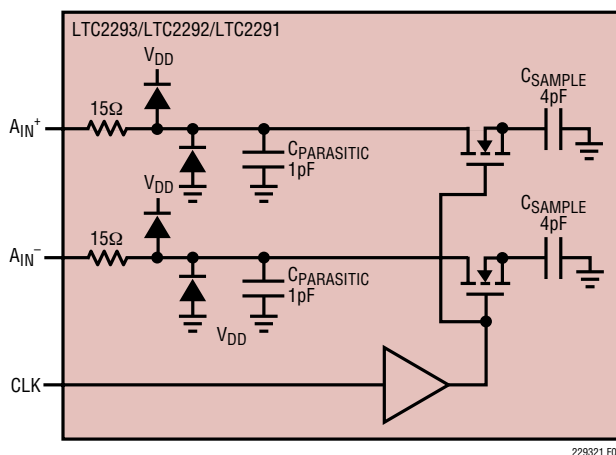


Figure 2. Equivalent Input Circuit

## APPLICATIONS INFORMATION

capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

### Single-Ended Input

For cost sensitive applications, the analog inputs can be driven single-ended. With a single-ended input the harmonic distortion and INL will degrade, but the SNR and DNL will remain unchanged. For a single-ended input,  $A_{IN}^+$  should be driven with the input signal and  $A_{IN}^-$  should be connected to 1.5V or  $V_{CM}$ .

### Common Mode Bias

For optimal performance the analog inputs should be driven differentially. Each input should swing  $\pm 0.5V$  for the 2V range or  $\pm 0.25V$  for the 1V range, around a common mode voltage of 1.5V. The  $V_{CM}$  output pin may be used to provide the common mode bias level.  $V_{CM}$  can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The  $V_{CM}$  pin must be bypassed to ground close to the ADC with a 2.2 $\mu F$  or greater capacitor.

### Input Drive Impedance

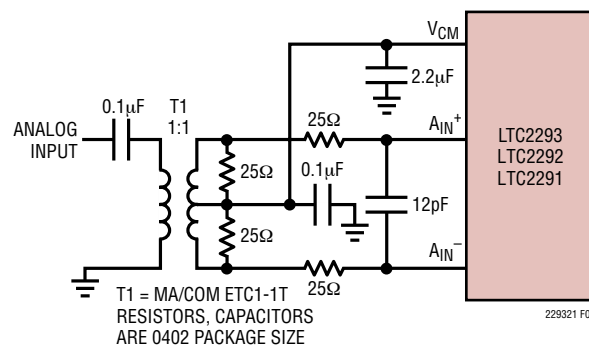
As with all high performance, high speed ADCs, the dynamic performance of the LTC2293/LTC2292/LTC2291 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and reactance can influence SFDR. At the falling edge of CLK, the sample-and-hold circuit will connect the 4pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when CLK rises, holding the sampled input on the sampling capacitor. Ideally the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period  $1/(2F_{ENCODE})$ ; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling

glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance, it is recommended to have a source impedance of 100 $\Omega$  or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

### Input Drive Circuits

Figure 3 shows the LTC2293/LTC2292/LTC2291 being driven by an RF transformer with a center tapped secondary. The secondary center tap is DC biased with  $V_{CM}$ , setting the ADC input signal at its optimum DC level. Terminating on the transformer secondary is desirable, as this provides a common mode path for charging glitches caused by the sample and hold. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used if the source impedance seen by the ADC does not exceed 100 $\Omega$  for each ADC input. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.



**Figure 3. Single-Ended to Differential Conversion Using a Transformer**

Figure 4 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of most op amps will limit the SFDR at high input frequencies.

## APPLICATIONS INFORMATION

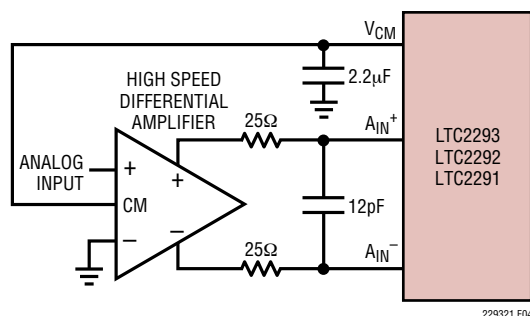


Figure 4. Differential Drive with an Amplifier

Figure 5 shows a single-ended input circuit. The impedance seen by the analog inputs should be matched. This circuit is not recommended if low distortion is required.

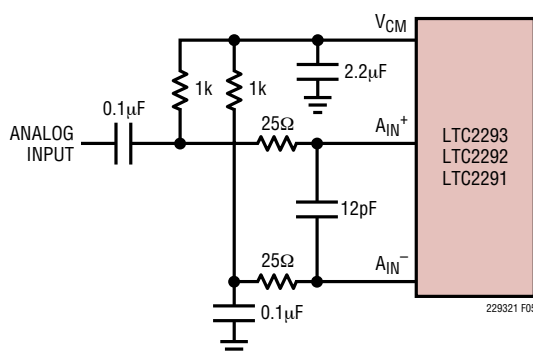


Figure 5. Single-Ended Drive

The 25Ω resistors and 12pF capacitor on the analog inputs serve two purposes: isolating the drive circuitry from the sample-and-hold charging glitches and limiting the wideband noise at the converter input.

For input frequencies above 70MHz, the input circuits of Figure 6, 7 and 8 are recommended. The balun transformer gives better high frequency response than a flux coupled center tapped transformer. The coupling capacitors allow the analog inputs to be DC biased at 1.5V. In Figure 8, the series inductors are impedance matching elements that maximize the ADC bandwidth.

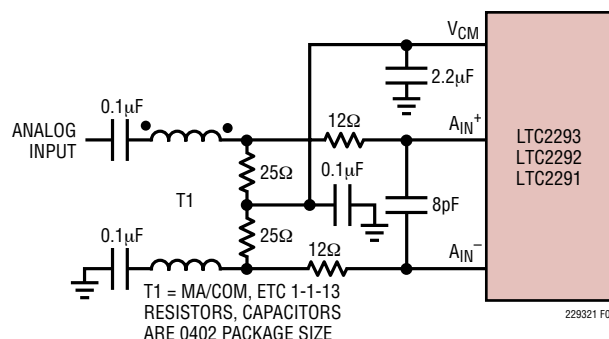


Figure 6. Recommended Front End Circuit for Input Frequencies Between 70MHz and 170MHz

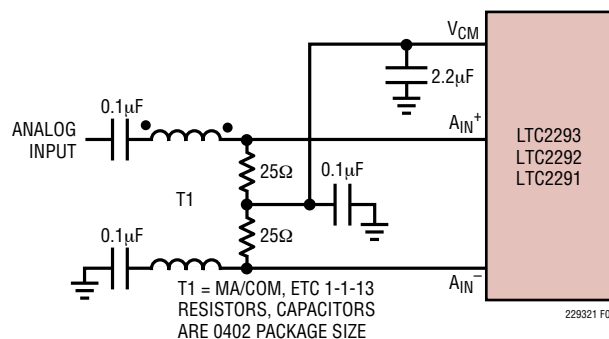


Figure 7. Recommended Front End Circuit for Input Frequencies Between 170MHz and 300MHz

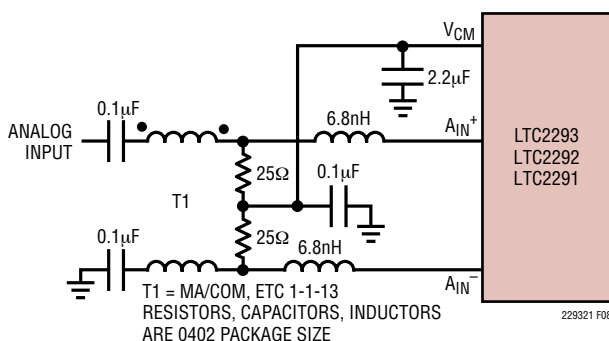


Figure 8. Recommended Front End Circuit for Input Frequencies Above 300MHz

Other voltage ranges between the pin selectable ranges can be programmed with two external resistors as shown in Figure 10. An external reference can be used by applying its output directly or through a resistor divider to SENSE. It is not recommended to drive the SENSE pin with a logic device. The SENSE pin should be tied to the appropriate level as close to the converter as possible. If the SENSE pin is driven externally, it should be bypassed to ground as close to the device as possible with a 1  $\mu$ F ceramic capacitor. For the best channel matching, connect an external reference to SENSEA and SENSEB.



The CLK inputs can be driven directly with a CMOS or TTL level signal. A sinusoidal clock can also be used along with a low jitter squaring circuit before the CLK pin (Figure 11).

## APPLICATIONS INFORMATION

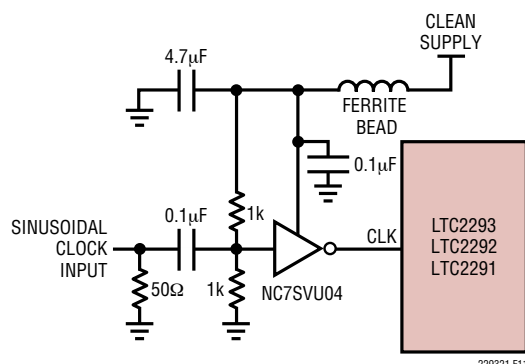


Figure 11. Sinusoidal Single-Ended CLK Drive

The noise performance of the LTC2293/LTC2292/LTC2291 can depend on the clock signal quality as much as on the analog input. Any noise present on the clock signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical, such as when digitizing high input frequencies, use as large an amplitude as possible. Also, if the ADC is clocked with a sinusoidal signal, filter the CLK signal to reduce wideband noise and distortion products generated by the source.

It is recommended that CLKA and CLKB are shorted together and driven by the same clock source. If a small time delay is desired between when the two channels sample the analog inputs, CLKA and CLKB can be driven by two different signals. If this delay exceeds 1ns, the performance of the part may degrade. CLKA and CLKB should not be driven by asynchronous signals.

### Maximum and Minimum Conversion Rates

The maximum conversion rate for the LTC2293/LTC2292/LTC2291 is 65Msps (LTC2293), 40Msps (LTC2292), and 25Msps (LTC2291). For the ADC to operate properly, the CLK signal should have a 50% ( $\pm 5\%$ ) duty cycle. Each half cycle must have at least 7.3ns (LTC2293), 11.8ns (LTC2292), and 18.9ns (LTC2291) for the ADC internal circuitry to have enough settling time for proper operation.

An optional clock duty cycle stabilizer circuit can be used if the input clock has a non 50% duty cycle. This circuit uses the rising edge of the CLK pin to sample the analog input. The falling edge of CLK is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 40% to 60% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require a hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin should be connected to  $1/3V_{DD}$  or  $2/3V_{DD}$  using external resistors. The MODE pin controls both Channel A and Channel B—the duty cycle stabilizer is either on or off for both channels.

The lower limit of the LTC2293/LTC2292/LTC2291 sample rate is determined by droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2293/LTC2292/LTC2291 is 1Msps.

## DIGITAL OUTPUTS

### Digital Output Buffers

Figure 12 shows an equivalent circuit for a single output buffer. Each buffer is powered by  $OV_{DD}$  and  $OGND$ , isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as  $50\Omega$  to external circuitry and may eliminate the need for external damping resistors.

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2293/LTC2292/LTC2291 should drive a minimal capacitive load to avoid possible interaction

## APPLICATIONS INFORMATION

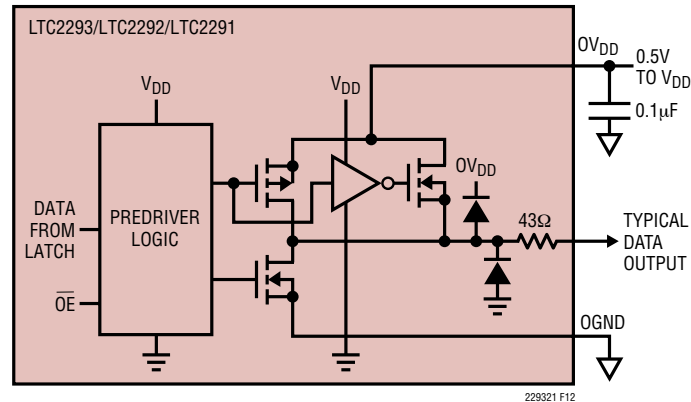


Figure 12. Digital Output Buffer

between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as an ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF.

Lower  $OV_{DD}$  voltages will also help reduce interference from the digital outputs.

### Data Format

Using the MODE pin, the LTC2293/LTC2292/LTC2291 parallel digital output can be selected for offset binary or 2's complement format. Note that MODE controls both Channel A and Channel B. Connecting MODE to GND or  $1/3V_{DD}$  selects straight binary output format. Connecting MODE to  $2/3V_{DD}$  or  $V_{DD}$  selects 2's complement output format. An external resistor divider can be used to set the  $1/3V_{DD}$  or  $2/3V_{DD}$  logic values. Table 1 shows the logic states for the MODE pin.

Table 1. MODE Pin Function

| MODE Pin    | Output Format   | Clock Duty Cycle Stabilizer |
|-------------|-----------------|-----------------------------|
| 0           | Straight Binary | Off                         |
| $1/3V_{DD}$ | Straight Binary | On                          |
| $2/3V_{DD}$ | 2's Complement  | On                          |
| $V_{DD}$    | 2's Complement  | Off                         |

### Overflow Bit

When OF outputs a logic high the converter is either overranged or underranged.

### Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers,  $OV_{DD}$ , should be tied to the same power supply as for the logic being driven. For example, if the converter is driving a DSP powered by a 1.8V supply, then  $OV_{DD}$  should be tied to that same 1.8V supply.

$OV_{DD}$  can be powered with any voltage from 500mV up to 3.6V.  $OGND$  can be powered with any voltage from GND up to 1V and must be less than  $OV_{DD}$ . The logic outputs will swing between  $OGND$  and  $OV_{DD}$ .

### Output Enable

The outputs may be disabled with the output enable pin,  $\overline{OE}$ .  $\overline{OE}$  high disables all data outputs including OF. The data access and bus relinquish times are too slow to allow the outputs to be enabled and disabled during full speed operation. The output Hi-Z state is intended for use during long periods of inactivity. Channels A and B have independent output enable pins ( $\overline{OEA}$ ,  $\overline{OEB}$ ).

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### Sleep and Nap Modes

The converter may be placed in shutdown or nap modes to conserve power. Connecting SHDN to GND results in normal operation. Connecting SHDN to  $V_{DD}$  and  $\overline{OE}$  to  $V_{DD}$  results in sleep mode, which powers down all circuitry including the reference and typically dissipates 1mW. When exiting sleep mode it will take milliseconds for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting SHDN to  $V_{DD}$  and  $\overline{OE}$  to GND results in nap mode, which typically dissipates 30mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap modes, all digital outputs are disabled and enter the Hi-Z state.

Channels A and B have independent SHDN pins ( $\overline{SHDNA}$ ,  $\overline{SHDNB}$ ). Channel A is controlled by  $\overline{SHDNA}$  and  $\overline{OEA}$ , and Channel B is controlled by  $\overline{SHDNB}$  and  $\overline{OEB}$ . The nap, sleep and output enable modes of the two channels are completely independent, so it is possible to have one channel operating while the other channel is in nap or sleep mode.

### Digital Output Multiplexer

The digital outputs of the LTC2293/LTC2292/LTC2291 can be multiplexed onto a single data bus. The MUX pin is a digital input that swaps the two data busses. If MUX is High, Channel A comes out on DA0-DA11, OFA; Channel B comes out on DB0-DB11, OFB. If MUX is Low, the output busses are swapped and Channel A comes out on DB0-DB11, OFB; Channel B comes out on DA0-DA11, OFA. To multiplex both channels onto a single output bus, connect MUX, CLKA and CLKB together (see the Timing Diagram for the multiplexed mode). The multiplexed data is available on either data bus—the unused data bus can be disabled with its  $\overline{OE}$  pin.

### Grounding and Bypassing

The LTC2293/LTC2292/LTC2291 requires a printed circuit board with a clean, unbroken ground plane. A multi-layer board with an internal ground plane is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the  $V_{DD}$ ,  $OV_{DD}$ ,  $V_{CM}$ , REFH, and REFL pins. Bypass capacitors must be located as close to the pins as possible. Of particular importance is the 0.1 $\mu$ F capacitor between REFH and REFL. This capacitor should be placed as close to the device as possible (1.5mm or less). A size 0402 ceramic capacitor is recommended. The large 2.2 $\mu$ F capacitor between REFH and REFL can be somewhat further away. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC2293/LTC2292/LTC2291 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

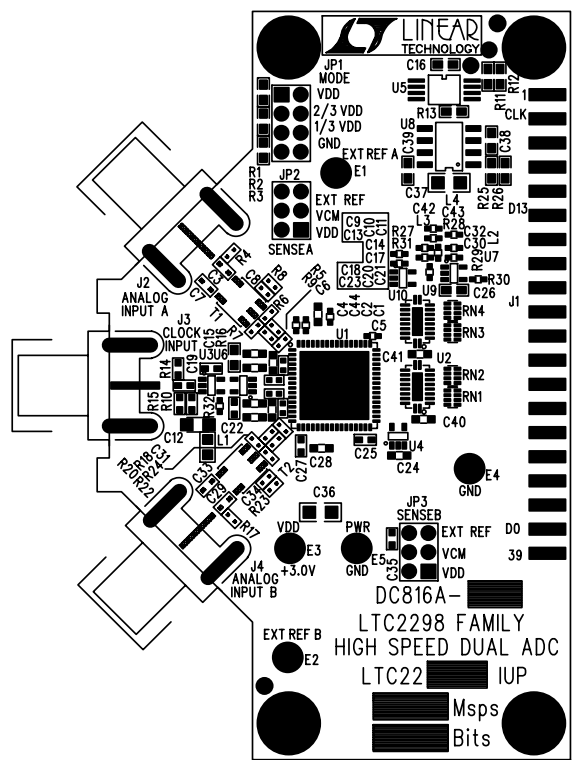
### Heat Transfer

Most of the heat generated by the LTC2293/LTC2292/LTC2291 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad should be soldered to a large grounded pad on the PC board. It is critical that all ground pins are connected to a ground plane of sufficient area.

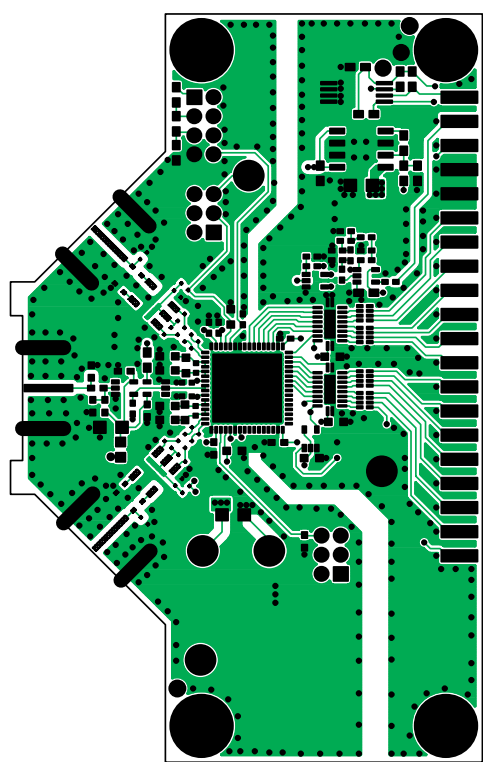


APPLICATIONS INFORMATION

Silkscreen Top

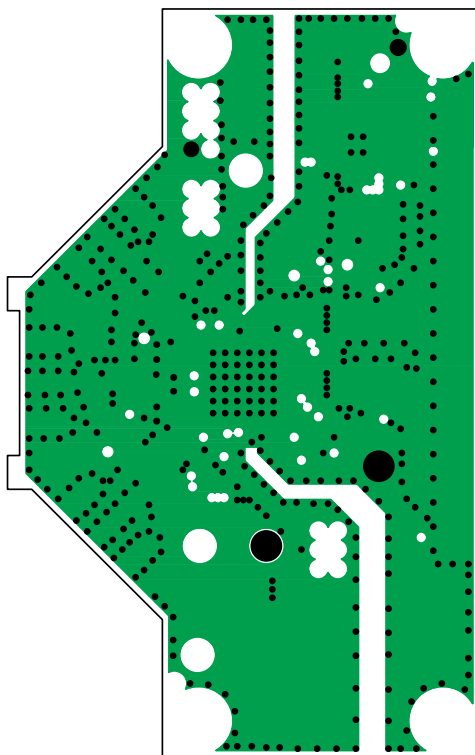


Top Side

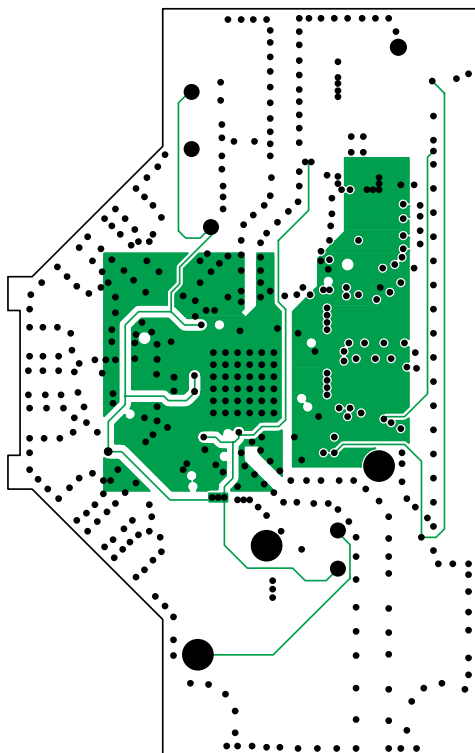


## APPLICATIONS INFORMATION

Inner Layer 2 GND

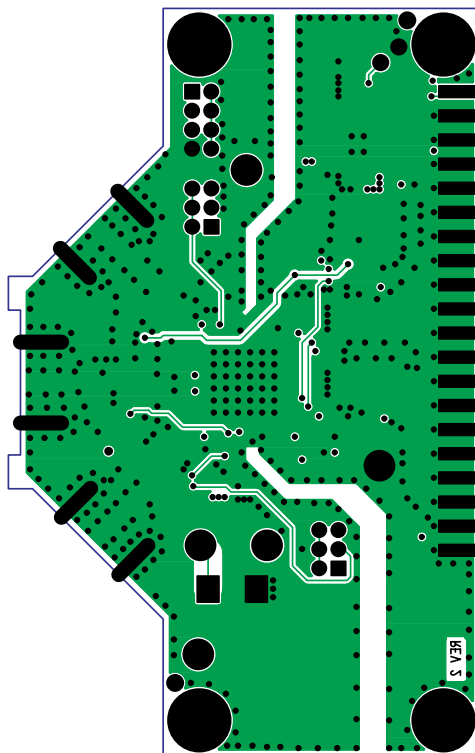


Inner Layer 3 Power



## APPLICATIONS INFORMATION

Bottom Side





## RELATED PARTS

| PART NUMBER      | DESCRIPTION                                                                | COMMENTS                                                                                  |
|------------------|----------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| LTC1403A/LTC1403 | 14-Bit/12-Bit 2.8Msps Serial ADC                                           | 3V, 14mW, Differential Input, MSOP Package                                                |
| LTC1407A/LTC1407 | 14-Bit/12-Bit 3Msps, Simultaneous Sampling Serial ADC                      | 3V, 14mW, 2-Ch. Differential Input, MSOP Package                                          |
| LTC1749          | 12-Bit, 80Msps Wideband ADC                                                | Up to 500MHz IF Undersampling, 87dB SFDR                                                  |
| LTC1750          | 14-Bit, 80Msps Wideband ADC                                                | Up to 500MHz IF Undersampling, 90dB SFDR                                                  |
| LTC2225          | 12-Bit, 10Msps ADC                                                         | 60mW, 71dB SNR, 5mm × 5mm QFN                                                             |
| LTC2226          | 12-Bit, 25Msps ADC                                                         | 75mW, 71dB SNR, 5mm × 5mm QFN                                                             |
| LTC2227          | 12-Bit, 40Msps ADC                                                         | 125mW, 71dB SNR, 5mm × 5mm QFN                                                            |
| LTC2228          | 12-Bit, 65Msps ADC                                                         | 205mW, 71dB SNR, 5mm × 5mm QFN                                                            |
| LTC2229          | 12-Bit, 80Msps ADC                                                         | 211mW, 70.6dB SNR, 5mm × 5mm QFN                                                          |
| LTC2236          | 10-Bit, 25Msps ADC                                                         | 75mW, 61dB SNR, 5mm × 5mm QFN                                                             |
| LTC2237          | 10-Bit, 40Msps ADC                                                         | 125mW, 61dB SNR, 5mm × 5mm QFN                                                            |
| LTC2238          | 10-Bit, 65Msps ADC                                                         | 205mW, 61dB SNR, 5mm × 5mm QFN                                                            |
| LTC2239          | 10-Bit, 80Msps ADC                                                         | 211mW, 61dB SNR, 5mm × 5mm QFN                                                            |
| LTC2245          | 14-Bit, 10Msps ADC                                                         | 60mW, 74.4dB SNR, 5mm × 5mm QFN                                                           |
| LTC2246          | 14-Bit, 25Msps ADC                                                         | 75mW, 74dB SNR, 5mm × 5mm QFN                                                             |
| LTC2247          | 14-Bit, 40Msps ADC                                                         | 125mW, 74dB SNR, 5mm × 5mm QFN                                                            |
| LTC2248          | 14-Bit, 65Msps ADC                                                         | 205mW, 74dB SNR, 5mm × 5mm QFN                                                            |
| LTC2249          | 14-Bit, 80Msps ADC                                                         | 222mW, 73dB SNR, 5mm × 5mm QFN                                                            |
| LTC2286          | Dual 10-Bit, 25Msps ADC                                                    | 150mW, 61dB SNR, 9mm × 9mm QFN                                                            |
| LTC2287          | Dual 10-Bit, 40Msps ADC                                                    | 235mW, 61dB SNR, 9mm × 9mm QFN                                                            |
| LTC2288          | Dual 10-Bit, 65Msps ADC                                                    | 400mW, 61dB SNR, 9mm × 9mm QFN                                                            |
| LTC2289          | Dual 10-Bit, 80Msps ADC                                                    | 445mW, 61dB SNR, 9mm × 9mm QFN                                                            |
| LTC2290          | Dual 12-Bit, 10Msps ADC                                                    | 120mW, 71dB SNR, 9mm × 9mm QFN                                                            |
| LTC2294          | Dual 12-Bit, 80Msps ADC                                                    | 445mW, 70.6dB SNR, 9mm × 9mm QFN                                                          |
| LTC2295          | Dual 14-Bit, 10Msps ADC                                                    | 120mW, 74.4dB SNR, 9mm × 9mm QFN                                                          |
| LTC2296          | Dual 14-Bit, 25Msps ADC                                                    | 150mW, 74dB SNR, 9mm × 9mm QFN                                                            |
| LTC2297          | Dual 14-Bit, 40Msps ADC                                                    | 235mW, 74dB SNR, 9mm × 9mm QFN                                                            |
| LTC2298          | Dual 14-Bit, 65Msps ADC                                                    | 400mW, 74dB SNR, 9mm × 9mm QFN                                                            |
| LTC2299          | Dual 14-Bit, 80Msps ADC                                                    | 445mW, 73dB SNR, 9mm × 9mm QFN                                                            |
| LT5512           | DC-3GHz High Signal Level Downconverting Mixer                             | DC to 3GHz, 21dBm IIP3, Integrated LO Buffer                                              |
| LT5514           | Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain | 450MHz 1dB BW, 47dB OIP3, Digital Gain Control 10.5dB to 33dB in 1.5dB/Step               |
| LT5515           | 1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator                  | 20dBm IIP3, Integrated LO Quadrature Generator                                            |
| LT5516           | 0.8GHz to 1.5GHz Direct Conversion Quadrature Demodulator                  | 21.5dBm IIP3, Integrated LO Quadrature Generator                                          |
| LT5517           | 40MHz to 900MHz Direct Conversion Quadrature Demodulator                   | 21dBm IIP3, Integrated LO Quadrature Generator                                            |
| LT5522           | 600MHz to 2.7GHz High Linearity Downconverting Mixer                       | 4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single Ended RF and LO Ports |