Document Title

128K x16 bit 2.5V Low Low Power Full CMOS Slow SRAM

Revision History

Revision No	History	Draft Date	Remark
00	Initial	Apr. 6. 2003	Final

DESCRIPTION

The HY62LF16206B is a high speed, super low power and 2Mbit full CMOS SRAM organized as 128K words by 16bits. The HY62LF16206B uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

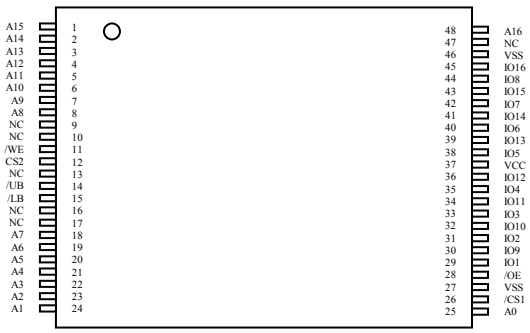
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(L-part)
  -. 1.2V(min) data retention
- Standard pin configuration
  -. 48-TSOP1

Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)	Temperature (°C)
				D	
HY62LF16206B	2.3~2.7	120	1	20	0~70

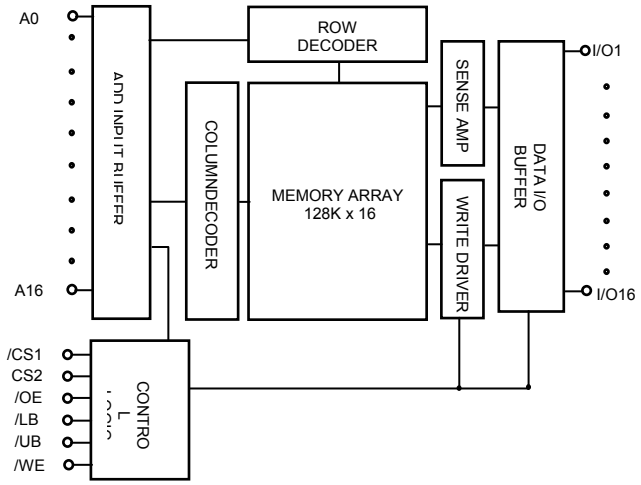
Notes :
1. Current value is max.

PIN CONNECTION



48-TSOP1(Forward)

BLOCK DIAGRAM



PIN CONNECTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS1	Chip Select 1	I/O1~I/O16	Data Inputs / Outputs
CS2	Chip Select 2	A0~A16	Address Inputs
/WE	Write Enable	Vcc	Power(2.3V~2.7V)
/OE	Output Enable	Vss	Ground
/LB	Lower Byte Control(I/O1~I/O8)	NC	No Connection
/UB	Upper Byte Control(I/O9~I/O16)		

ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62LF16206B-DT12C	120	D-part	0℃ ~ 70℃	48-TSOP1

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit	Remark
V_{IN}, V_{OUT}	Input/Output Voltage	-0.3 to 3.3	V	
Vcc	Power Supply	-0.3 to 3.3	V	
T_A	Operating Temperature	0 to 70	°C	
T_{STG}	Storage Temperature	-40 to 125	°C	
P_D	Power Dissipation	1.0	W	
T_{SOLDER}	Ball Soldering Temperature & Time	260 • 10	°C•sec	

Note :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS1	CS2	/WE	/OE	/LB	/UB	Mode	I/O		Power
							I/O1~I/O8	I/O9~I/O16	
H	X	X	X	X	X	Deselected	High-Z	High-Z	Standby
X	L	X	X	X	X		High-Z	High-Z	
X	X	X	X	H	H		High-Z	High-Z	
L	H	H	H	L	X	Output Disabled	High-Z	High-Z	Active
L	H	H	H	X	L		High-Z	High-Z	
L	H	H	L	L	H	Read	D_{OUT}	High-Z	
				H	L		High-Z	D_{OUT}	
				L	L		D_{OUT}	D_{OUT}	
L	H	L	X	L	H	Write	D_{IN}	High-Z	
				H	L		High-Z	D_{IN}	
				L	L		D_{IN}	D_{IN}	

Note:

1. H=V_{IH}, L=V_{IL}, X=don't care(Vil or Vih)
2. UB, LB(Upper, Lower Byte enable)
   These active LOW inputs allow individual bytes to be written or read.
   When LB is LOW, data is written or read to the lower byte, I/O 1 -I/O 8.
   When UB is LOW, data is written or read to the upper byte, I/O 9 -I/O 16.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	2.3	2.5	2.7	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.4	V

Note :
1. VIL = -1.5V for pulse width less than 30ns

DC ELECTRICAL CHARACTERISTICS

Vcc = 2.3V~2.7V, T_A = 0°C to 70°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	Vss ≤ V_{IN} ≤ Vcc	-1	-	1	uA
I_{LO}	Output Leakage Current	Vss ≤ V_{OUT} ≤ Vcc, /CS1 = V_{IH} or CS2= V_{IL}, /OE = V_{IH} or /WE = V_{IL}, or /UB = /LB = V_{IH}	-1	-	1	uA
Icc	Operating Power Supply Current	/CS1 = V_{IL}, CS2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA	-	-	1	mA
I_{CC1}	Average Operating Current	Cycle Time=Min.100% duty, /CS1 = 0.2V, CS2 = Vcc-0.2V, /WE = Vcc-0.2V, $I_{I/O}$ = 0mA Other Inputs = Vcc-0.2V/0.2V	-	-	5	mA
		Cycle time = 1us, /CS1 ≤ 0.2V, CS2 ≥ Vcc-0.2V, V_{IN}<0.2V or Vin ≥ Vcc-0.2V, $I_{I/O}$ = 0mA	-	-	2	mA
I_{SB}	Standby Current (TTL Input)	/CS1 = V_{IH}, CS2 = V_{IL} /UB = /LB = V_{IH}, V_{IN} = V_{IH} or V_{IL}	-	-	0.3	mA
I_{SB1}	Standby Current (CMOS Input)	/CS1 ≥ Vcc - 0.2V or CS2 ≤ Vss+0.2V or /UB = /LB ≥ Vcc - 0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	-	-	20	uA
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.5mA	1.8	-	-	V

Notes :
1. Typical values are at Vcc = 2.5V, T_A = 25°C
2. Typical values are sampled and not 100% tested

CAPACITANCE

(Temp = 25°C, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance(Add, /CS, /WE, /OE)	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance(I/O)	$V_{I/O}$ = 0V	10	pF

Note :
1. These parameters are sampled and not 100% tested

AC CHARACTERISTICS

Vcc = 2.3V~2.7V, T_A = 0°C to 70°C, unless otherwise specified

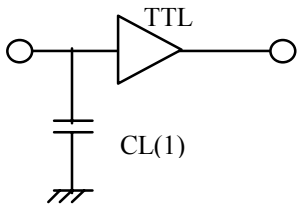
#	Symbol	Parameter	-12		Unit
			Min.	Max.	
READ CYCLE					
1	tRC	Read Cycle Time	120	-	ns
2	tAA	Address Access Time	-	120	ns
3	tACS	Chip Select Access Time	-	120	ns
4	tOE	Output Enable to Output Valid	-	80	ns
5	tBA	/LB, /UB Access Time	-	120	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	10	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	45	ns
10	tOHZ	Out Disable to Output in High Z	0	45	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	45	ns
12	tOH	Output Hold from Address Change	10	-	ns
WRITE CYCLE					
13	tWC	Write Cycle Time	120	-	ns
14	tCW	Chip Selection to End of Write	100	-	ns
15	tAW	Address Valid to End of Write	100	-	ns
16	tBW	/LB, /UB Valid to End of Write	100	-	ns
17	tAS	Address Set-up Time	0	-	ns
18	tWP	Write Pulse Width	85	-	ns
19	tWR	Write Recovery Time	0	-	ns
20	tWHZ	Write to Output in High Z	0	35	ns
21	tDW	Data to Write Time Overlap	60	-	ns
22	tDH	Data Hold from Write Time	0	-	ns
23	tOW	Output Active from End of Write	10	-	ns

AC TEST CONDITIONS

T_A = 0°C to 70°C, unless otherwise specified

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.1V
Output Load	tCLZ,tOLZ,tBLZ,tCHZ,tOHZ,tBHZ,tWHZ,tOW	CL = 5pF + 1TTL Load
	Others	CL = 30pF + 1TTL Load

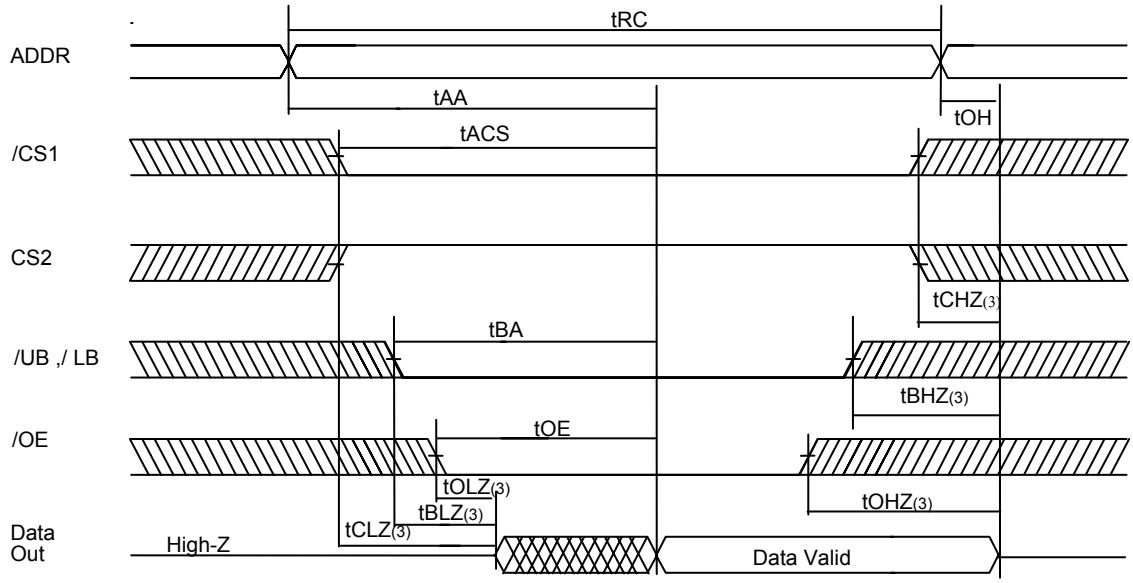
AC TEST LOADS



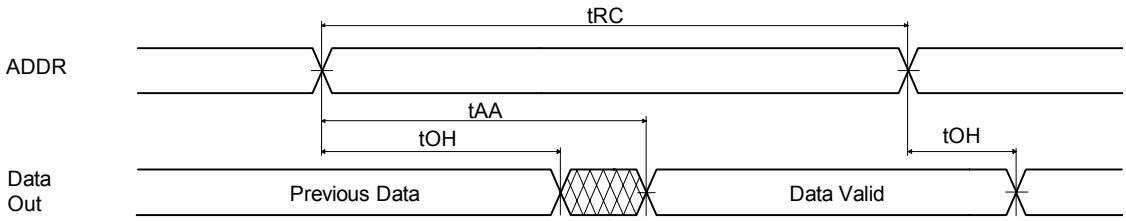
Note :
1. Including jig and scope capacitance

TIMING DIAGRAM

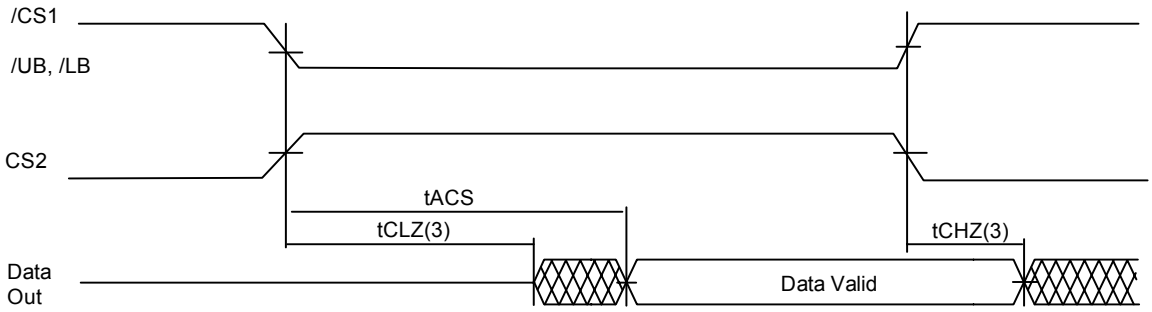
READ CYCLE 1(Note 1,4)



READ CYCLE 2(Note 2,3,4)

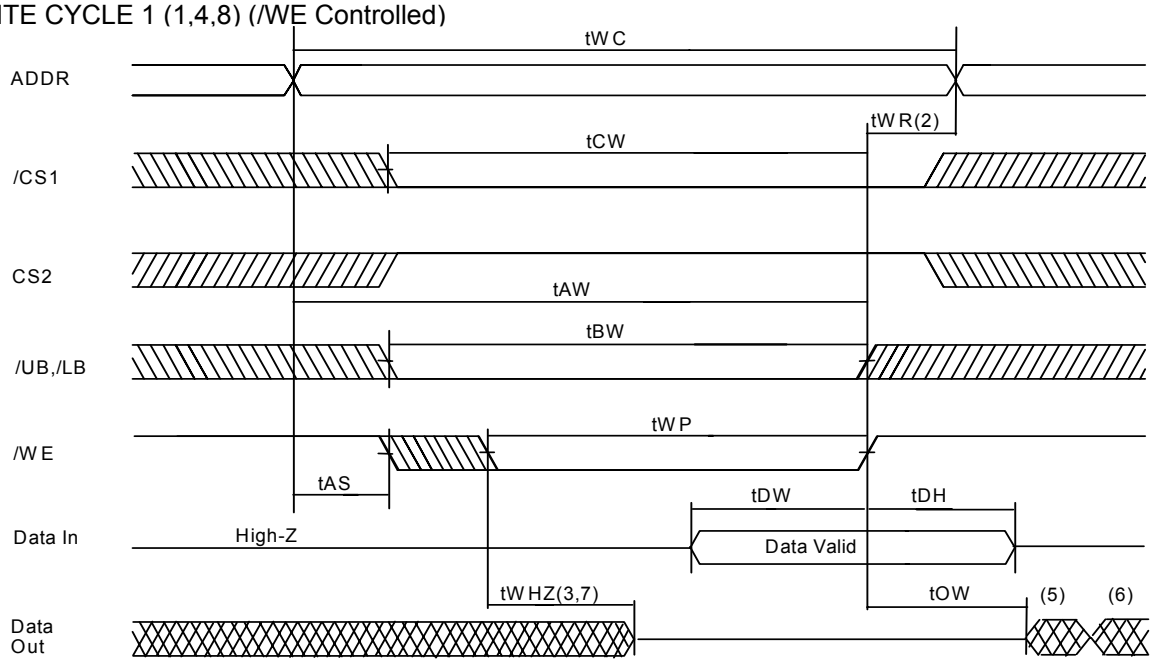


READ CYCLE 3(Note 1,2,4)

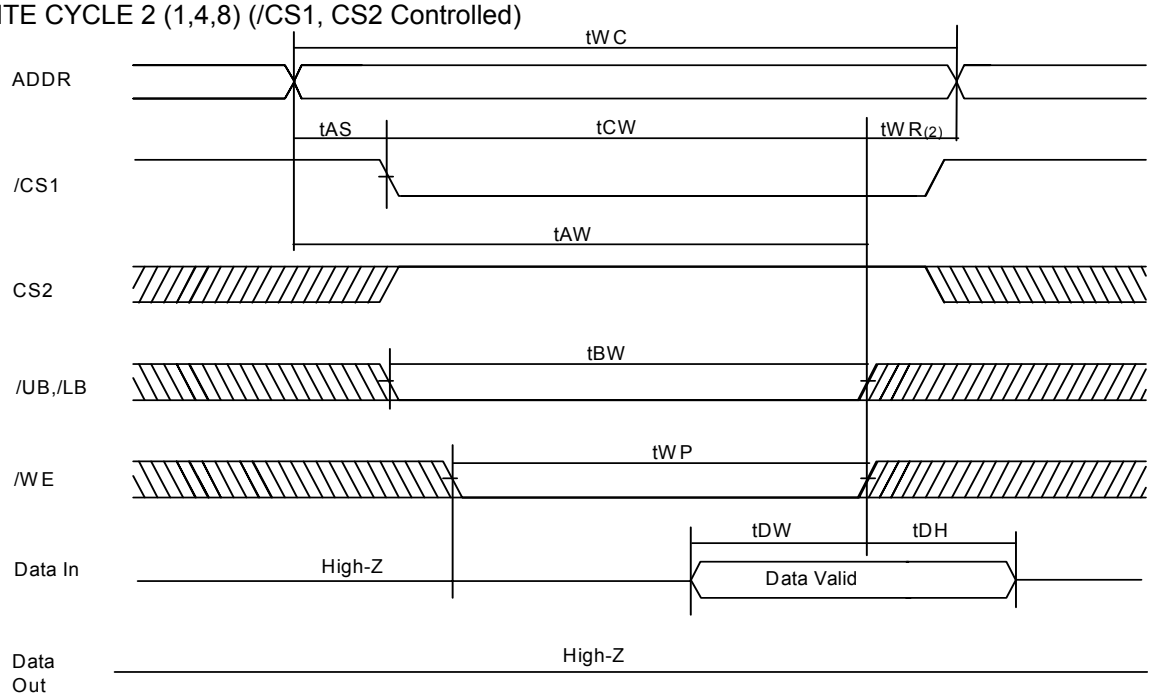


Notes:
1. A read occurs during the overlap of a low /OE, a high /WE, a low /CS1, a high CS2 and low /UB and/or /LB.
2. /OE = V_{IL}
3. Transition is measured ± 200mV from steady state voltage.
   This parameter is sampled and not 100% tested.
4. /CS1 in high for the standby, low for active. CS2 in low for the standby, high for active.
   /UB and /LB in high for the standby, low for active

WRITE CYCLE 1 (1,4,8) (/WE Controlled)



WRITE CYCLE 2 (1,4,8) (/CS1, CS2 Controlled)



Notes:

1. A write occurs during the overlap of a low /WE, a low /CS1, a high CS2 and low /UB and/or /LB.
2. tWR is measured from the earlier of /CS, /LB, /UB, or /WE going high or CS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS1, /LB and /UB low transition with CS2 high transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured ±200mV from steady state.
   This parameter is sampled and not 100% tested.
8. /CS1 in high for the standby, low for active. CS2 in low for the standby, high for active.
   /UB and /LB in high for the standby, low for active

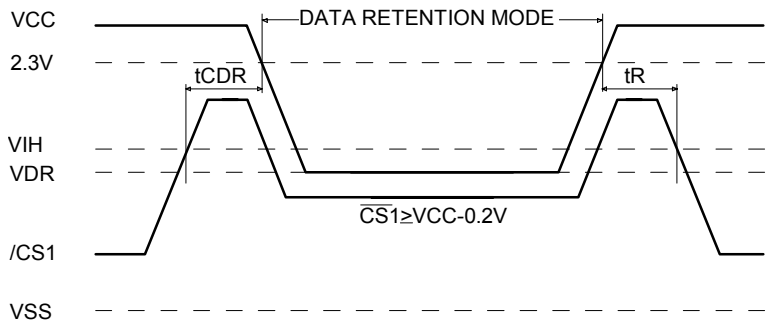
DATA RETENTION ELECTRIC CHARACTERISTIC

T_A = 0°C to 70°C

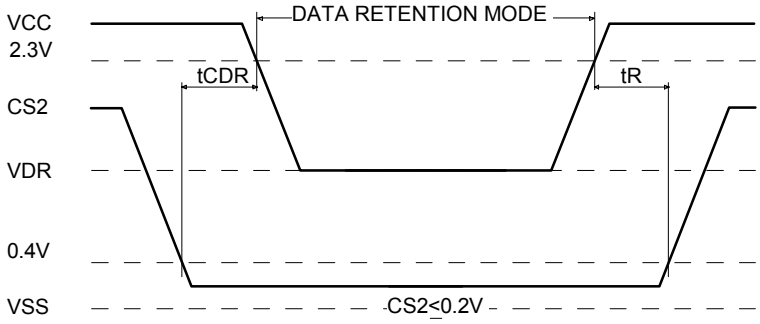
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	Vcc for Data Retention	/CS1 ≥ Vcc - 0.2V or CS2 ≤ Vss+0.2V or /UB = /LB ≥ Vcc-0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	1.2	-	2.7	V
I_{CCDR}	Data Retention Current	Vcc=1.5V, /CS1 ≥ Vcc - 0.2V, CS2 ≤ Vss+0.2V, /UB = /LB ≥ Vcc-0.2V or V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	-	-	20	uA
tCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
tR	Operating Recovery Time		tRC(3)	-	-	ns

Notes:
1. Typical values are under the condition of T_A = 25°C.
2. Typical Values are sampled and not 100% tested
3. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM 1

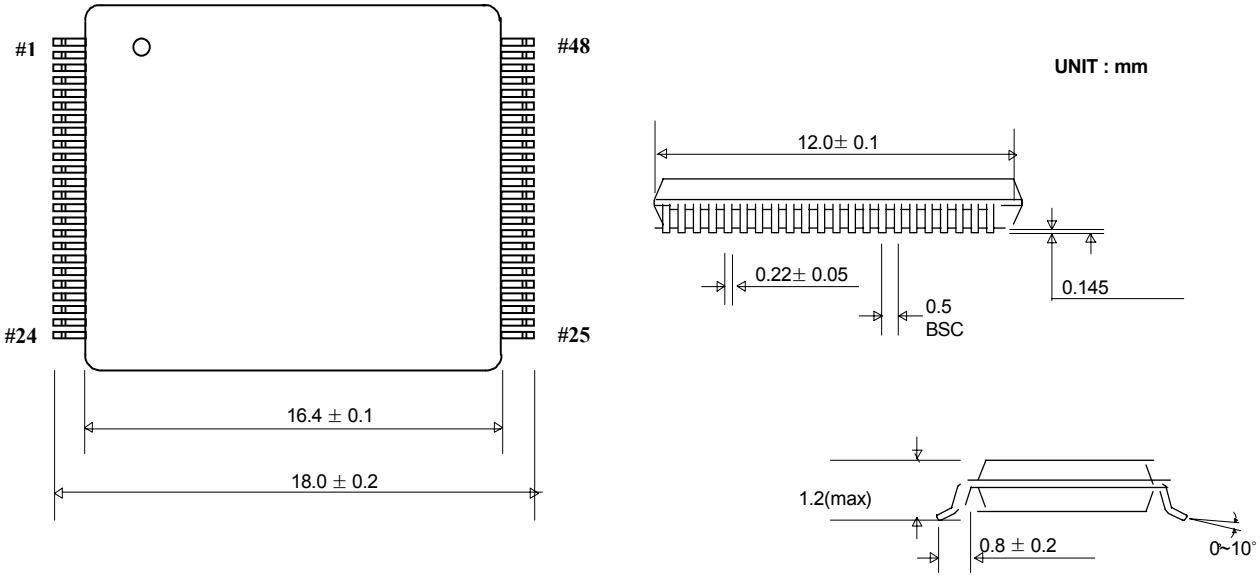


DATA RETENTION TIMING DIAGRAM 2



PACKAGE INFORMATION

48pin Thin Small Outline Package Forward



MARKING INSTRUCTION

- **Top Side**

Package	Marking Example
TSOP-I (Forward)	○ hynix KOREA HY62LF16206B yywwp DT12C

Index

• **hynix**	: Hynix Logo	
• **KOREA**	: Origin Country	
• **HY62LF16206B**	: Part Name	
HY	: HYNIX	
62	: Product Group	: Slow SRAM
L	: Operating Voltage	: 2.5V(2.3V ~ 2.7V)
F	: Tech. + Classification	: Full CMOS
16	: Organization	: x16
20	: Density	: 2M
6	: Mode	: 2CS with /UB,/LB;tCS
B	: Version	: 3rd Generation
• **yy**	: Year (ex : 03 = year 2003, 04 = year 2004)	
• **ww**	: Work Week (ex : 12 = ww12)	
• **p**	: Process Code	
	- A	: 12mm X 18mm
• **D**	: Power Consumption	: Low Low Power
• **T**	: Package Type	: TSOP-I
• **12**	: Speed	: 120ns
• **C**	: Temperature	: Commercial (0 ~ 70 °C)

Note

- Capital Letter : Fixed Item
- Small Letter : Non-fixed Item

- **Bottom Side**

Package	Marking Example
TSOP-I (Forward)	x x x x x x x x

Index	
• **xxxxxxxx**	: FAB Run No.
Note	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item