



STD95N2LH5 STU95N2LH5

N-channel 25 V - 0.0038 Ω - 80 A - DPAK - IPAK
STripFET™ V Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STD95N2LH5	25 V	<0.0045 Ω	80 A
STU95N2LH5	25 V	<0.0049 Ω	80 A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Application

Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFET™ technology. The lowest available R_{DS(on)} * Q_g, in the standard packages, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

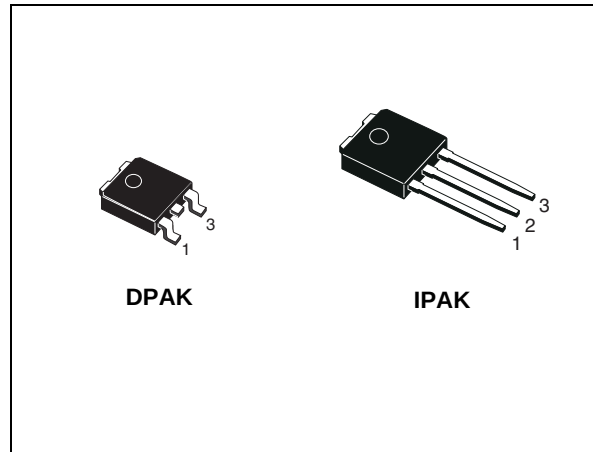


Figure 1. Internal schematic diagram

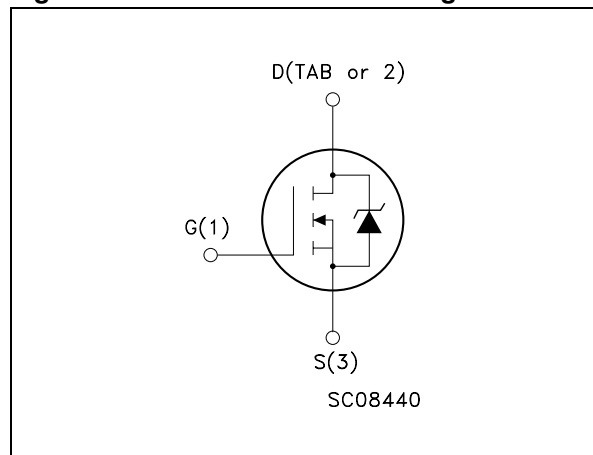


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD95N2LH5	95N2LH5	DPAK	Tape and reel
STU95N2LH5	95N2LH5	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	25	V
V_{GS}	Gate-Source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	67	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	70	W
	Derating factor	0.47	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	165	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting $T_j = 25^\circ\text{C}$, $I_d = 40\text{ A}$, $V_{dd} = 20\text{ V}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.14	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-case max	100	$^\circ\text{C/W}$
T_j	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	25			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 25\ \text{V}$ $V_{DS} = 25\ \text{V}$, $T_c = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$, $I_D = 40\ \text{A}$ SMD version		0.0038	0.0045	Ω
		$V_{GS} = 10\ \text{V}$, $I_D = 40\ \text{A}$		0.0044	0.0049	Ω
		$V_{GS} = 5\ \text{V}$, $I_D = 40\ \text{A}$ SMD version		0.005	0.006	Ω
		$V_{GS} = 5\ \text{V}$, $I_D = 40\ \text{A}$		0.006	0.007	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$		1817		pF
C_{oss}	Output capacitance			420		pF
C_{rss}	Reverse transfer capacitance			67		pF
Q_g	Total gate charge	$V_{DD} = 13\ \text{V}$, $I_D = 80\ \text{A}$		13.4		nC
Q_{gs}	Gate-source charge	$V_{GS} = 5\ \text{V}$		6.7		nC
Q_{gd}	Gate-drain charge	(see Figure 16)		4.1		nC
Q_{gs1}	Pre V_{th} gate-to-source charge	$V_{DD} = 13\ \text{V}$, $I_D = 80\ \text{A}$ (see Figure 19)		3.5		nC
Q_{gs2}	Post V_{th} gate-to-source charge			3.2		nC
R_G	Gate input resistance	$f = 1\ \text{MHz}$ gate bias Bias = 0 test signal level = 20 mV open drain		1.1		Ω

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=12.5\text{ V}$, $I_D=40\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 15)		7 38		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=12.5\text{ V}$, $I_D=40\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 15)		22 7		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				80 320	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=35\text{ A}$, $V_{GS}=0$			1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=80\text{ A}$, $V_{DD}=20\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$, (see Figure 17)		32.4 27.1 1.7		ns nC A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

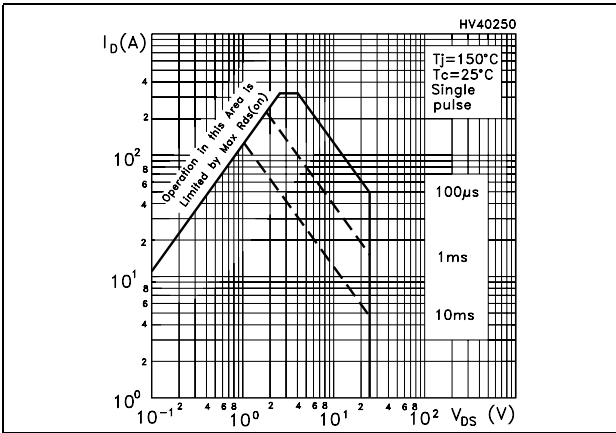


Figure 3. Thermal impedance

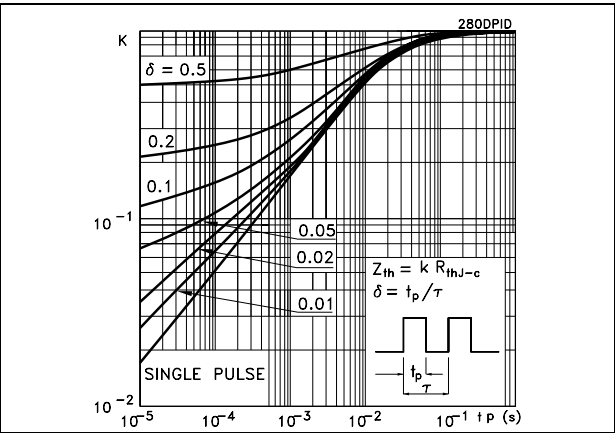


Figure 4. Output characteristics

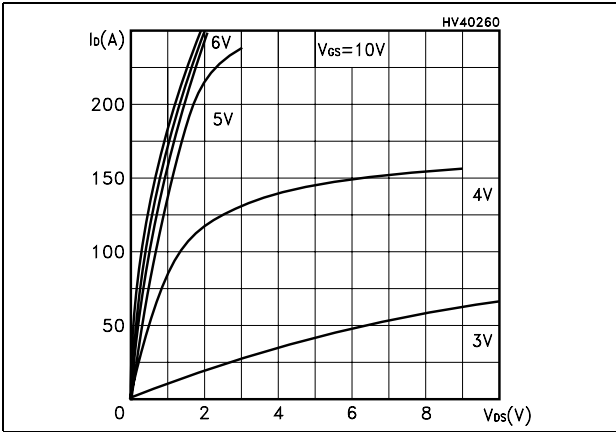


Figure 5. Transfer characteristics

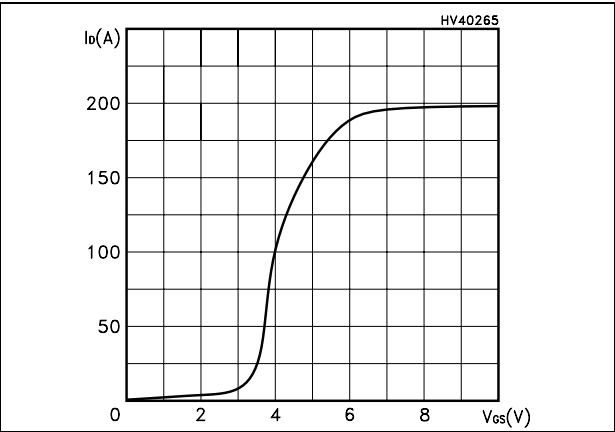


Figure 6. Normalized B_VDSS vs temperature

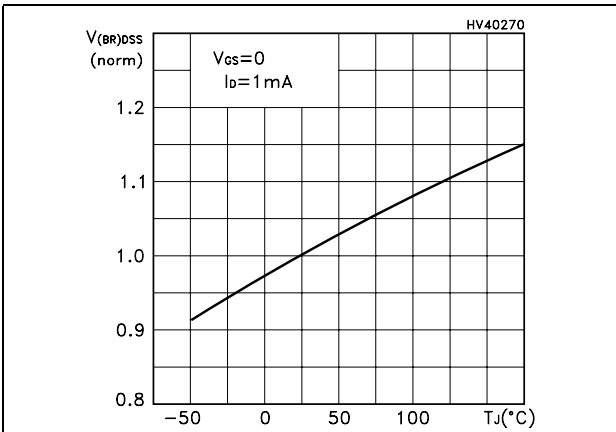


Figure 7. Static drain-source on resistance

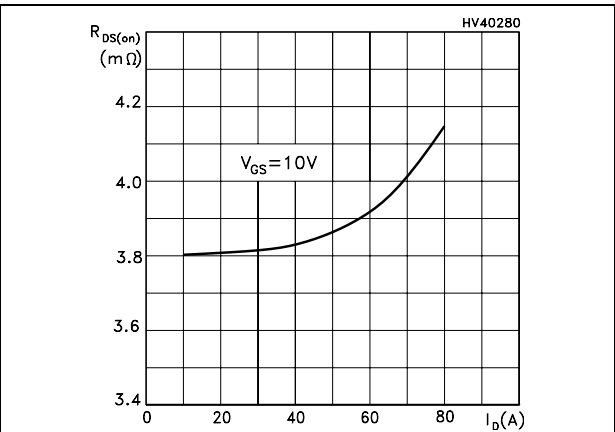


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

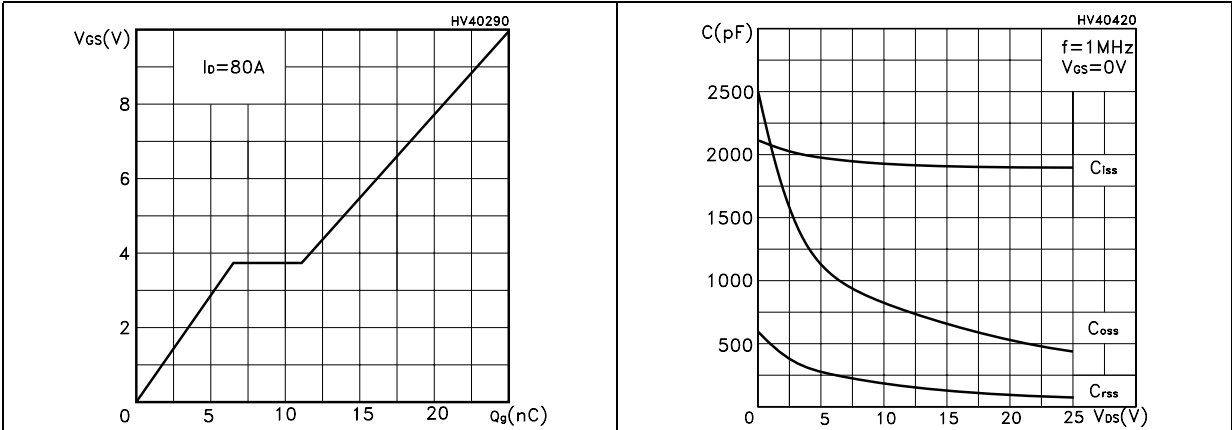


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

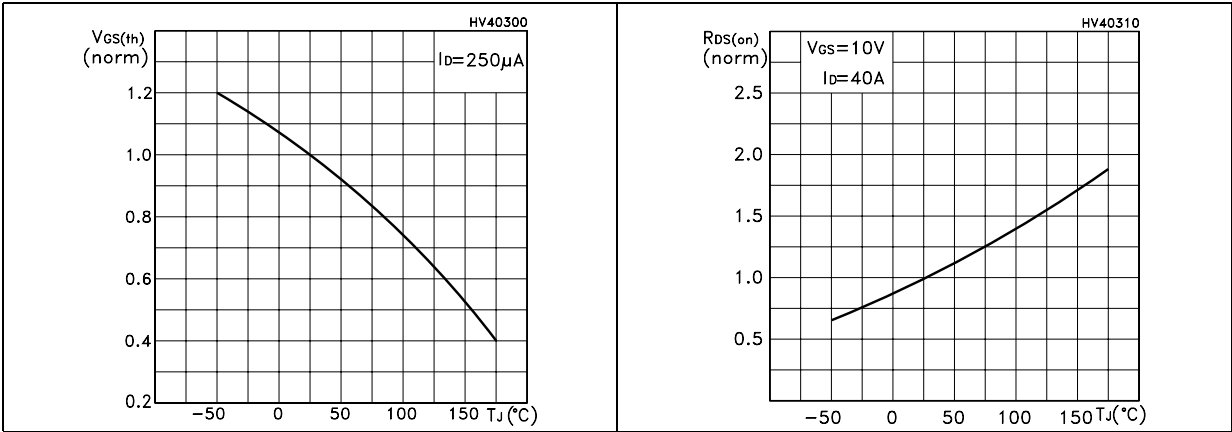
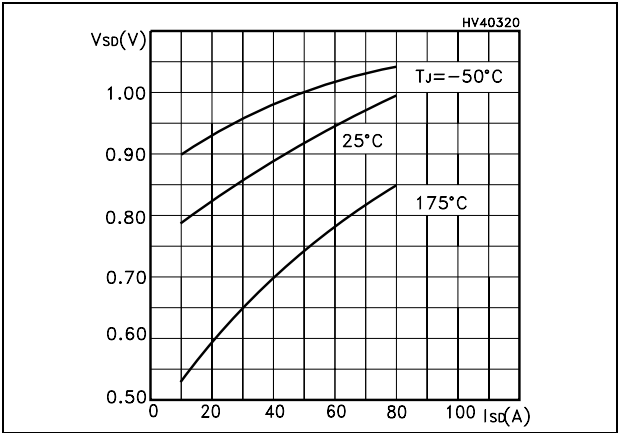


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Unclamped inductive load test circuit

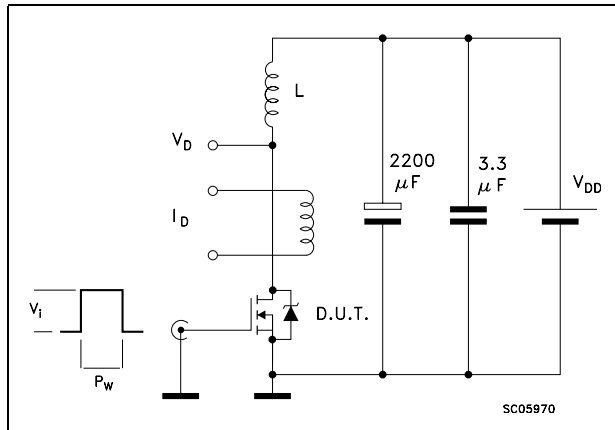


Figure 14. Unclamped inductive waveform

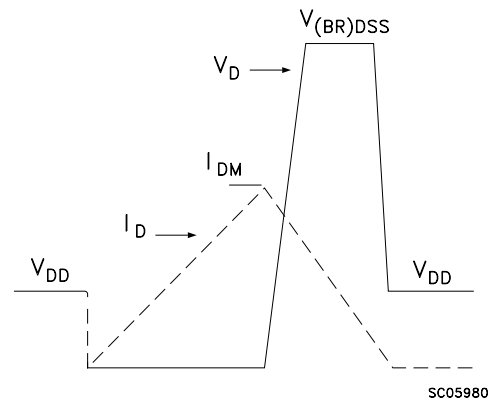


Figure 15. Switching times test circuit for resistive load

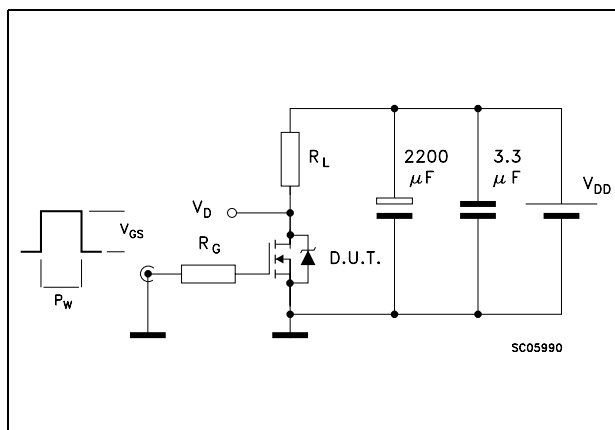


Figure 16. Gate charge test circuit

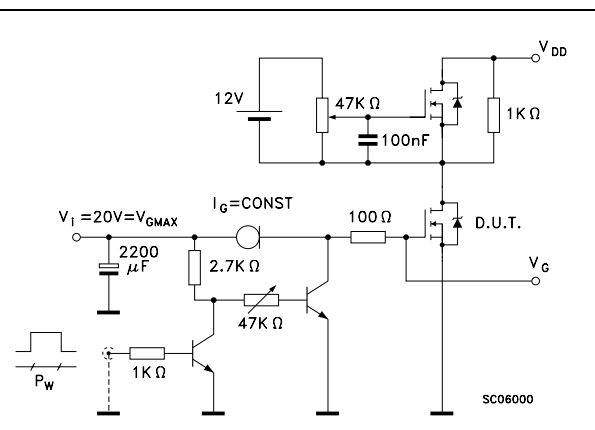


Figure 17. Test circuit for inductive load switching and diode recovery times

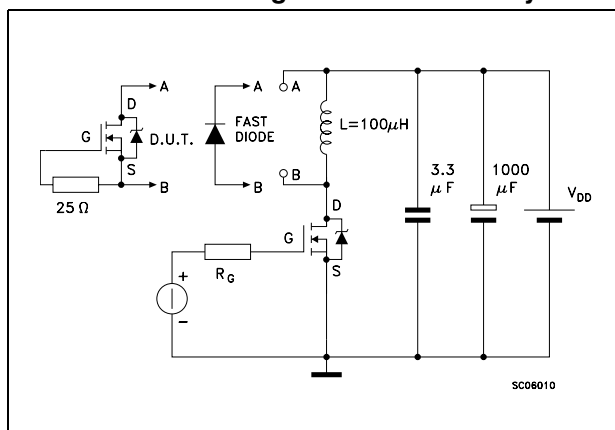


Figure 18. Switching time waveform

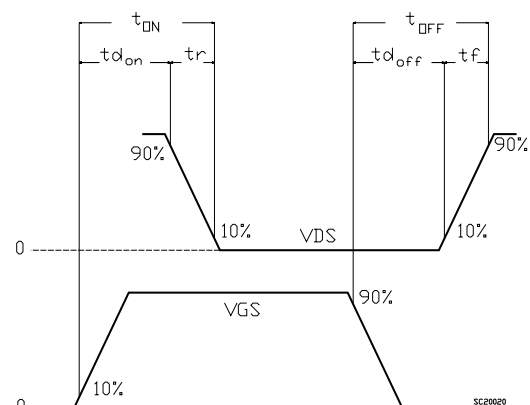
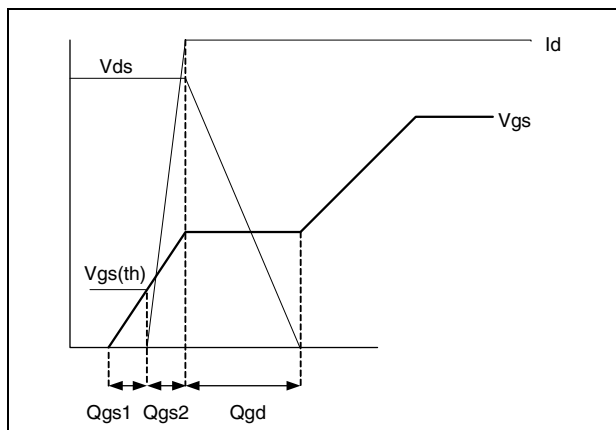


Figure 19. Gate charge waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

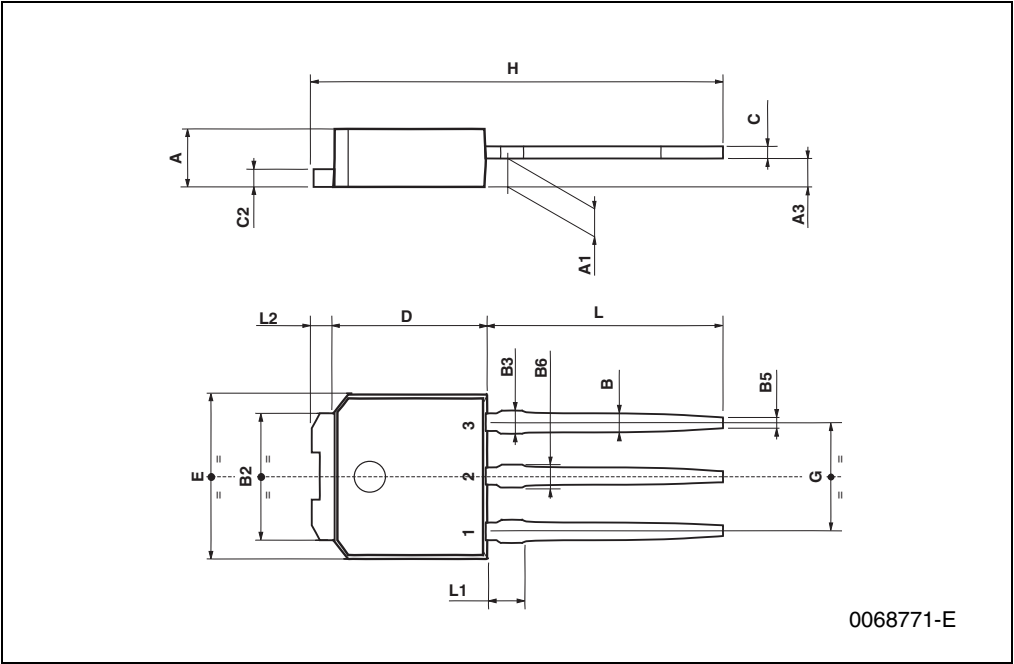
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The mechanical drawing illustrates the DPAK package geometry. The top view shows dimensions E (total width), b4 (lead width), and e (pitch). The side view shows dimensions A (height), A1 (lead height), A2 (lead thickness), B (lead thickness), C (lead thickness), C2 (lead thickness), D (total height), D1 (lead height), E1 (lead height), and H (total height). The detail view shows dimensions L2 (lead length), L4 (lead length), L (lead length), L1 (lead length), and V2 (lead angle). The thermal pad is shown with dimensions E1 and D1. The seating plane and gauge plane are indicated.

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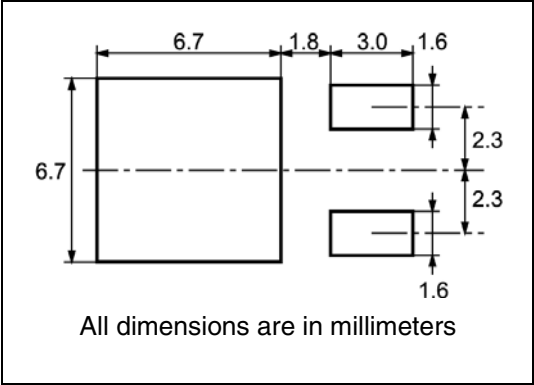
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

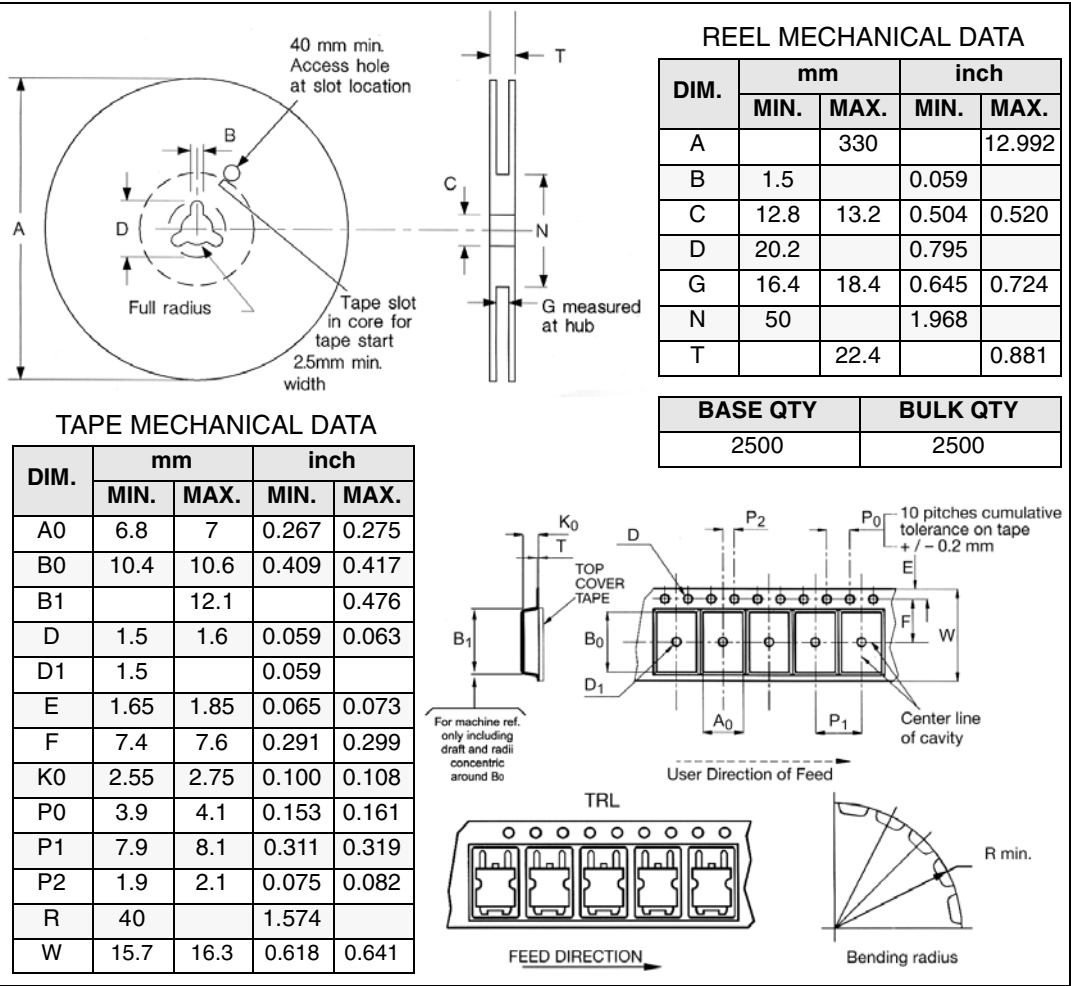


5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
16-Oct-2007	1	First release
20-Feb-2008	2	Modified Table 4.: Static

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