## KAD5512P

## Low Power 12-Bit, 250/210/170/125MSPS ADC

## General Description

The KAD5512P is the low-power member of the KAD5512 family of 12 -bit analog-to-digital converters. Designed with Kenet's proprietary FemtoCharge ${ }^{\circledR}$ technology on a standard CMOS process, the family supports sampling rates of up to 250MSPS. The KAD5512P is part of a pin-compatible portfolio of 10, 12 and 14-bit A/Ds with sample rates ranging from 125 MSPS to 500MSPS.
A serial peripheral interface (SPI) port allows for extensive configurability, as well as fine control of various parameters such as gain and offset.

Digital output data is presented in selectable LVDS or CMOS formats. The KAD5512P is available in 72and 48 -contact QFN packages with an exposed paddle. Operating from a 1.8 V supply, performance is specified over the full industrial temperature range ( -40 to $+85^{\circ} \mathrm{C}$ ).

## Features

- Pin-Compatible with the KAD5512HP family, operating at half the power
- Programmable gain and offset control
- 1.3 GHz analog input bandwidth
- 52fs Clock Jitter
- Over-range indicator
- Selectable Clock Divider: $\div 1, \div 2$ or $\div 4$
- Clock Phase Selection
- Nap and Sleep modes
- Two's complement, Gray code or Binary data format
- SDR/DDR LVDS-compatible or LVCMOS outputs
- Programmable Built-in Test Patterns
- 1.8V Analog and Digital Supplies


## Applications

- Power Amplifier Linearization
- Radar and Satellite Antenna Array Processing
- Broadband Communications
- High-Performance Data Acquisition
- Communications Test Equipment
- WiMAX and Microwave Receivers



## Key Specifications

- $\quad S N R=65.1 \mathrm{dBFS}$ for $\mathrm{fin}_{\mathrm{I}}=124 \mathrm{MHz}(-1 \mathrm{dBFS})$
- $\quad S F D R=81 \mathrm{dBc}$ for $\mathrm{fin}_{\mathrm{I}}=124 \mathrm{MHz}(-1 \mathrm{dBFS})$
- Power consumption
- 250/199mW @ 250/125MSPS (SDR Mode)
- 203/159mW @ 250/125MSPS (DDR Mode)


## Pin-Compatible Family

| Model | Resolution | Speed (MSPS) |
| :--- | :---: | :---: |
| KAD5514P-25 | 14 | 250 |
| KAD5514P-21 | 14 | 210 |
| KAD5514P-17 | 14 | 170 |
| KAD5514P-12 | 14 | 125 |
| KAD5512P-50 | 12 | 500 |
| KAD5512P-25, KAD5512HP-25 | 12 | 250 |
| KAD5512P-21, KAD5512HP-21 | 12 | 210 |
| KAD5512P-17, KAD5512HP-17 | 12 | 170 |
| KAD5512P-12, KAD5512HP-12 | 10 | 500 |
| KAD5510P-50 |  |  |

## KAD5512P

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## KAD5512P

## Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD $=1.8 \mathrm{~V}, \mathrm{OVDD}=1.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=$ $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, AIN $=-1 \mathrm{dBFS}, \mathrm{f}_{\text {SAMPLE }}=$ Maximum Conversion Rate (per speed grade).

## DC Specifications

| Parameter | Symbol | Conditions | KAD5512P-25 |  |  | KAD5512P-21 |  |  | KAD5512P-17 |  |  | KAD5512P-12 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Analog Input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Full-Scale Analog Input Range | $V_{\text {FS }}$ | Differential | 1.38 | 1.45 | 1.59 | 1.38 | 1.45 | 1.59 | 1.38 | 1.45 | 1.59 | 1.38 | 1.45 | 1.59 | VPP |
| Input Resistance | Rin | Differential |  | 1000 |  |  | 1000 |  |  | 1000 |  |  | 1000 |  | $\Omega$ |
| Input Capacitance | Cin | Differential |  | 4 |  |  | 4 |  |  | 4 |  |  | 4 |  | pF |
| Full Scale Range Temp. Drift | Avtc | Full Temp |  | 90 |  |  | 90 |  |  | 90 |  |  | 90 |  | ppm $/{ }^{\circ} \mathrm{C}$ |
| Input Offset Voltage | Vos |  |  | $\pm 1.5$ |  |  | $\pm 1.5$ |  |  | $\pm 1.5$ |  |  | $\pm 1.5$ |  | mV |
| Gain Error | $\mathrm{E}_{\mathrm{G}}$ |  |  | $\pm 0.6$ |  |  | $\pm 0.6$ |  |  | $\pm 0.6$ |  |  | $\pm 0.6$ |  | \% |
| Common-Mode Output Voltage | $\mathrm{V}_{\mathrm{CM}}$ |  |  | 0.535 |  |  | 0.535 |  |  | 0.535 |  |  | 0.535 |  | V |
| Power Requirements |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1.8V Analog Supply Voltage | AVDD |  | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| 1.8V Digital Supply Voltage | OVDD |  | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| 1.8V Analog Supply Current | I ${ }_{\text {aVdo }}$ |  |  | 78 | TBD |  | 71 | TBD |  | 65 | TBD |  | 58 | TBD | mA |
| 1.8V Digital Supply Current (SDR) | lovdd |  |  | 62 | TBD |  | 58 | TBD |  | 56 | TBD |  | 53 | TBD | mA |
| 1.8V Digital Supply Current (DDR) | lovdd |  |  | 35.2 | TBD |  | 33.4 | TBD |  | 31.9 | TBD |  | 30.1 | TBD | mA |
| Power Supply Rejection Ratio | PSRR |  |  | -53 |  |  | -53 |  |  | -53 |  |  | -53 |  | dBFS |
| Power Dissipation |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Normal Mode (SDR) | PD |  |  | 250 | TBD |  | 233 | TBD |  | 218 | TBD |  | 199 | TBD | mW |
| Normal Mode (DDR) | $\mathrm{P}_{\mathrm{D}}$ |  |  | 203 | TBD |  | 188 | TBD |  | 175 | TBD |  | 159 | TBD | mW |
| Nap Mode | PD |  |  | 40 | TBD |  | 40 | TBD |  | 40 | TBD |  | 40 | TBD | mW |
| Sleep Mode | PD |  |  | 10 | TBD |  | 10 | TBD |  | 10 | TBD |  | 10 | TBD | mW |

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## AC Specifications



## KAD5512P

## Digital Specifications

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Inputs |  |  |  |  |  |  |
| Input Current High (RESETN) | $\mathrm{I}_{\mathrm{H}}$ | $\mathrm{VIN}=1.8 \mathrm{~V}$ | 0 | 1 | 10 | $\mu \mathrm{A}$ |
| Input Current Low (RESETN) | $1 / 2$ | VIN $=0 \mathrm{~V}$ | 25 | 50 | 75 | $\mu \mathrm{A}$ |
| Input Current High (OUTMODE, NAP/SLP, CLKDIV, OUTFMT ) | $\mathrm{IIH}^{\text {H }}$ |  | TBD | 25 | TBD | $\mu \mathrm{A}$ |
| Input Current Low (OUTMODE, NAP/SLP, CLKDIV, OUTFMT ) | $1 / 2$ |  | TBD | 25 | TBD | $\mu \mathrm{A}$ |
| Input Capacitance | $C_{\text {d }}$ |  |  | 3 |  | pF |
| LVDS Outputs |  |  |  |  |  |  |
| Differential Output Voltage | $V_{T}$ |  |  | 210 |  | mV |
| Output Offset Voltage | Vos |  |  | TBD |  | mV |
| Output Rise Time | $t_{R}$ |  |  | 500 |  | ps |
| Output Fall Time | ${ }_{\text {F }}$ |  |  | 500 |  | ps |
| CMOS Outputs |  |  |  |  |  |  |
| Voltage Output High | Vон |  |  | OVDD-0.1 |  | $\checkmark$ |
| Voltage Output Low | VoL |  |  | 0.1 |  | $\checkmark$ |
| Output Rise Time | $t_{R}$ |  |  | TBD |  | ns |
| Output Fall Time | ${ }_{\text {t }}$ |  |  | TBD |  | ns |

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## Switching Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ADC |  |  |  |  |  |
| Aperture Delay | $t_{\text {A }}$ |  | 375 |  | ps |
| RMS Aperture Jitter | $j_{A}$ |  | 52 |  | fs |
| Input Clock to Output Clock Propagation Delay | tcpd | TBD | TBD | TBD | ps |
| Input Clock to Data Propagation Delay | $t_{\text {PD }}$ | TBD | TBD | TBD | ps |
| Output Clock to Data Propagation Delay | toc | TBD | TBD | TBD | ps |
| Latency (Pipeline Delay) | L |  | 7.5 |  | cycles |
| Over Voltage Recovery | tove |  | 1 |  | cycles |

## Timing Diagrams



Figure 1a. LVDS Timing Diagram—DDR


Figure 1b. LVDS Timing Diagram—SDR


Figure 2a. CMOS Timing Diagram—DDR


Figure 2b. CMOS Timing Diagram—SDR

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## Absolute Maximum Ratings ${ }^{1}$

| Parameter | Min | Max | Unit |
| :--- | :---: | :---: | :---: |
| AVDD to AVSS | -0.4 | 2.1 | V |
| OVDD to OVSS | -0.4 | 2.1 | V |
| AVSS to OVSS | -0.3 | 0.3 | V |
| Analog Inputs to AVSS | -0.4 | $\mathrm{AVDD}+0.3$ | V |
| Clock Inputs to AVSS | -0.4 | AVDD +0.3 | V |
| Logic Input to AVSS | -0.4 | OVDD +0.3 | V |
| Logic Inputs to OVSS | -0.4 | OVDD +0.3 | V |
| Operating Temperature | -40 | 85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | -65 | 150 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |

1. Exposing the device to levels in excess of the maximum ratings may cause permanent damage. Exposure to maximum conditions for extended periods may affect device reliability.

## Thermal Impedance

| Parameter | Symbol | Typ | Unit |
| :--- | :---: | :---: | :---: |
| Junction to Paddle $^{2}$ | $\Phi_{\mathrm{JP}}$ | 30 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Junction to Case $^{2}$ | $\Phi_{\mathrm{JC}}$ | TBD | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Junction to Ambient $^{2}$ | $\Phi_{\mathrm{JA}}$ | TBD | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## 2. Paddle soldered to ground plane.

## ESD



Electrostatic charge accumulates on humans, tools and equipment and may discharge through any metallic package contacts (pins, balls, exposed paddle, etc.) of an integrated circuit. Industry-standard protection techniques have been utilized in the design of this product. However, reasonable care must be taken in the storage and handling of ESD sensitive products. Contact Kenet for the specific ESD sensitivity rating of this product.

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## Pin Descriptions-72QFN

| Pin \# | LVDS [LVCMOS] Name | LVDS [LVCMOS] Function |
| :---: | :---: | :---: |
| 1,6,19, 24, 71 | AVDD | 1.8V Analog Supply |
| 2-5, 13, 14, 17, 18, 28-31 | DNC | Do Not Connect |
| 7, 8, 11, 12, 72 | AVSS | Analog Ground |
| 9, 10 | VINN, VINP | Analog Input Negative, Positive |
| 15 | VCM | Common Mode Output |
| 16 | CLKDIV | Clock Divider Control |
| 20, 21 | CLKP, CLKN | Clock Input True, Complement |
| 22 | OUTMODE | Output Mode (LVDS, LVCMOS) |
| 23 | NAPSLP | Power Control (Nap, Sleep modes) |
| 25 | RESETN | Power On Reset (Active Low) |
| 26, 45, 55, 65 | OVSS | Output Ground |
| 27, 36, 56 | OVDD | 1.8V Output Supply |
| 32, 33 | DON, DOP [NC, DO] | LVDS Bit 0 (LSB) Output Complement, True [NC, LVCMOS Bit 0] |
| 34, 35 | DIN, DIP [NC, DI] | LVDS Bit 1 Output Complement, True [NC, LVCMOS Bit 1] |
| 37,38 | D2N, D2P [NC, D2] | LVDS Bit 2 Output Complement, True [NC, LVCMOS Bit 2] |
| 39,40 | D3N, D3P [NC, D3] | LVDS Bit 3 Output Complement, True [NC, LVCMOS Bit 3] |
| 41, 42 | D4N, D4P [NC, D4] | LVDS Bit 4 Output Complement, True [NC, LVCMOS Bit 4] |
| 43, 44 | D5N, D5P [NC, D5] | LVDS Bit 5 Output Complement, True [NC, LVCMOS Bit 5] |
| 46 | RLVDS | LVDS Bias Resistor (connect to OVSS with a 10k 2 , $1 \%$ resistor) |
| 47, 48 | CLKOUTN, CLKOUTP [NC, CLKOUT] | LVDS Clock Output Complement, True [NC, LVCMOS CLKOUT] |
| 49, 50 | D6N, D6P [NC, D6] | LVDS Bit 6 Output Complement, True [NC, LVCMOS Bit 6] |
| 51, 52 | D7N, D7P [NC, D7] | LVDS Bit 7 Output Complement, True [NC, LVCMOS Bit 7] |
| 53, 54 | D8N, D8P [NC, D8] | LVDS Bit 8 Output Complement, True [NC, LVCMOS Bit 8] |
| 57, 58 | D9N, D9P [NC, D9] | LVDS Bit 9 Output Complement, True [NC, LVCMOS Bit 9] |
| 59,60 | DION, DIOP [NC, DIO] | LVDS Bit 10 Output Complement, True [NC, LVCMOS Bit 10] |
| 61,62 | DIIN, DIIP [NC, DII] | LVDS Bit 11 (MSB) Output Complement, True [NC, LVCMOS Bit 11] |
| 63,64 | ORN, ORP [NC, OR] | LVDS Over Range Complement, True [NC, LVCMOS Over Range] |
| 66 | SDO | SPI Serial Data Output ( $4.7 \mathrm{k} \Omega$ pull-up to OVDD is required) |
| 67 | CSB | SPI Chip Select (active low) |
| 68 | SCLK | SPI Clock |
| 69 | SDIO | SPI Serial Data Input/Output |
| 70 | OUTFMT | Output Data Format (Two's Comp., Gray Code, Offset Binary) |
| Exposed Paddle | AVSS | Analog Ground |

LVCMOS Output Mode Functionality is shown in brackets (NC = No Connection)

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## Pin Configuration—72QFN



Figure 3. 72 QFN Pin Configuration

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## Pin Descriptions-48QFN

| Pin \# | LVDS [LVCMOS] Name | LVDS [LVCMOS] Function |
| :---: | :---: | :---: |
| 1, 9, 13, 17, 47 | AVDD | 1.8V Analog Supply |
| 2-4, 11, 21, 22 | DNC | Do Not Connect |
| 5, 8, 12, 48 | AVSS | Analog Ground |
| 6,7 | VINN, VINP | Analog Input Negative, Positive |
| 10 | VCM | Common Mode Output |
| 14, 15 | CLKP, CLKN | Clock Input True, Complement |
| 16 | NAPSLP | Power Control (Nap, Sleep modes) |
| 18 | RESETN | Power On Reset (Active Low) |
| 19, 29, 41 | OVSS | Output Ground |
| 20, 42 | OVDD | 1.8 V Output Supply |
| 23, 24 | DON, DOP [NC, DO] | LVDS Bit 0 (LSB) Output Complement, True [NC, LVCMOS Bit 0] |
| 25, 26 | DIN, DIP [NC, DI] | LVDS Bit 1 Output Complement, True [NC, LVCMOS Bit 1] |
| 27, 28 | D2N, D2P [NC, D2] | LVDS Bit 2 Output Complement, True [NC, LVCMOS Bit 2] |
| 30 | RLVDS | LVDS Bias Resistor (connect to OVSS with a 10k $2,1 \%$ resistor) |
| 31, 32 | CLKOUTN, CLKOUTP [NC, CLKOUT] | LVDS Clock Output Complement, True [NC, LVCMOS CLKOUT] |
| 33, 34 | D3N, D3P [NC, D3] | LVDS Bit 3 Output Complement, True [NC, LVCMOS Bit 3] |
| 35,36 | D4N, D4P [NC, D4] | LVDS Bit 4 Output Complement, True [NC, LVCMOS Bit 4] |
| 37, 38 | D5N, D5P [NC, D5] | LVDS Bit 5 Output Complement, True [NC, LVCMOS Bit 5] |
| 39,40 | ORN, ORP [NC, OR] | LVDS Over Range Complement, True [NC, LVCMOS Over Range] |
| 43 | SDO | SPI Serial Data Output (4.7k pull-up to OVDD is required) |
| 44 | CSB | SPI Chip Select (active low) |
| 45 | SCLK | SPI Clock |
| 46 | SDIO | SPI Serial Data Input/Output |
| Exposed Paddle | AVSS | Analog Ground |

LVCMOS Output Mode Functionality is shown in brackets (NC = No Connection)

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## Pin Configuration-48QFN



Figure 4. 48QFN Pin Configuration

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## Typical Performance Curves




Figure 6. HD2 \& HD3 vs. $\mathrm{f}_{\mathrm{IN}}$
$\square$
Figure 8. HD2 \& HD3 vs. AIn
$\square$
Figure 9. SNR \& SFDR vs. fsample

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## Typical Performance Curves



Figure 11. Power vs. fsAMPLE
$\square$
Figure 13. Integral Nonlinearity
$\square$
Figure 15. Noise Histogram


Figure 12. Differential Nonlinearity


Figure 14. SNR \& SFDR vs. VCM
$\square$
Figure 16. Single Tone Spectrum @ 10 MHz

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## Typical Performance Curves



Figure 17. Single Tone Spectrum @ 70 MHz
$\square$
Figure 19. Single Tone Spectrum @ 240 MHz
$\square$
Figure 21. Two-Tone Spectrum @ 10 MHz


Figure 18. Single Tone Spectrum @ 140 MHz


Figure 20. Single Tone Spectrum @ 500 MHz


Figure 22. Two-Tone Spectrum @ 70 MHz

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## Typical Performance Curves



Figure 23. Two-Tone Spectrum @ 140 MHz
$\square$
Figure 25. Two-Tone Spectrum @ 500 MHz


Figure 27. SNR \& SFDR vs. Power Supply Voltage


Figure 24. Two-Tone Spectrum @ 240 MHz


Figure 26. SNR \& SFDR vs. Temperature

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## Functional Description

The KAD5512P is based upon a 12-bit, 250MSPS A/D converter core that utilizes a pipelined successive approximation architecture (Figure 28). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. The converter pipeline requires six samples to produce a result. Digital error correction is also applied, resulting in a total latency of seven and a half clock cycles. This is evident to the user as a time lag between the start of a conversion and the data being available on the digital outputs.

## Power-On Calibration

At start-up, the core performs a self-calibration to minimize gain and offset errors. An internal power-onreset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins (especially 3, 4 and 18) must not be pulled up or down
- SDO (pin 66) must be high
- RESETN (pin 25) must begin low
- SPI communications must not be attempted A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.
The SDO pin requires an external $4.7 \mathrm{k} \Omega$ pull-up to OVDD. If the SDO pin is pulled low externally during power-up, calibration will not be executed properly.
After the power supply has stabilized the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. The RESETN pin should be connected to an open-drain driver with a drive strength of less than 0.5 mA .
The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 29. The overrange output (OR) is set high once RESETN is pulled low, and remains in that state until calibration is complete. The OR output returns to normal operation at that time, so it's important that the analog input be within the converter's full-scale range in order to observe the transition. If the input is in an over-range condition the OR pin will stay high and it will not be possible to detect the end of the calibration cycle.


Figure 28. ADC Core Block Diagram

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While RESETN is low, the output clock (CLKOUTP/CLKOUTN) stops toggling and is set low. Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RESETN is deasserted. At 250 MSPS the nominal calibration time is 300 ms .


Figure 29. Calibration Timing

## User Initiated Reset

Recalibration of the ADC can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength of less than 0.5 mA is recommended. As is the case during power-on reset, the SDO, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

## Analog Input

The ADC core contains a fully differential input (VINP/VINN) to the sample and hold amplifier (SHA). The ideal full-scale input voltage is 1.45 V , centered at the VCM voltage of 0.535 V as shown in Figure 30 .


Figure 30. Analog Input Range

Best performance is obtained when the analog inputs are driven differentially. The common mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 31 through 33. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 31 and 32.


Figure 31. Transformer Input for General Purpose Applications


Figure 32. Transmission-line Transformer Input for High IF Applications
A back-to-back transformer scheme is used to improve common mode rejection, which keeps the common mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the KAD5512P is $1000 \Omega$.
The SHA design uses a switched capacitor input stage, which creates charge kick-back when the sampling capacitance is reconnected to the input voltage. This kick-back creates a disturbance at the input which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 1:1 transformer and low shunt resistance are recommended for optimal performance.


Figure 33. Differential Amplifier Input

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A differential amplifier, as shown in Figure 33, can be used in applications that require dc-coupling. In this configuration the amplifier will typically dominate the achievable SNR and distortion performance.

## Clock Input

The clock input circuit is a differential pair (see Figure 36). Driving these inputs with a high level (up to $1.8 \mathrm{~V}_{\text {PP }}$ on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels.
The recommended drive circuit is shown in Figure 34. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 to facilitate ac coupling.


Figure 34. Recommended Clock drive
A selectable $2 \mathrm{X} / 4 \mathrm{X}$ divider is provided in series with the clock input. The divider can be used in the 2 X mode with a sample clock equal to twice the desired sample rate. This will result in a clock input with $50 \%$ duty cycle and will maximize the converter's performance.

| CLKDIV Pin | Divide Ratio |
| :---: | :---: |
| AVSS | 2 |
| Float | 1 |
| AVDD | 4 |

Table 1. CLKDIV Pin Settings
The clock divider can also be controlled through the SPI port, which overrides the CLKDIV pin setting. Details on this are contained in the Serial Peripheral Interface section.
A delay-locked loop (DLL) generates internal clock signals for various stages within the charge pipeline. If the frequency of the input clock changes, the DLL may take up to $52 \mu$ s to regain lock at 250MSPS. The lock time is inversely proportional to the sample rate.

## Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter ( $t_{\mathrm{J}}$ ) and SNR is shown in Equation 1 and is illustrated in Figure 35.

$$
S N R=20 \log _{10}\left(\frac{1}{2 \pi f_{\mathbb{N}} t_{J}}\right)
$$

Equation 1.


Figure 35. SNR vs. Clock Jitter
This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure 1. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

## Voltage Reference

A temperature compensated voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each $A / D$ is proportional to the reference voltage. The voltage reference is internally bypassed and is not accessible to the user.

## Digital Outputs

Output data is available as a parallel bus in LVDScompatible or CMOS modes. Additionally, the data can be presented in either double data rate (DDR) or single data rate (SDR) formats. The even numbered output bits are active in DDR mode. When CLKOUT is

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low the MSB and all odd bits are output, while on the high phase the LSB and all even bits are presented. Figures 1 and 2 show the timing relationships for LVDS/CMOS and DDR/SDR modes.
The 48-QFN package option contains six LVDS data outputs, and therefore can only support DDR mode.
Additionally, the drive current for LVDS mode can be set to a nominal 3 mA or a power-saving 2 mA . The lower current setting can be used in designs where the receiver is in close physical proximity to the ADC. The applicability of this setting is dependent upon the PCB layout, therefore the user should experiment to determine if performance degradation is observed.
The output mode and LVDS drive current are selected via the OUTMODE pin as shown in Table 2.

| OUTMODE Pin | Mode |
| :---: | :---: |
| AVSS | LVCMOS |
| Float | LVDS, 3 mA |
| AVDD | LVDS, 2 mA |

Table 2. OUTMODE Pin Settings
The output mode can also be controlled through the SPI port, which overrides the OUTMODE pin setting. Details on this are contained in the Serial Peripheral Interface section.
An external resistor creates the bias for the LVDS drivers. A $10 \mathrm{k} \Omega, 1 \%$ resistor must be connected from the RLVDS pin to OVSS.

## Power Dissipation

The power dissipated by the KAD5512P is primarily dependent on the sample rate, but is also related to the input signal in CMOS output mode. There is a static bias in the analog supply, while the remaining power dissipation is linearly related to the sample rate. The output supply dissipation is approximately constant in LVDS mode, but linearly related to the clock frequency in CMOS mode. Figures 36 and 37 illustrate these relationships.


Figure 36. Power vs. Sample Rate, LVDS Mode


Figure 37. Power vs. Sample Rate, CMOS Mode

## Nap/Sleep

Portions of the device may be shut down to save power during times when operation of the ADC is not required. Two power saving modes are available: nap, and sleep. Nap mode reduces power dissipation to 40 mW and recovers to normal operation in approximately $1 \mu \mathrm{~s}$. Sleep mode reduces power dissipation to 10 mW but requires 1 ms to recover. The clock should remain running and at a fixed frequency during Nap or Sleep. Recovery time from Nap mode will increase if the clock is stopped, since the internal DLL can take up to $52 \mu \mathrm{~s}$ to regain lock at 250MSPS.
By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 3.

| NAPSLP Pin | Mode |
| :---: | :---: |
| AVSS | Normal |
| Float | Sleep |
| AVDD | Nap |

Table 3. NAPSLP Pin Settings

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The power down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in the Serial Peripheral Interface section. This is an indexed function when controlled from the SPI, but a global function when driven from the pin.

## Data Format

Output data can be presented in three formats: two's complement, Gray code and offset binary. The data format is selected via the OUTFMT pin as shown in Table 5.

| OUTFMT Pin | Mode |
| :---: | :---: |
| AVSS | Offset Binary |
| Float | Two's Complement |
| AVDD | Gray Code |

Table 4. OUTFMT Pin Settings
The data format can also be controlled through the SPI port, which overrides the OUTFMT pin setting. Details on this are contained in the Serial Peripheral Interface section.
Offset binary coding maps the most negative input voltage to code $0 \times 000$ (all zeros) and the most positive input to 0xFFF (all ones). Two's complement coding simply complements the MSB of the offset binary representation.
When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 38 shows this operation.


Figure 38. Binary to Gray Code Conversion
Converting back to offset binary from gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 39.


Figure 39. Gray Code to Binary Conversion
Mapping of the input voltage to the various data formats is shown in Table 6.

| Input <br> Voltage | Offset <br> Binary | Two's <br> Complement | Gray <br> Code |
| :---: | :---: | :---: | :---: |
| -Full Scale | 000000000000 | 100000000000 | 000000000000 |
| -Full Scale <br> + 1LSB | 000000000001 | 100000000001 | 000000000001 |
| Mid-Scale | 100000000000 | 000000000000 | 110000000000 |
| +Full Scale <br> -1LSB | 11111111110 | 01111111110 | 100000000001 |
| +Full Scale | 11111111111 | 01111111111 | 100000000000 |

Table 5. Input Voltage to Output Code Mapping

## Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) and serial data input/output (SDIO). The maximum SCLK rate is equal to the ADC sample rate (fsample) divided by 16 for write operations and $\mathrm{f}_{\text {sAMPLE }}$ divided by 66 for reads. At $\mathrm{f}_{\text {SAMPLE }}=$ 250 MHz , maximum SCLK is 15.63 MHz for writing and 3.79 MHz for write operations. There is no minimum SCLK rate.
The following sections describe various registers that are used to configure the SPI or adjust performance

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or functional parameters. Many registers in the available address space ( $0 \times 00$ to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

## SPI Physical Interface

The SPI port operates in a half or full duplex master/slave configuration, with the KAD5512P functioning as a slave. Multiple slave devices can interface to a single master. The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time. If multiple slave devices are selected for reading at the same time, the results will be indeterminate.
The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin. The state of the SDIO pin is set automatically in the communication protocol (described below). A dedicated serial data output pin (SDO) can be activated by setting $0 \times 00[7]$ high to allow operation in full duplex mode.
The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high to low transition on CSB determines the beginning of the two-byte instruction/address com-
mand. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting $0 \times 00[6]$ high. Figures 40 and 41 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented.
In the default mode the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and WO, determine the number of data bytes to be read or written (see Table 6). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 42, and timing values are given in the Switching Specifications section.
After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the ADC (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.


Figure 40. MSB-First Addressing


Figure 41. LSB-First Addressing

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| [W1:W0] | Bytes Transferred |
| :---: | :---: |
| 00 | 1 |
| 01 | 2 |
| 10 | 3 |
| 11 | 4 or more |

Table 6. Byte Transfer Selection
Figures 43 and 44 illustrate the timing relationships for 2-byte and N -byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

## SPI Configuration

## Address 0x00: chip_port_config

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first)
or LSB to MSB (LSB first) to accommodate various microcontrollers.
Bit 7 SDO Active

Bit 6 LSB First
Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.
Bit 5 Soft Reset
Setting this bit high resets all SPI registers to default values.

Bit 4 Reserved
This bit should always be set high.
Bits 3:0 These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.


Figure 42. Instruction/Address Phase


Figure 43. 2-Byte Transfer


Figure 44. N -Byte Transfer

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## Address 0x02: burst_end

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. In 3-wire SPI mode the burst is ended by pulling the CSB pin high. If the device is operated in 2-wire mode the CSB pin is not available. In that case, setting the burst_end address determines the end of the transfer. During a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.
Bits 7:0 Burst End Address
This register value determines the ending address of the burst data.

## DUT Information

## Address 0x08: chip_id

Address 0x09: chip_version
The generic die identifier and a revision number, respectively, can be read from these two registers.

## Indexed DUT Configuration/Control

## Address 0x10: device_index_A

A common SPI map, which can accommodate sin-gle-channel or multi-channel devices, is used for all Kenet ADC products. Certain configuration commands (identified as Indexed in the SPI map) can be executed on a per-converter basis. This register determines which converter is being addressed for an Indexed command. It is important to note that only a single converter can be addressed at a time.
This register defaults to 00h, indicating that no ADC is addressed. Single-channel ADCs must set Bit 0 of this register high in order to execute any Indexed commands.

## Address 0x20: offset_coarse

## Address 0x21: offset_fine

The input offset of the ADC core can be adjusted in fine and coarse steps. Both adjustments are made via an 8 -bit word as detailed in Table 7. The data format is twos complement.
The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

| Parameter | 0x20[7:0] <br> Coarse Offset | 0x21[7:0] <br> Fine Offset |
| :---: | :---: | :---: |
| Steps | 256 | 256 |
| -Full Scale (0x80) | -24.0 mV | -1.7 mV |
| Mid-Scale (0x00) | 0.0 mV | 0.0 mV |
| +Full Scale (0x7F) | +23.8 mV | +1.7 mV |
| Nominal Step Size | $187.5 \mu \mathrm{~V}$ | $13.3 \mu \mathrm{~V}$ |

Table 7. Offset Adjustments

## Address 0x22: gain_coarse

Address 0x23: gain_medium

## Address 0x24: gain_fine

Gain of the ADC core can be adjusted in coarse, medium and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8 -bit. The data format is twos complement for all three registers.
The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

| Parameter | 0x22[3:0] <br> Coarse Gain |
| :---: | :---: |
| Steps | 16 |
| -Full Scale (0x08) | $-11.2 \%$ |
| Mid-Scale (0x00) | $0.0 \%$ |
| +Full Scale (0x07) | $+9.8 \%$ |
| Nominal Step Size | $1.4 \%$ |

Table 8. Coarse Gain Adjustment

| Parameter | 0x23[7:0] <br> Medium Gain | 0x24[7:0] <br> Fine Gain |
| :---: | :---: | :---: |
| Steps | 256 | 256 |
| -Full Scale (0x80) | $-10.56 \%$ | $-1.06 \%$ |
| Mid-Scale (0x00) | $0.0 \%$ | $0.0 \%$ |
| +Full Scale (0x7F) | $+10.48 \%$ | $+1.05 \%$ |
| Nominal Step Size | $0.0825 \%$ | $0.00825 \%$ |

Table 9. Medium and Fine Gain Adjustments

## Address 0x25: modes

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal

## KAD5512P

operation, nap or sleep modes (refer to Nap/Sleep section). This functionality can be overridden and controlled through the SPI. This is an indexed function when controlled from the SPI, but a global function when driven from the pin. This register is not changed by a Soft Reset.

| Value | 0x25[2:0] <br> Power Down Mode |
| :---: | :---: |
| 000 | Pin Control |
| 001 | Normal Operation |
| 010 | Nap Mode |
| 100 | Sleep Mode |

Table 10. Power Down Control

## Global DUT Configuration/Control

## Address 0x71: phase_slip

When using a clock divider, it's not possible to determine the synchronization of the incoming and divided clock phases. This is particularly important when multiple ADCs are used in a time-interleaved system. The phase slip feature allows the rising edge of the divided clock to be advanced by one input clock cycle, as shown in Figure 45.


Figure 45. Phase Slip

## Address 0x72: clock_divide

The KAD5512P has a selectable clock divider that can be set to divide by four, two or one (no division). By default, the tri-level CLKDIV pin selects the divisor (refer to Clock Input section). This functionality can be overridden and controlled through the SPI, as shown in Table 11. This register is not changed by a Soft Reset.

| Value | 0x72[2:0] <br> Clock Divider |
| :---: | :---: |
| 000 | Pin Control |
| 001 | Divide by 1 |
| 010 | Divide by 2 |
| 100 | Divide by 4 |

Table 11. Clock Divider Selection

## Address 0x73: output_mode_A

The output_mode_A register controls the physical output format of the data, as well as the logical coding. The KAD5512P can present output data in two physical formats: LVDS or LVCMOS. Additionally, the drive strength in LVDS mode can be set high (3mA) or low ( 2 mA ). By default, the tri-level OUTMODE pin selects the mode and drive level (refer to Digital Outputs section). This functionality can be overridden and controlled through the SPI, as shown in Table 12.
Data can be coded in three possible formats: two's complement, Gray code or offset binary. By default, the tri-level OUTFMT pin selects the data format (refer to Data Format section). This functionality can be overridden and controlled through the SPI, as shown in Table 13 .
This register is not changed by a Soft Reset.

| Value | 0x93[7:5] <br> Output Mode |
| :---: | :---: |
| 000 | Pin Control |
| 001 | LVDS 2mA |
| 010 | LVDS 3mA |
| 100 | LVCMOS |

Table 12. Output Mode Control

| Value | 0x93[2:0] <br> Output Format |
| :---: | :---: |
| 000 | Pin Control |
| 001 | Two's Complement |
| 010 | Gray Code |
| 100 | Offset Binary |

Table 13. Output Format Control
Address 0x74: output_mode_B
Address 0x75: config_status
Bit 6 DLL Range

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This bit sets the DLL operating range to fast (TBD2MSPS to 250MSPS) or slow (40 to TBDIMSPS).
Bit 4 DDR Enable
Setting this bit enables Double Data-Rate mode.

The output_mode_B and config_status registers are used in conjunction to enable DDR mode and select the frequency range of the DLL clock generator. The method of setting these options is different from the other registers.


Figure 46. Setting output_mode_B register
The procedure for setting output_mode_B is shown in Figure 46. Read the contents of output_mode_B and config_status and XOR them. Then XOR this result with the desired value for output_mode_B and write that XOR result to the register.

| Value | 0xCO[3:0] <br> Output Test Mode | Word 1 | Word 2 |
| :---: | :---: | :---: | :---: |
| 0000 | Off |  |  |
| 0001 | Midscale | $0 \times 8000$ | N/A |
| 0010 | Positive Full-Scale | 0xFFFF | N/A |
| 0011 | Negative Full-Scale | 0x0000 | N/A |
| 0100 | Checkerboard | 0xAAAA | 0x5555 |
| 0101 | Reserved | N/A | N/A |
| 0110 | Reserved | N/A | N/A |
| 0111 | One/Zero | 0xFFFF | 0x0000 |
| 1000 | User Pattern | user_patt1 | user_patt2 |

Table 14. Output Test Modes
Address 0xC2: user_patt1_Isb
Address 0xC3: user_patt1_msb
These registers define the lower and upper eight bits, respectively, of the first user-defined test word.
Address 0xC2: user_patt2_Isb
Address 0xC3: user_patt2_msb
These registers define the lower and upper eight bits, respectively, of the second user-defined test word.

## DUT Test

The KAD5512 can produce preset or user defined patterns on the digital outputs to facilitate in-situ testing. A static word can be placed on the output bus, or two different words can alternate. In the alternate mode, the values defined as Word 1 and Word 2 (as shown in Table 13) are set on the output bus on alternating clock phases.

## Address 0xC0: test_io

Bits 7:6 User Test Mode
These bits set the test mode to static (0x00) or alternate (0x01) mode. Other values are reserved.
The four LSBs in this register (Output Test Mode) determine the test pattern in combination with registers $0 \times C 2$ through 0xC5. Refer to Table 14.

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## SPI Memory Map

|  | Addr <br> (Hex) | Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Def. Value <br> (Hex) | Indexed/ Global |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 00 | port_config | SDO Active | LSB First | Soft Reset |  |  | Mirror (bit5) | Mirror (bit6) | Mirror (bit7) | 00h | G |
|  | 01 | reserved | Reserved |  |  |  |  |  |  |  |  |  |
|  | 02 | burst_end | Burst end address [7:0] |  |  |  |  |  |  |  | 00h | G |
|  | 03-07 | reserved | Reserved |  |  |  |  |  |  |  |  |  |
| $\bigcirc$ | 08 | chip_id | Chip ID \# |  |  |  |  |  |  |  | Read only | G |
| $\bigcirc \subseteq$ | 09 | chip_version | Chip Version \# |  |  |  |  |  |  |  | Read only | G |
|  | 10 | device_index_A | Reserved ${ }^{\text {a }}$ ADC00 |  |  |  |  |  |  |  | 00h | I |
|  | 11-1F | reserved | Reserved |  |  |  |  |  |  |  |  |  |
|  | 20 | offset_coarse | Coarse Offset |  |  |  |  |  |  |  | cal. value | I |
|  | 21 | offset_fine | Fine Offset |  |  |  |  |  |  |  | cal. value | I |
|  | 22 | gain_coarse | Reserved |  |  |  | Coarse Gain |  |  |  | cal. value | 1 |
|  | 23 | gain_medium | Medium Gain |  |  |  |  |  |  |  | cal. value | I |
|  | 24 | gain_fine | Fine Gain |  |  |  |  |  |  |  | cal. value | I |
|  | 25 | modes |  |  |  |  |  | $\|$Power Down Mode [2:0] <br> $000=$ Pin Control <br> $001=$ Normal Operation <br> $010=$ Nap <br> $100=$ Sleep <br> other codes=reserved |  |  |  | 1 |
|  | 26-5F | reserved | Reserved |  |  |  |  |  |  |  |  |  |
|  | 60-6F | reserved | Reserved |  |  |  |  |  |  |  |  |  |
|  | 70 | reserved | Reserved |  |  |  |  |  |  |  |  |  |
|  | 71 | phase_slip | Reserved |  |  |  |  |  |  | Next Clock Edge | 00h | G |
|  | 72 | clock_divide |  |  |  |  |  | Clock Divide [2:0] <br> 000=Pin Control <br> $001=$ divide by 1 <br> 010=divide by 2 <br> $100=$ divide by 4 <br> other codes=reserved |  |  | 00 h NOT <br> affected by Soft Reset | G |
|  | 73 | output_mode_A | Output Mode [2:0] <br> 000=Pin Control <br> 001=LVDS 2mA <br> 010=LVDS 3mA <br> 100=LVCMOS <br> other codes=reserved |  |  |  |  | Output Format [2:0] 000=Pin Control 001=Twos Complement 010=Gray Code 100=Offset Binary other codes=reserved |  |  | $00 h$ NOT <br> affected by Soft Reset | G |
|  | 74 | output_mode_B |  | $\begin{aligned} & \text { DLL Range } \\ & 0=\text { fast } \\ & 1=\text { slow } \end{aligned}$ |  |  |  |  |  |  | OOh NOT affected by Soft Reset | G |
|  | 75 | config_status |  | XOR Result |  | XOR Result |  |  |  |  | Read Only | G |
|  | 76-BF | reserved | Reserved |  |  |  |  |  |  |  |  |  |
| $\frac{\frac{\pi}{0}}{\frac{\oplus}{5}}$ | C0 | test_io | $\begin{aligned} & \text { User Test Mode [2:0] } \\ & 00=\text { Single } \\ & 01=\text { Alternate } \\ & 10=\text { Single Once } \\ & 11=\text { Alternate Once } \end{aligned}$ |  | Reset PN | Reset PN Short Gen | Output Test Mode [3:0] |  |  |  | 00h | G |
|  |  |  |  |  | Long Gen |  | $\begin{aligned} & \hline 0=\text { Off } \\ & 1=\text { Midscale Short } \\ & 2=+ \text { FS Short } \\ & 3=- \text { FS Short } \\ & 4=\text { Checker Board } \\ & 5=\text { reserved } \\ & 6=\text { reserved } \end{aligned}$ |  | 7=One/Zero Word Toggle 8=User Input <br> 9-15=reserved |  |  |  |
|  | C1 | Reserved | Reserved |  |  |  |  |  |  |  | 00h | G |
|  | C2 | user_pattl_Isb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h | G |
|  | C3 | user_pattl_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h | G |
|  | C4 | user_patt2_Isb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h | G |
|  | C5 | user_patt2_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h | G |
|  | C6-FF | reserved |  |  |  | Res | erved |  |  |  |  |  |

Table 15. SPI Memory Map

## Equivalent Circuits



Figure 47. Analog Inputs


Figure 48. Clock Inputs


Figure 49. Tri-Level Digital Inputs


Figure 50. Digital Inputs


Figure 51. LVDS Outputs


Figure 52. CMOS Outputs


Figure 53. VCM_OUT Output

## Layout Considerations

## Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. Many complex board designs benefit from isolating the analog and digital sections. Analog supply and ground planes should be laid out under signal and clock inputs. Locate the digital planes under outputs and logic pins. Grounds should be joined under the chip.

## Clock Input Considerations

Use matched transmission lines to the transformer inputs for the analog input and clock signals. Locate transformers and terminations as close to the chip as possible.

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## Exposed Paddle

The exposed paddle must be electrically connected to analog ground (AVSS) and should be connected to a large copper plane using numerous vias for optimal thermal performance.

## Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is a good choice. For best performance, keep ceramic bypass capacitors very close to device pins. Longer traces will increase inductance, resulting in diminished dynamic performance and accuracy. Make sure that connections to ground are direct and low impedance. Avoid forming ground loops.

## LVDS Outputs

Output traces and connections must be designed for $50 \Omega$ ( $100 \Omega$ differential) characteristic impedance. Keep traces direct and minimize bends where possible. Avoid crossing ground and power plane breaks with signal traces.

## LVCMOS Outputs

Output traces and connections must be designed for $50 \Omega$ characteristic impedance.

## Unused Inputs

Standard logic inputs (RESETN, CSB, SCLK, SDIO, SDO) which will not be operated do not require connection to ensure optimal ADC performance. These inputs can be left floating if they are not used. Tri-level inputs (NAPSLP, OUTMODE, OUTFMT, CLKDIV) accept a floating input as a valid state, and therefore should be biased according to the desired functionality.

## Definitions

Analog Input Bandwidth is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB from its full-scale low-frequency value. This is also referred to as Full Power Bandwidth.
Aperture Delay or Sampling Delay is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.
Aperture Jitter is the RMS variation in aperture delay for a set of samples.

Clock Duty Cycle is the ratio of the time the clock wave is at logic high to the total time of one clock period.
Differential Non-Linearity (DNL) is the deviation of any code width from an ideal 1 LSB step.
Effective Number of Bits (ENOB) is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: $\mathrm{ENOB}=$ (SINAD-1.76) / 6.02
Gain Error is the ratio of the difference between the voltages that cause the lowest and highest code transitions to the full-scale voltage (less 2 LSB). It is typically expressed in percent.
Integral Non-Linearity (INL) is the deviation of each individual code from a line drawn from negative fullscale ( $1 / 2$ LSB below the first code transition) through positive full-scale ( $1 / 2$ LSB above the last code transition). The deviation of any given code from this line is measured from the center of that code.
Least Significant Bit (LSB) is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is $\mathrm{V}_{\text {FS }} /\left(2^{\mathrm{N}}-1\right)$ where N is the resolution in bits.

Missing Codes are output codes that are skipped and will never appear at the ADC output. These codes cannot be reached with any input value.
Most Significant Bit (MSB) is the bit that has the largest value or weight.
Pipeline Delay is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the data.
Power Supply Rejection Ratio (PSRR) is the ratio of a change in input voltage necessary to correct a change in output code that results from a change in power supply voltage.
Signal to Noise-and-Distortion (SINAD) is the ratio of the RMS signal amplitude to the RMS value of the sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

Signal-to-Noise Ratio (without Harmonics) is the ratio of the RMS signal amplitude to the sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.
SNR and SINAD are either given in units of dBC ( dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS ( $d B$ to full scale) when the converter's full-scale input power is used as the reference.

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Spurious-Free-Dynamic Range (SFDR) is the ratio of the RMS signal amplitude to the RMS value of the peak spurious spectral component. The peak spurious spectral component may or may not be a harmonic.
Two-Tone SFDR is the ratio of the RMS value of the lowest power input tone to the RMS value of the peak spurious component, which may or may not be an IMD product.

## Outline Dimensions-72QFN



Figure 54. 72QFN Dimensions

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## Outline Dimensions-48QFN



NDTE:

1) TSLP AND SLP SHARE THE SAME EXPDSE ZUTLINE BUT WITH DIFFERENT THICKNESS:

|  |  | $T S L F$ | $S L P$ |
| :---: | :---: | :---: | :---: |
| $A$ | MAX. | 0.800 | 0.900 |
|  | NロM. | 0.750 | 0.850 |
|  | MIN. | 0.700 | 0.800 |



SIDE VIEW

Figure 55. 48QFN Dimensions

## KAD5512P

## Ordering Guide

The KAD5512P is compliant with EU directive 2002/95/EC regarding the Restriction of Hazardous Substances (RoHS). Contact Kenet for a materials declaration for this product.

| Model | Speed | Package | Temp. Range |
| :--- | :--- | :--- | :---: |
| KAD5512P-25Q72 | 250 MSPS | $72-\mathrm{QFN}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| KAD5512P-21Q72 | 210 MSPS | $72-\mathrm{QFN}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| KAD5512P-17Q72 | 170 MSPS | $72-\mathrm{QFN}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| KAD5512P-12Q72 | 250 MSPS | $72-\mathrm{QFN}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| KAD5512P-25Q48 | 210 MSPS | $48-\mathrm{QFN}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| KAD5512P-21Q48 | 170 MSPS | $48-Q F N$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| KAD5512P-17Q48 | $125 M S P S$ | $48-Q F N$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| KAD5512P-12Q48 | $48-Q F N$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |

## Revision History

| 14-May-07: | Rev 0.1 | Updated to new format |
| :--- | :--- | :--- |
| 21-Jun-07: | Rev 0.2 | Errata Updated |
| 13-Aug-07: | Rev 0.3 | Content/specification updates |
| 07-Dec-07: | Rev 0.4 | Content/specification updates |
| 21-Feb-08: | Rev 0.5 | Updated specifications, added functional descriptions |

## Preliminary Datasheet

This datasheet contains preliminary technical data, which is subject to change without notice. Contact Kenet prior to initiating design activity using this product.

