DATA SHEET

Part No.	AN8150FB
Package Code No.	QFP044-P-1010F

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Contents

AN8150FB

Octal, high precision 13-bit voltage output DAC

■ Overview

AN8150FB is IC which has octal 13 bit DACs constituted by Bi-CMOS process.

■ Features

- Resolution: 13-bit
- Built-in DAC: 8 DACs.
- Integral linearity error: ±2 LSB typ.
- Differential linearity error: ±0.5 LSB typ.
- Supply voltage: +10.5 V (AV_{CC}), –7.5 V (AV_{EE}), +5 V (V_{DD})
- Output range: –3.3 V to +7.7 V
- DAC input data: 13-bit parallel
- DAC selection address data: 3-bit parallel
- Input interface: TTL compatible

■ Applications

- Industrial instrumentation

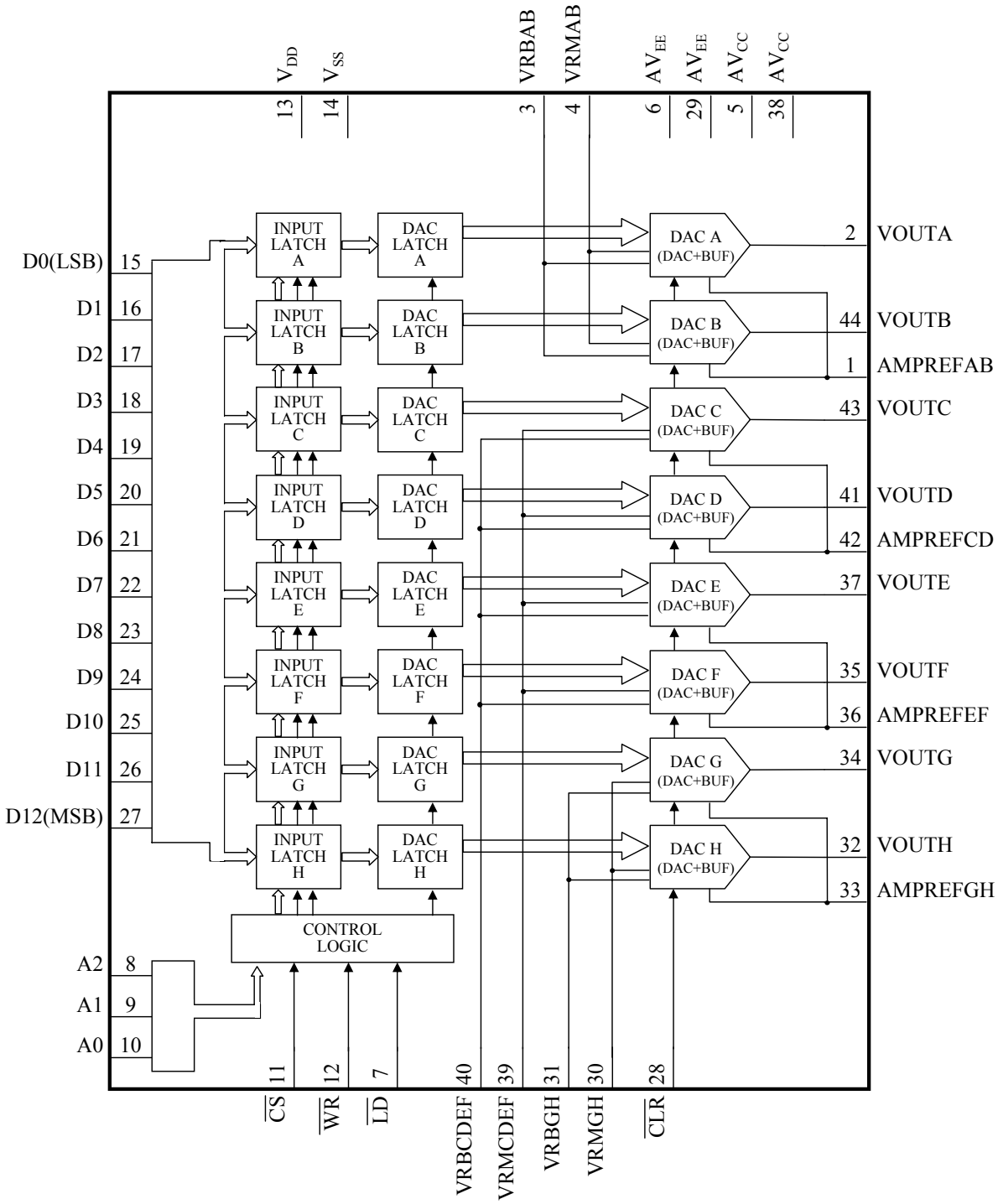
■ Package

- 44 pin plastic quad flat package (QFP type)

■ Type

- Silicon monolithic bipolar IC

■ Block Diagram



Note) This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	AMPREFAB	Input	Offset adjustment for DAC A, B
2	VOUTA	Output	Output voltage of DAC A
3	VRBAB	Input	Reference voltage (Bottom) for DAC A, B
4	VRMAB	Input	Reference voltage (Midpoint) for DAC A, B
5	AV_{CC}	Power supply	Analogue positive supply voltage
6	AV_{EE}	Power supply	Analogue negative supply voltage
7	$\overline{LD}$	Input	Load input
8	A2	Input	Address 2 digital input (MSB)
9	A1	Input	Address 1 digital input
10	A0	Input	Address 0 digital input (LSB)
11	$\overline{CS}$	Input	Chip selection digital input
12	$\overline{WR}$	Input	Write digital input
13	V_{DD}	Power supply	Digital positive supply voltage
14	V_{SS}	GND	Ground for digital
15	D0(LSB)	Input	Digital input (LSB)
16	D1	Input	Digital input
17	D2	Input	Digital input
18	D3	Input	Digital input
19	D4	Input	Digital input
20	D5	Input	Digital input
21	D6	Input	Digital input
22	D7	Input	Digital input
23	D8	Input	Digital input
24	D9	Input	Digital input
25	D10	Input	Digital input
26	D11	Input	Digital input
27	D12(MSB)	Input	Digital input (MSB)
28	$\overline{CLR}$	Input	Asynchronous clear input
29	AV_{EE}	Power supply	Analogue negative supply voltage
30	VRMGH	Input	Reference voltage (Midpoint) for DAC G, H
31	VRBGH	Input	Reference voltage (Bottom) for DAC G, H
32	VOUTH	Output	Output voltage of DAC H
33	AMPREFGH	Input	Offset adjustment for DAC G, H
34	VOUTG	Output	Output voltage of DAC G

■ Pin Descriptions (continued)

Pin No.	Pin name	Type	Description
35	VOUTF	Output	Output voltage of DAC F
36	AMPREFEF	Input	Offset adjustment for DAC E, F
37	VOUTE	Output	Output voltage of DAC E
38	AV_{CC}	Power supply	Analog positive supply voltage
39	VRMCDEF	Input	Reference voltage (Midpoint) for DAC C, D, E, F
40	VRBCDEF	Input	Reference voltage (Bottom) for DAC C, D, E, F
41	VOUTD	Output	Output voltage of DAC D
42	AMPREFCD	Input	Offset adjustment for DAC C, D
43	VOUTC	Output	Output voltage of DAC C
44	VOUTB	Output	Output voltage of DAC B

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage	$AV_{CC} - AV_{EE}$	19.7	V	*1
		V_{DD}	7	V	
2	Supply current	I_{CC}	50	mA	—
		I_{EE}	–50	mA	—
		I_{DD}	10	mA	—
3	Power dissipation	P_D	359	mW	*2
4	Operating ambient temperature	T_{opr}	0 to +70	°C	*3
5	Storage temperature	T_{stg}	–55 to +125	°C	*3

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The power dissipation shown is the value at T_a = 70°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the • $P_D - T_a$ diagram in the ■ Technical Data and use under the condition not exceeding the allowable value.

*3: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
Supply voltage range	AV_{CC}	+10.0 V to +11.0 V	V	—
	AV_{EE}	–7.7 V to –6.8 V		—
	V_{DD}	4.75 V to 5.25 V		—

Note) The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Electrical Characteristics at AV_{CC} = 10.5 V, AV_{EE} = –7.5 V, V_{DD} = 5 V

Note) T_a = 25°C±2° unless otherwise specified.

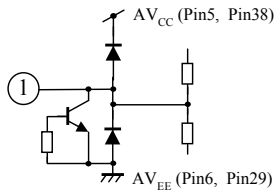
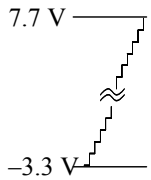
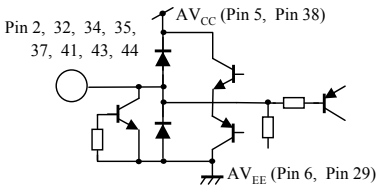
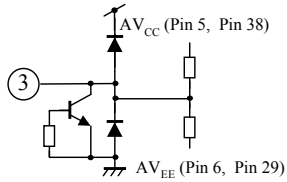
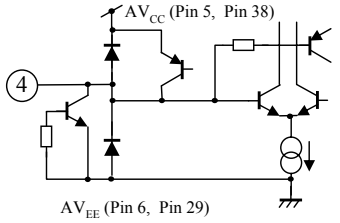
B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
1	Supply current	I_{CC}	—	28	33	38	mA	—
2	Supply current	I_{EE}	—	–33	–28	–23	mA	—
3	Supply current	I_{DD}	—	—	0.01	1	mA	—
4	High digital input current	I_{IH}	—	–1	—	1	µA	—
5	Low digital input current	I_{IL}	—	–1	—	1	µA	—
6	High reference resistor current (1)	I_{VRM}	VRMAB, VRMGH VRM = 2.2 V, VRB = 0 V	–3	–1.5	—	µA	—
7	Low reference resistor current (1)	I_{VRB}	VRBAB, VRBGH VRM = 2.2 V, VRB = 0 V	–1 870	–1 600	–1 330	µA	—
8	High reference resistor current (2)	I_{VRM}	VRMCDEF VRM = 2.2 V, VRB = 0 V	–6	–3	—	µA	—
9	Low reference resistor current (2)	I_{VRB}	VRBCDEF VRM = 2.2 V, VRB = 0 V	–3 740	–3 200	– 2 660	µA	—
10	High-level digital input voltage	D_{IH}	—	$0.7 \times V_{DD}$	—	V_{DD}	V	—
11	Low-level digital input voltage	D_{IL}	—	V_{SS}	—	$0.3 \times V_{DD}$	V	—
12	Max. output voltage	V_{OMAX}	—	$AV_{CC} - 2$	—	—	V	*1
13	Min. output voltage	V_{OMIN}	—	—	—	$AV_{EE} + 3$	V	*1
14	Reference voltage (midpoint)	V_{RM}	—	VRB	2.2	—	V	*1
15	Reference voltage (bottom)	V_{RB}	—	—	0	VRM	V	*1
16	Resolution	Res	—	—	13	—	Bits	—
17	Linearity error	E_L	—	—	±2	±4	LSB	—
18	Differential linearity error	E_D	—	—	±0.5	±1	LSB	—
19	Full-scale error	E_{FS}	—	—	±4	±8	LSB	—
20	Zero-scale error	E_{ZS}	—	—	±4	±8	LSB	
21	Gain error	E_G	—	—	±4	±10	LSB	
22	Offset error	E_{OFF}	—	—	±4	±8	LSB	
23	Output voltage slew rate	SR	—	3	—	—	V/µs	
24	Settling time	T_{ST}	—	—	—	30	µs	

Note) *1: Sets so that the following conditions are satisfied. For details, refer to ■ Technical Data.
$V_{OMAX} = 5 \times VRM - 2.5 \times VRB - 1.5 \times AMPREF < AV_{CC} - 2$ V
$V_{OMIN} = 2.5 \times VRB - 1.5 \times AMPREF > AV_{EE} + 3$ V

■ Technical Data

1. I/O block circuit diagrams and pin function descriptions

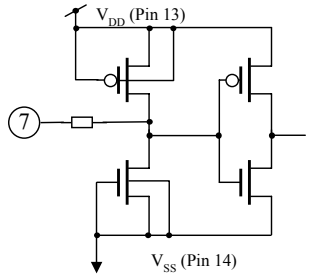
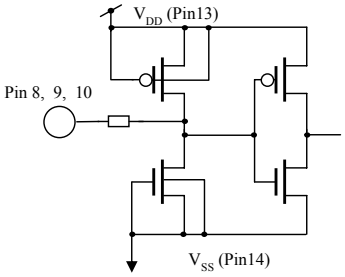
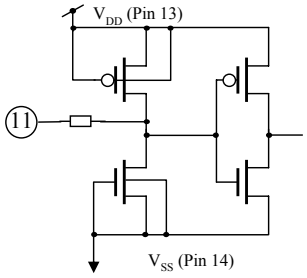
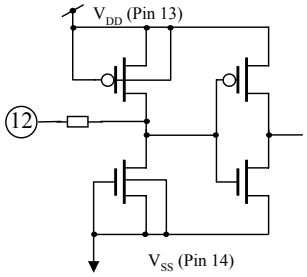
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
1	DC = 2.2 V		10 MΩ or more	Offset adjustment pin of DAC A, B. Apply the same voltage as VRMAB normally.
2, 32, 34, 35, 37, 41, 43, 44			80 Ω	DAC A to H output voltage
3	DC = 0 V		1.38 kΩ or more	Reference voltage of DAC A, B (bottom). Apply 0 V normally.
4	DC = 2.2 V		10 MΩ or more	Reference voltage of DAC A, B (midpoint) VRTAB. i.e., 2 × (VRMAB–VRBAB) is generated inside the IC. DAC A, B output amplitude = 2.5 × (VRTAB – VRBAB)
5, 38	+10.0 V to +11.0 V	—	—	Analog positive supply voltage Apply 10.5 V normally
6, 29	–7.7 V to –6.8 V	—	—	Analog negative supply voltage Apply –7.5 V normally.

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
7	5 V 0 V		10 MΩ or more	Load input Transfer the data of input latch to DAC latch at LD. Start DAC settling.
8, 9, 10	5 V 0 V		10 MΩ or more	Address input A2: MSB, A0: LSB
11	5 V 0 V		10 MΩ or more	Chip select digital input Level trigger. DAC determined by A1, A2, and A0 is selected when this pin is low.
12	5 V 0 V		10 MΩ or more	Write digital input Level trigger. The data is written to the input latch of DAC selected at A2, A1, A0 when this pin is low.
13	+4.75 V to +5.25 V	—	—	Digital positive supply voltage Apply 5 V normally.
14	0 V	—	—	Digital ground

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

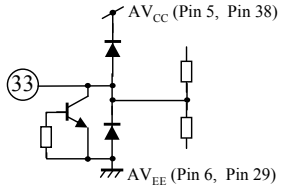
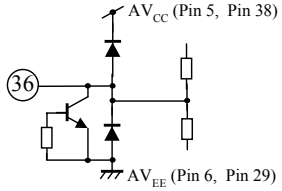
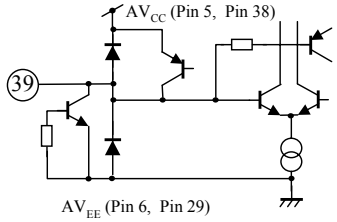
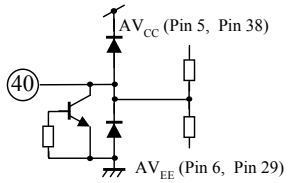
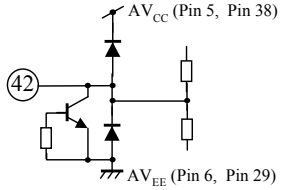
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
15 to 27	5 V 0 V	V_{DD} (Pin 13) Pin 15 to 27 V_{SS} (Pin 14)	10 MΩ or more	Digital input DB0: LSB, DB12: MSB
28	5 V 0 V	V_{DD} (Pin 13) 28 V_{SS} (Pin 14)	10 MΩ or more	Asynchronous clear input 0 V is output during low. The previous value is hold as for latch.
30	DC = 2.2 V	AV_{CC} (Pin 5, Pin 38) 30 AV_{EE} (Pin 6, Pin 29)	10 MΩ or more	Reference voltage of DAC G, H (midpoint) VRTGH. i.e., 2 × (VRMGH – VRBGH) is generated inside the IC. DAC G, H output amplitude = 2.5 × (VRTGH – VRBGH)
31	DC = 0 V	AV_{CC} (Pin 5, Pin 38) 31 AV_{EE} (Pin 6, Pin 29)	1.38 kΩ	Reference voltage of DAC G, H (bottom). Apply 0 V normally.

■ Technical Data (continued)

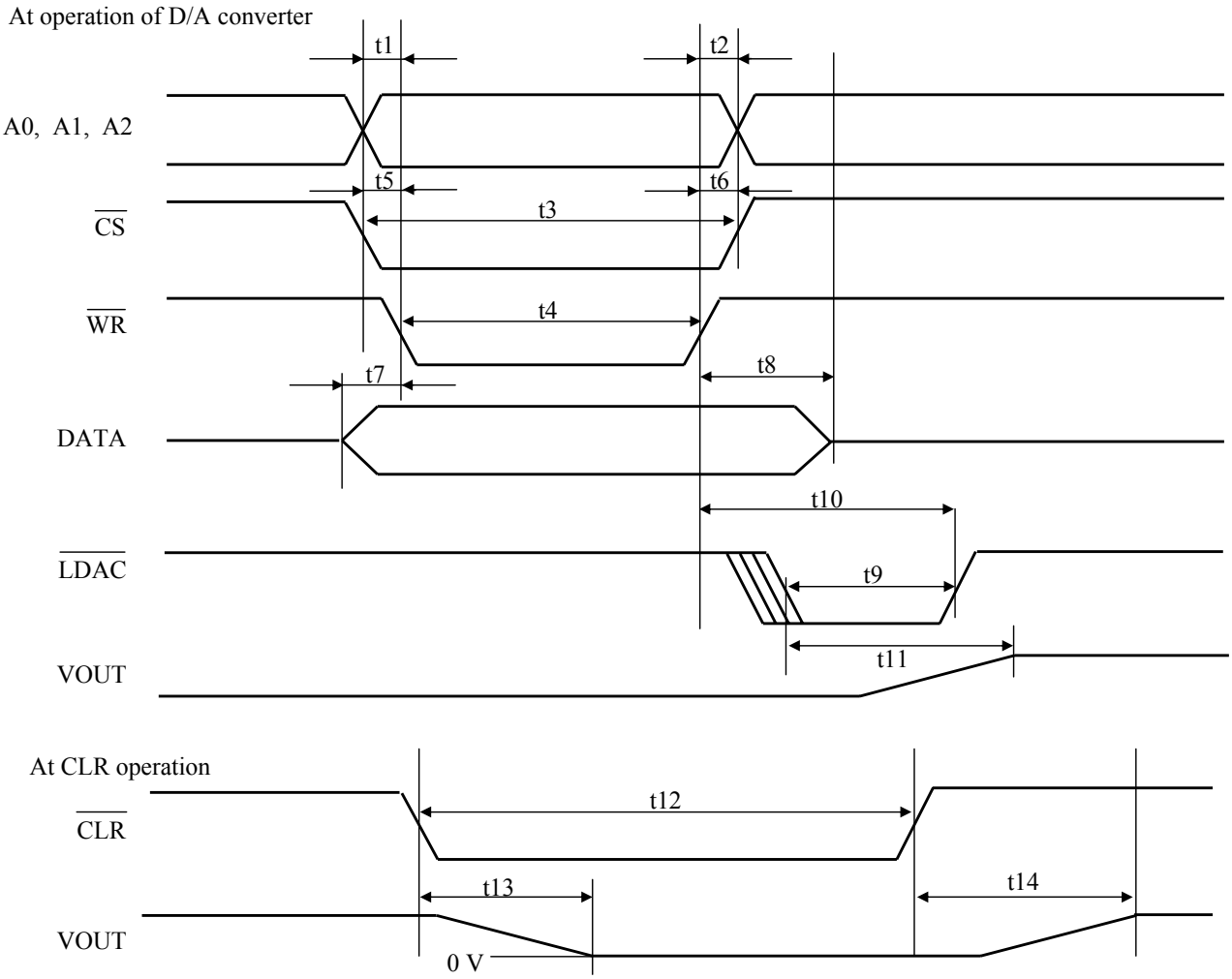
1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
33	DC = 2.2 V		9 kΩ	Offset adjustment pin of DAC G, H. Apply the same voltage as VRMGH normally.
36	DC = 2.2 V		9 kΩ	Offset adjustment pin of DAC E, F. Apply the same voltage as VRMEF normally.
39	DC = 2.2 V		10 MΩ or more	Reference voltage of DAC C, D, E, F (midpoint) VRTAB. i.e., 2 × (VRMCDEF – VRBCDEF) is generated inside the IC. DAC C, D, E, F output amplitude = 2.5 × (VRTCDEF – VRBCDEF)
40	DC = 0 V		0.69 kΩ	Reference voltage of DAC C, D, E, F (bottom). Apply 0 V normally.
42	DC = 2.2 V		9 kΩ	Offset adjustment pin of DAC C, D. Apply the same voltage as VRMCD normally.

■Technical Data (continued)

2. Timing chart



Symbol	Rating	Unit	Description
t1	25	ns	Setup time of A0, A1, A2 compared to $\overline{WR}$
t2	25	ns	Hold time of A0, A1, A2 compared to $\overline{WR}$
t3	75	ns	Pulse width of $\overline{CS}$
t4	75	ns	Min. pulse width of $\overline{WR}$
t5	0	ns	Setup time of $\overline{CS}$ compared to $\overline{WR}$
t6	0	ns	Hold time of $\overline{CS}$ compared to $\overline{WR}$
t7	15	ns	Setup time of DATA compared to $\overline{WR}$
t8	15	ns	Hold time of DATA compared to $\overline{WR}$
t9	75	ns	Min. pulse width of $\overline{LDAC}$
t10	100	ns	Setup time of $\overline{WR}$ compared to $\overline{LDAC}$
t11	30	µs	Settling time of VOUT compared to $\overline{LDAC}$
t12	75	ns	Min. pulse width of $\overline{CLR}$
t13	30	µs	Settling time of VOUT compared to $\overline{CLR}$
t14	30	µs	Settling time of VOUT compared to $\overline{CLR}$ cancel

■ Technical Data (continued)

3. Truth table

DAC address

A2	A1	A0	機能
0	0	0	DAC A input latch
0	0	1	DAC B input latch
0	1	0	DAC C input latch
0	1	1	DAC D input latch
1	0	0	DAC E input latch
1	0	1	DAC F input latch
1	1	0	DAC G input latch
1	1	1	DAC H input latch

DAC operation

CLR	LD	WR	CS	INPUT LATCH	DAC LATCH
1	0	0	0	T	T
1	1	1	x	L	L
1	1	x	1	L	L
1	x	0	0	T	x
1	x	1	x	L	x
1	x	x	1	L	x
1	0	x	x	x	T (0 V)
0	x	x	x	T (0 V)	T (0 V)

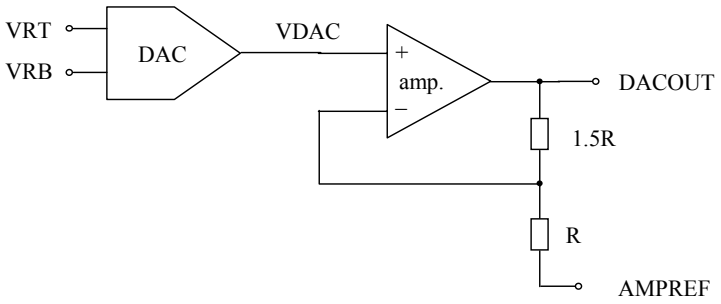
Note) T: through
L: latch

■ Technical Data (continued)

4. DAC code table

	Bipolar	Unipolar
VRM	2.2 V (VRT = 4.4 V) *1	2 V (VRT = 4 V)
VRB	0 V	0 V
Output amplitude	11 V[p-p]	10 V[p-p]
Midpoint electric potential	2.2 V	2 V
DACOUT (Max)	7.69866 V	6.99878 V
DACOUT (Min)	–3.3 V	–3 V
1 1111 1111 1111	7.69866 V	6.99878 V
:	:	:
1 0000 0000 0001	2.20134 V	2.00122 V
1 0000 0000 0000	2.2 V	2 V
0 1111 1111 1111	2.19866 V	1.99878 V
:	:	:
0 0000 0000 0001	–3.29866 V	–2.99878 V
0 0000 0000 0000	–3.3 V	–3 V

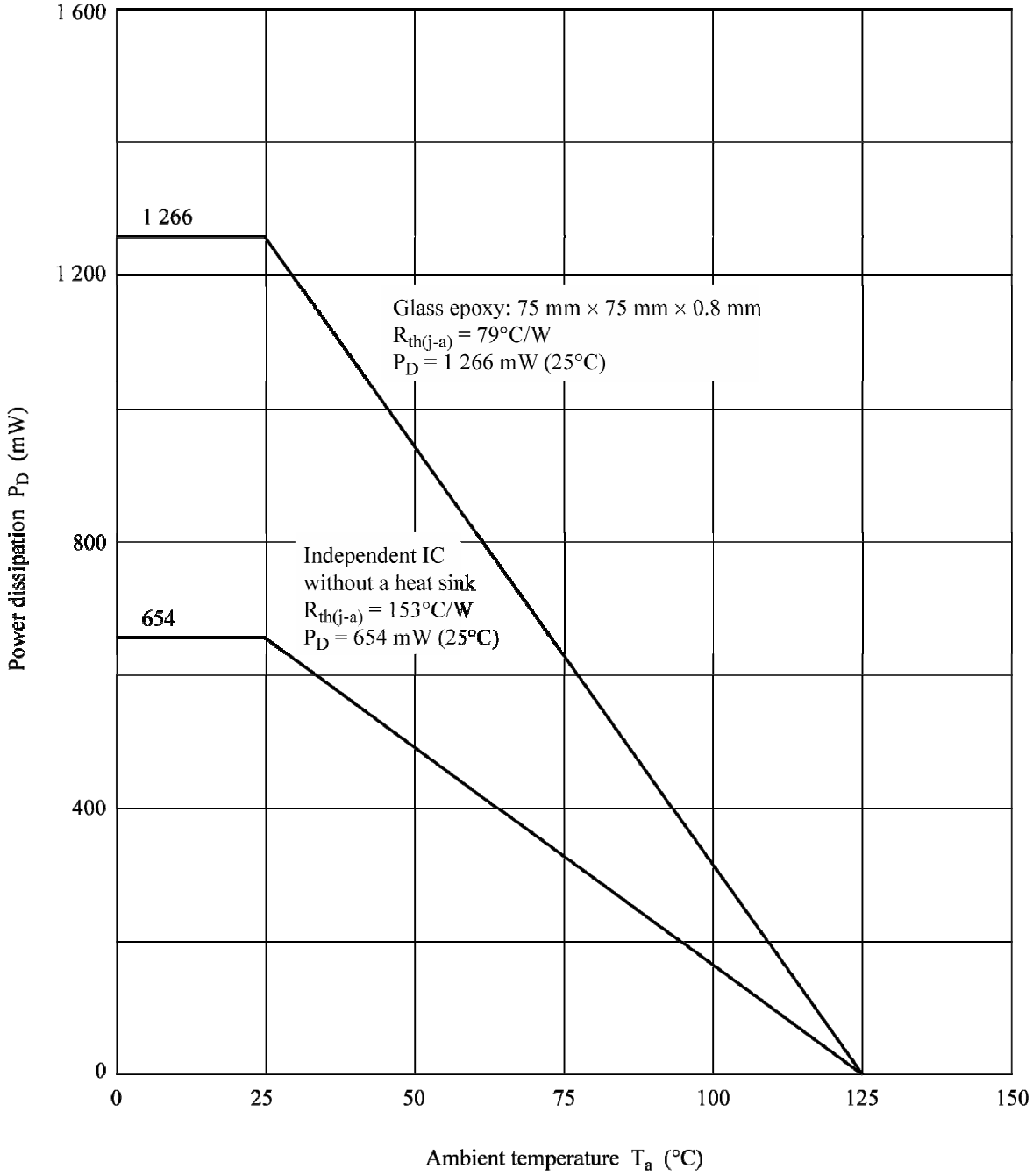
Note) *1: VRT = 2 × VRM – VRB (generated inside)
VDAC = (VRM–VRB) × 2 × D/8192+VRB (internal DAC output voltage)
DACOUT = 2.5 × VDAC – 1.5 × AMPREF
AMPREF = VRM



Equivalent circuit of DAC output block

■ Technical Data (continued)

5. P_D — T_a diagram



■ Usage Notes

1. This IC is intended to be used for Industrial instrumentation.
   Consult our sales staff in advance for information on the following applications:
   • Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   • Any applications other than the standard applications intended.
   1) Space appliance (such as artificial satellite, and rocket)
   2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   3) Medical equipment for life support
   4) Submarine transponder
   5) Control equipment for power plant
   7) Weapon
   8) Others: Applications of which reliability equivalent to 1) to 7) is required.

2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin – V_{CC} short (Power supply fault), output pin – GND short (Ground fault), or output-to-output-pin short (load short).
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

6. When using the LSI for new models, verify the safety including the long-term reliability for each product.

7. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.

8. Power-on sequence
   Note that this IC may be latched up depending on the power-on sequence because it has positive/negative multi-power supplies.
   The recommended power-on sequence is described below.
   1) DV_{DD}
   ↓
   2) AV_{CC} , VRT, VRB, AMPREF (No sequence limit)
   Note) The sequence of AV_{EE} does not matter; that is, AV_{EE} does not malfunction either before or after DV_{DD} .

9. DV_{DD} voltage supply range
   The conversion accuracy of this IC may deteriorates depending on the voltage of DV_{DD} and VRM.
   Use the IC within the following range.
   $2 \times VRM - VRB - DV_{DD} \leq 0.3$ V

10. The conversion accuracy of this IC deteriorates depending on the voltage of VRM. Use the IC within the following range.
    $VRB \geq -0.3$ V

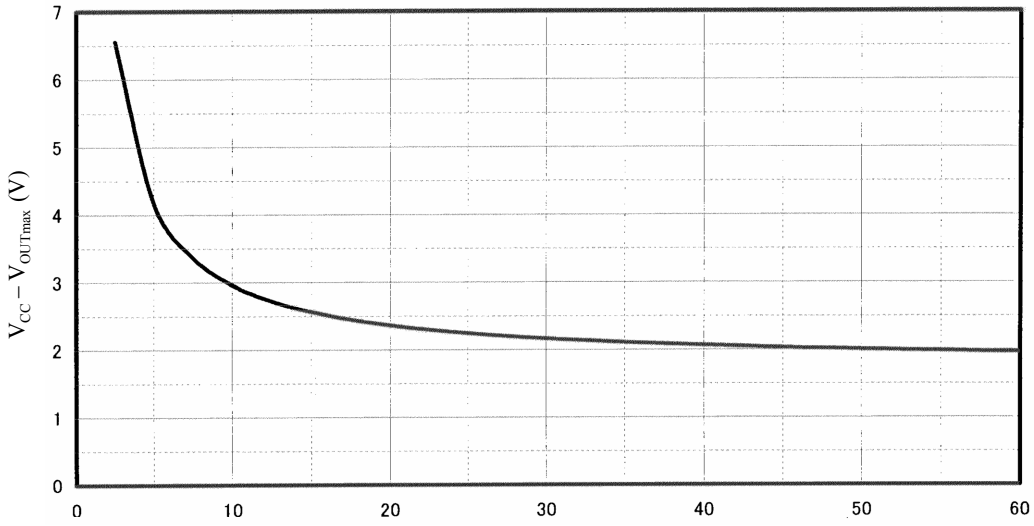
■ Usage Notes (continued)

11. Output voltage and load resistance

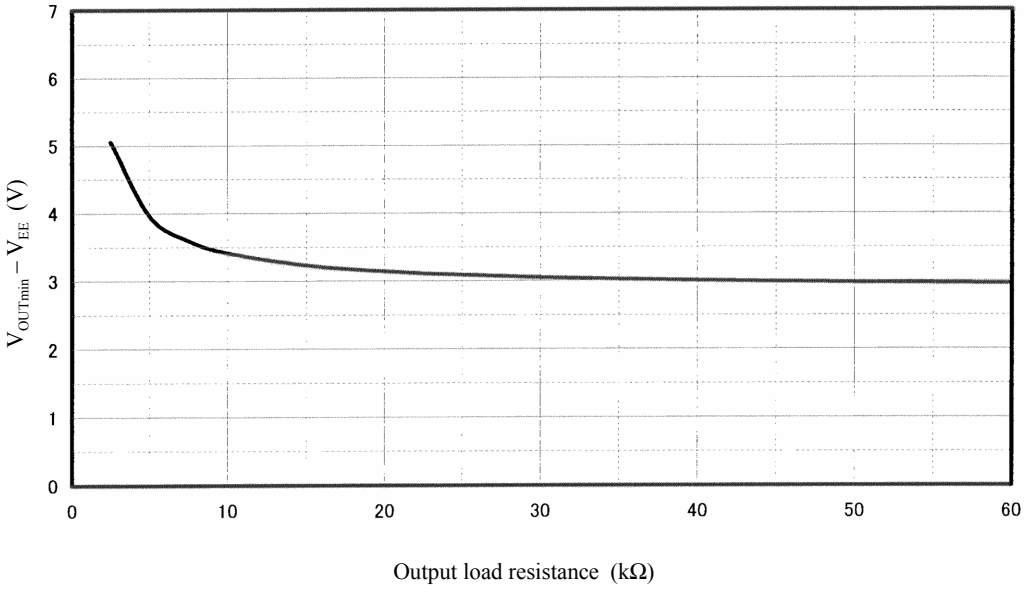
This IC has been designed to drive an output load resistance of 50 Ω. When this IC is used with a resistance under 50 kΩ, the integral linearity error might be worse. In this case, raise the power supply voltage to prevent it.

Determine the power supply voltage referring to the diagrams below.

$V_{CC} - V_{OUTmax}$ output load resistance characteristics



$V_{EE} - V_{OUTmin}$ output load resistance characteristics



Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products, and no license is granted under any intellectual property right or other right owned by our company or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.