National Semiconductor

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LP5952
350mA Dual Rail Linear Regulator

General Description

The LP5952 is a Dual Supply Rail Linear Regulator optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries.

In the typical post regulation application V_{BATT} is directly connected to the battery (range 2.5V...5.5V) and V_{IN} is supplied by the output voltage of the DC-DC Converter (range 0.7V... 4.5V).

The device offers superior dropout and transient features combined with very low quiescent currents. In shutdown mode (Enable pin pulled low) the device turns off and reduces battery consumption to 0.1µA (typ.).

The LP5952 also features internal protection against over-temperature, over-current and under-voltage conditions.

Performance is specified for a -40°C to 125°C junction temperature range.

The LP5952 is available in a micro SMD package, lead free.

The device is available in fixed output voltages in the range of 0.5V to 2.0V. For availability, please contact your local NSC sales office.

Features

- Excellent load transient response: ±15mV typical
- Excellent line transient response: ±1mV typical
- $0.7V \le V_{IN} \le 4.5V$
- $2.5V \le V_{BATT} \le 5.5V$
- $0.5V \le V_{OUT} \le 2.0V$
- For I_{LOAD} = 350mA: $V_{BATT} \ge V_{OUT(NOM)}$ + 1.5V or 2.5V whichever is higher
- For I_{LOAD} = 150mA: $V_{BATT} \ge V_{OUT(NOM)}$ + 1.3V or 2.5V whichever is higher
- 50µA typical quiescent current from V_{BATT}
- 10µA typical quiescent current from V_{IN}
- 0.1µA typical quiescent current in shutdown
- Guaranteed 350mA output current
- Noise voltage = 100µV_{RMS} typical
- Operates from a single Li-Ion cell or 3 cell NiMH/NiCd batteries
- Only one or two tiny surface-mount external components required depending on application
- Small 5 bump micro SMD package, lead free
- Thermal-overload and short-circuit protection
- -40°C to +125°C junction temperature range

Applications

- Mobile Phones
- Hand-Held Radios
- Personal Digital Assistants
- Palm-Top PCs
- Portable Instruments
- Battery Powered Devices

Typical Application Circuit

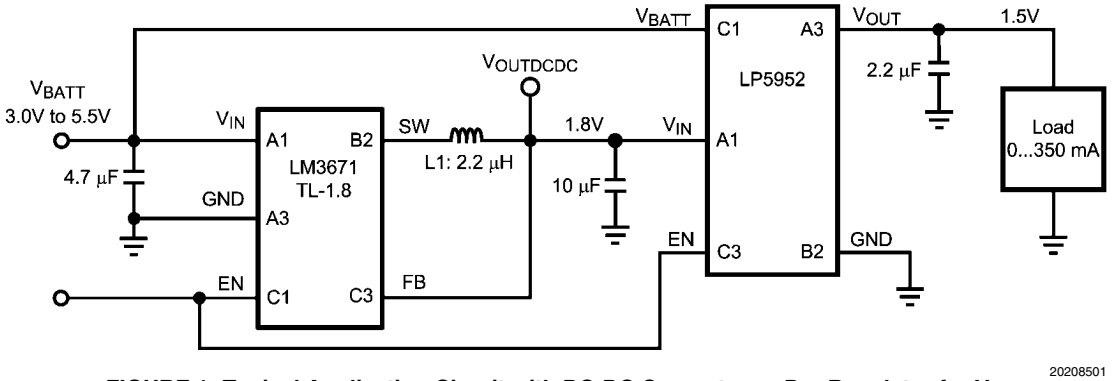

FIGURE 1: Typical Application Circuit with DC-DC Converter as Pre-Regulator for V_{IN}

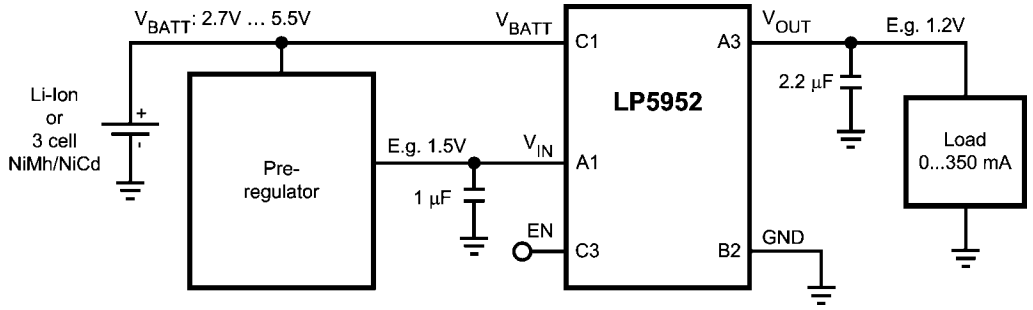

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FIGURE 2: Typical Application Circuit

Connection Diagrams

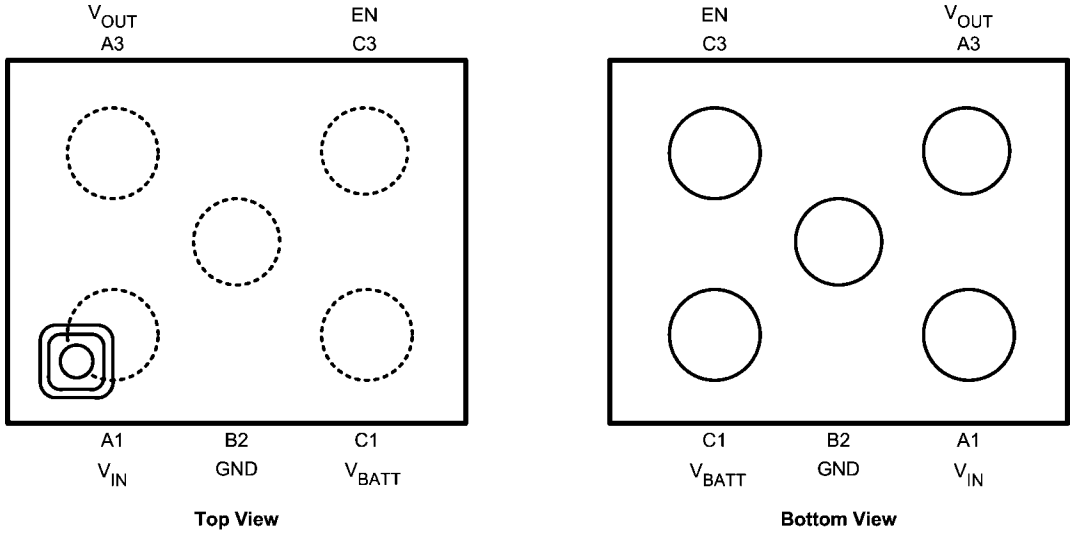

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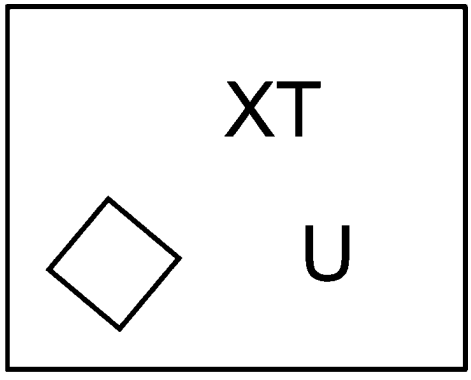
FIGURE 3: Connection Diagram 5-Bump Thin Micro SMD Package, Large Bump, 0.5mm Pitch
See NS Package Number TLA05



Package Mark - Top View

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FIGURE 4: Package Marking

Note: The actual physical placement of the package marking will vary from part to part. The package marking “X” designates the date code. “T” is a NSC internal code for die traceability. Both will vary considerably. “U” identifies the device (part number, option, etc.).

Pin Descriptions

Pin Number	Pin Name	Description
A1	V_{IN}	Power input voltage; input range: 0.7V to 4.5V, $V_{IN} \leq V_{BATT}$
A3	V_{OUT}	Regulated output voltage
B2	GND	Ground
C1	V_{BATT}	Bias input voltage; input range: 2.5V to 5.5V
C3	EN	Enable pin logic input: low = shutdown, high = active, normal operation. This pin should not be left floating. Tie to V_{BATT} if this function is not used.

Order Information

Output Voltage (V)	LP5952 Supplied as 250 Units, Tape and Reel, lead free	LP5952 Supplied as 3000 Units, Tape and Reel, lead free	Flow	Package Marking
0.7	LP5952TL-0.7	LP5952TLX-0.7	NOPB	4
1.2	LP5952TL-1.2	LP5952TLX-1.2	NOPB	7
1.3	LP5952TL-1.3	LP5952TLX-1.3	NOPB	U
1.4	LP5952TL-1.4	LP5952TLX-1.4	NOPB	A
1.5	LP5952TL-1.5	LP5952TLX-1.5	NOPB	T
1.6	LP5952TL-1.6	LP5952TLX-1.6	NOPB	B
1.8	LP5952TL-1.8	LP5952TLX-1.8	NOPB	8
2.0	LP5952TL-2.0	LP5952TLX-2.0	NOPB	5

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}, V_{BATT} pins: Voltage to GND, $V_{IN} \leq V_{BATT}$:	-0.2V to 6.0V
V_{BATT} pin to V_{IN} pin:	0.2V
EN pin: Voltage to GND:	-0.2V to 6.0V
Continuous Power Dissipation (Note 3):	Internally Limited
Junction Temperature (T_{J-MAX}):	150°C
Storage Temperature Range:	-65°C to + 150°C
Package Peak Reflow Temperature (Pb-free, 10-20 sec.)(Note 4):	260°C
ESD Rating(Note 5):	
Human Body Model:	2.0kV
Machine Model:	200V

Operating Ratings

Input Voltage Range V_{IN}	0.7V to 4.5V
Input Voltage Range V_{BATT}	2.5V to 5.5V
V_{EN} Input Voltage	0 to V_{BATT}
Recommended Load Current	0mA to 350mA
Junction Temperature (T_J) Range	-40°C to + 125°C
Ambient Temperature (T_A) Range (Note 6)	-40°C to + 85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), TLA05 package (Note 7)	95°C/W

ESD Caution Notice

National Semiconductor recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling techniques can result in damage.

Electrical Characteristics (Notes 2, 8, 11)

Typical values and limits appearing in standard typeface are for T_A = 25°C. Limits appearing in **boldface** type apply over the full operating temperature range: -40°C ≤ T_J ≤ +125°C. Unless otherwise noted, specifications apply to the typical application circuit with $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{BATT} = V_{OUT(NOM)} + 1.5V$ or 2.5V, whichever is higher, I_{OUT} = 1mA, C_{VIN} = 1.0µF, C_{OUT} = 2.2µF, $V_{EN} = V_{BATT}$.

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
$\Delta V_{OUT} / V_{OUT}$	Output Voltage Tolerance	$V_{IN} = V_{OUT(NOM)} + 0.3V$		-1.5 **-2.0**	1.5 **2.0**	% %
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation Error	$V_{IN} = V_{OUT(NOM)} + 0.3V$ to 4.5V, V_{BATT} = 4.5V	0.3		**1.0**	mV/V
$\Delta V_{OUT} / \Delta V_{BATT}$		$V_{BATT} = V_{OUT(NOM)} + 1.5V$ (≥ 2.5V) to 5.5V	0.5		**2.2**	
$\Delta V_{OUT} / \Delta mA$	Load Regulation Error	I_{OUT} = 1mA to 350mA	15		**30**	µV/mA
I_{SC}	Output Current (short circuit)	V_{OUT} = 0V, $V_{EN} = V_{IN} = V_{BATT} = V_{OUT(NOM)} + 1.5V$	500	**350**		mA
V_{DO_VBATT} (Note 10)	Output Voltage Dropout (Note 9)	I_{OUT} = 350mA, $V_{IN} = V_{OUT(NOM)} + 0.3V$	1.07		**1.5**	V
		I_{OUT} = 150mA, $V_{IN} = V_{OUT(NOM)} + 0.3V$	0.96		**1.3**	V
V_{DO_VIN}		I_{OUT} = 350mA, $V_{BATT} = V_{OUT(NOM)} + 1.5V$ or 2.5V	88		**200**	mV
E_N	Output Noise	10Hz to 100kHz	100			μV_{RMS}

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
PSRR	Power Supply Rejection Ratio	Sine modulated V_{BATT}				
		f = 10Hz	70			dB
		f = 100Hz	65			dB
		f = 1kHz	45			dB
		Sine modulated V_{IN}				
		f = 10Hz	80			dB
		f = 100Hz	90			dB
		f = 1kHz	95			dB
		f = 10kHz	85			dB
		f = 100kHz	64			dB

Quiescent Currents

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
I_{Q_VBATT}	Current into V_{BATT}	I_{LOAD} = 0...350mA	50		**100**	µA
I_{Q_VIN}	Current into V_{IN}	I_{LOAD} = 0	11		**28**	µA

Shutdown Currents

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
I_{Q_VBATT}	Current into V_{BATT}	V_{EN} = 0V	0.1		**1**	µA
I_{Q_VIN}	Current into V_{IN}	V_{EN} = 0V	0.1		**1**	µA

Enable Control Characteristics

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
I_{EN}	Maximum Input Current at V_{EN} Input		0.01		**1**	µA
V_{IL}	Low Input Threshold (shutdown)				**0.4**	V
V_{IH}	High Input Threshold (enable)			**1.0**		V

Thermal Protection

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
T_{SHDN}	Thermal-Shutdown Temperature		165			°C
ΔT_{SHDN}	Thermal-Shutdown Hysteresis		20			°C

Transient Characteristics

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Dynamic Line Transient Response V_{IN}	$V_{IN} = V_{OUT(NOM)} + 0.3V$ to $V_{OUT(NOM)} + 0.9V$; tr, tf = 10µs	±1			mV
ΔV_{OUT}	Dynamic Line Transient Response V_{BATT}	$V_{BATT} = V_{OUT(NOM)} + 1.5V$ to $V_{OUT(NOM)} + 2.1V$; tr, tf = 10µs	±15			mV
ΔV_{OUT}	Dynamic Load Transient Response	Pulsed load 0 ...300mA, di/dt = 300mA/1µs	±15			mV
$T_{STARTUP}$	Startup Time	EN to 0.95 * V_{OUT}	70		**150**	µs

Input and Output Capacitors, Recommended Specification

Symbol	Parameter	Conditions	Nom	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitance	Capacitance (Note 12)	2.2	1.5	10	µF
		ESR		3	300	mΩ
C_{VIN}	Input Capacitance at V_{IN}	Capacitance (Note 12), not needed in typ post regulation application, see FIGURE 1	1	0.47		µF
		ESR		3	300	mΩ

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typ.) and disengages at T_J = 145°C (typ.).

Note 4: For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1112: Micro SMD Wafer Level Chip Scale Package (AN-1112).

Note 5: The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. (MIL-STD-883 3015.7)

Note 6: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 7: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special attention must be paid to thermal dissipation issues in board design.

Note 8: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical (Typ) numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{BATT} = V_{OUT(NOM)} + 1.5V$ or 2.5V, whichever is higher, T_A = 25° C.

Note 9: Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100mV below the nominal output voltage.

Note 10: This specification does not apply for output voltages below 1.0V (as $V_{BATTMIN}$ = 2.5V).

Note 11: $V_{OUT(NOM)}$ is the stated output voltage option

Note 12: The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. The shown minimum limit represents real minimum capacitance, including all tolerances and must be maintained over temperature and dc bias voltage (See capacitor section in Applications Hints)

Block Diagram

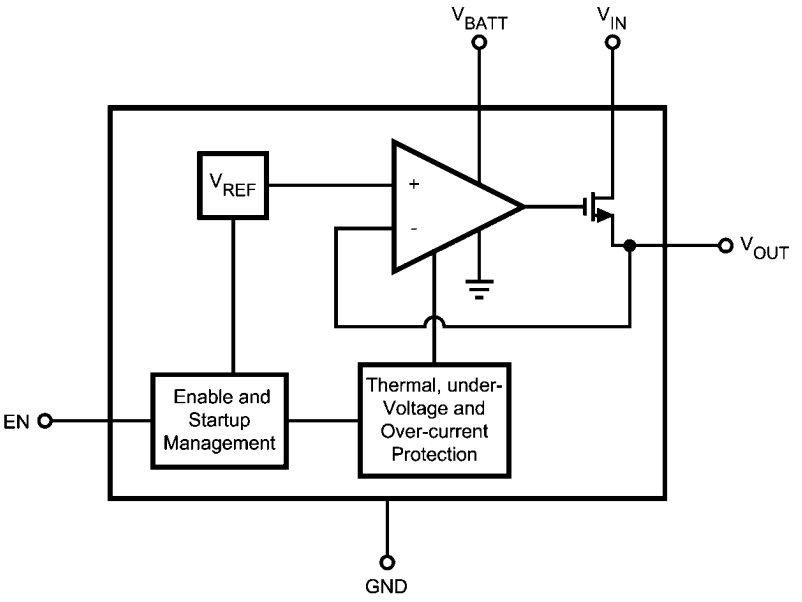
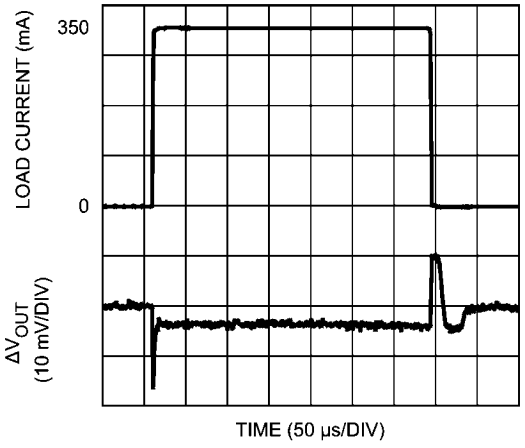


FIGURE 5: Block Diagram

Typical Performance Characteristics

Unless otherwise specified, C_{IN} = 1.0µF ceramic, C_{OUT} = 2.2µF ceramic, $V_{IN} = V_{OUT(NOM)} + 1V$, $V_{BATT} = V_{OUT(NOM)} + 1.5V$, T_A = 25°C, Enable pin is tied to V_{BATT}.

Load Transient Response, 0.7V Option



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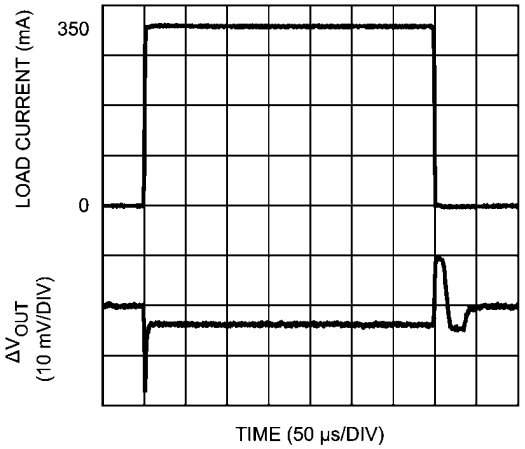
Load Transient Response, 1.5V Option



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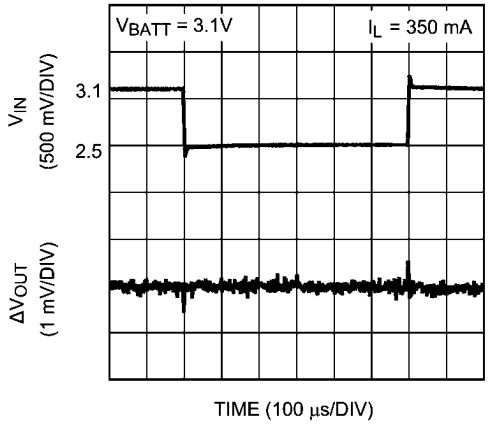
Line Transient Response V_{IN}, 1.5V Option



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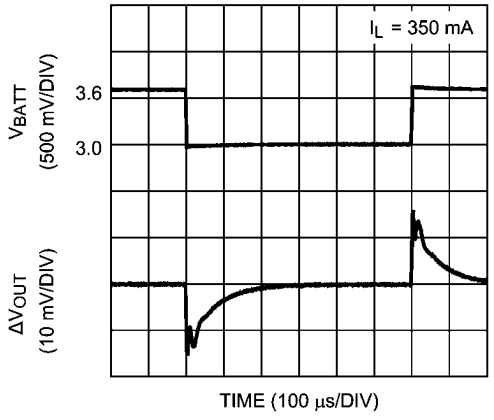
Line Transient Response V_{BATT}, 1.5V Option



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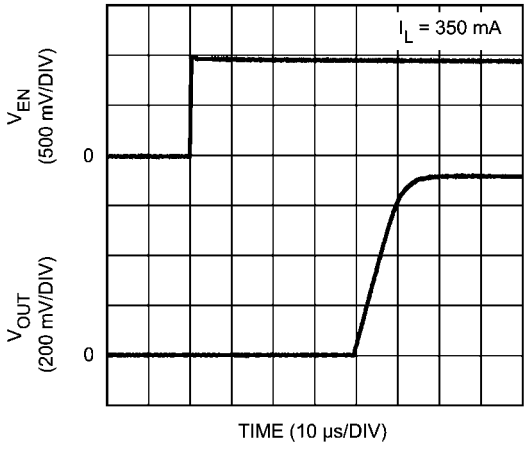
Enable Start-up Time, 0.7V Option



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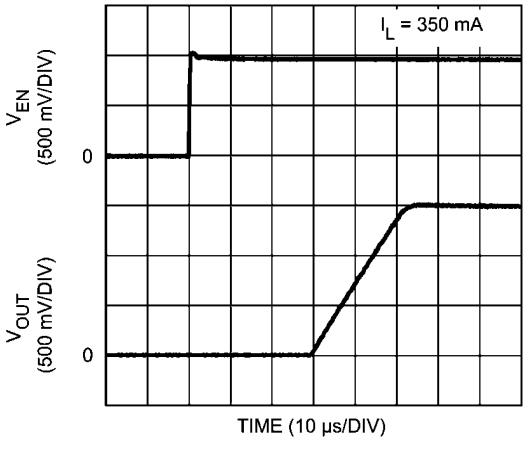
Enable Start-up Time, 1.5V Option



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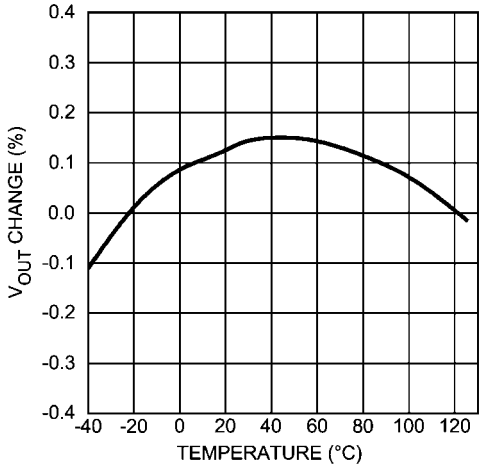
Output Voltage Change vs Temperature



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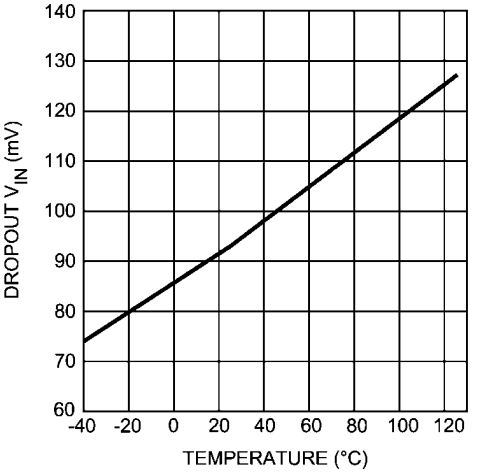
Dropout V_{IN} vs Temperature, I_{LOAD} = 350mA



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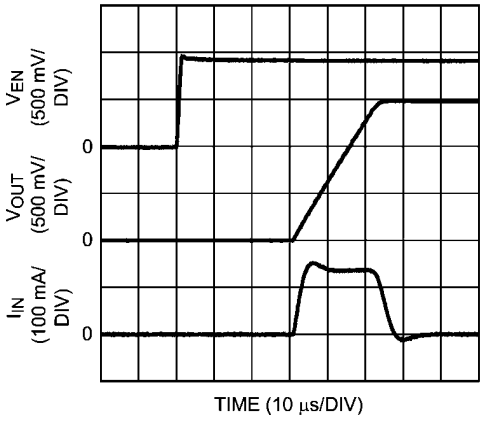
Inrush Current V_{IN}, 1.5V Option



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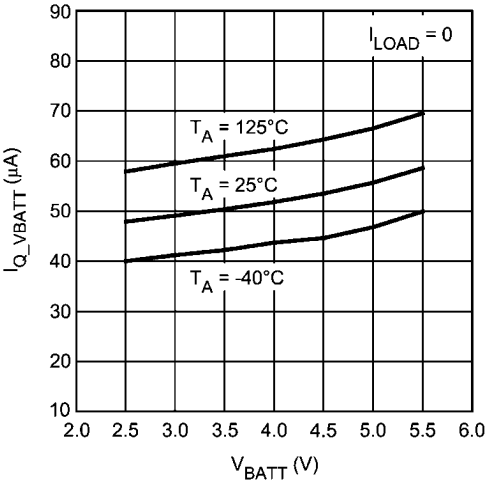
Quiescent Current I_{Q_VBATT} vs V_{BATT}



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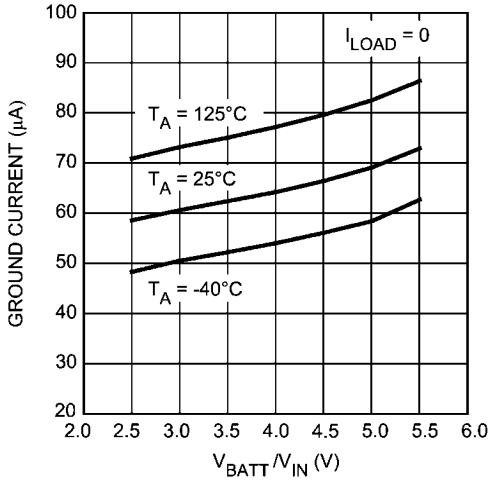
Ground Current vs V_{BATT} / V_{IN}



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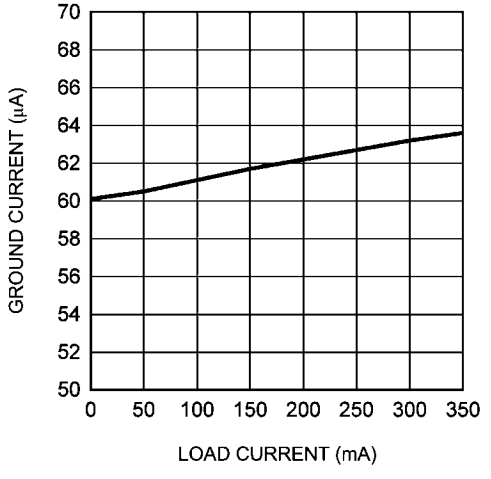
Ground Current vs Load Current



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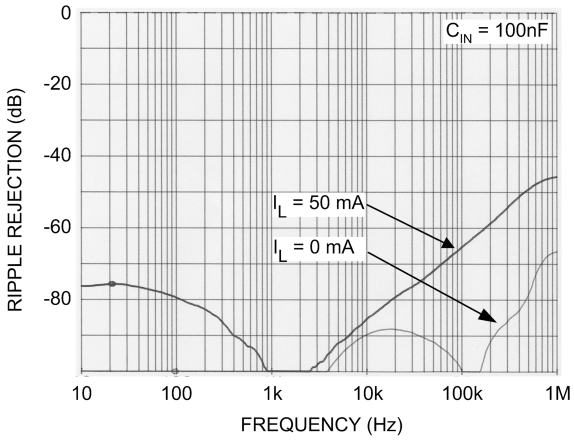
Power Supply Rejection Ratio V_{IN}, 1.5V Option



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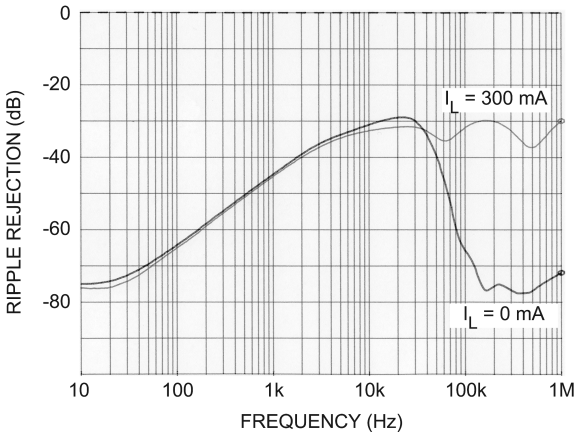
Power Supply Rejection Ratio V_{BATT}, 1.5V Option



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Application Hints

DUAL RAIL SUPPLY

The LP5952 requires two different supply voltages:

•V_{IN}, the power input voltage, is regulated to the fixed output voltage

•V_{BATT}, the bias input voltage, supplies internal circuitry.

It's important that V_{IN} does not exceed V_{BATT} at any time. If the device is used in the typical post regulation application as shown in FIGURE 1, the sequencing of the two power supplies is not an issue as V_{BATT} supplies both, the DC-DC regulator and the LP5952. The output voltage of the DC-DC regulator will take some time to rise up and supply V_{IN} of LP5952. In this application V_{IN} will always ramp up more slowly than V_{BATT}.

In case V_{IN} is shorted to V_{BATT}, the voltages at the two supply pins will ramp up simultaneously causing no problem.

Only in applications with two independent supplies connected to the LP5952 special care must be taken to guarantee that V_{IN} is always ≤ V_{BATT}.

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in the electrical specification section, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$$

With a θ_{JA} = 95°C/W, the device in the 5 bump micro SMD package returns a value of 1053mW with a maximum junction temperature of 125°C at T_A of 25°C or 421mW at T_A of 85°C.

The actual power dissipation across the device can be estimated by the following equation:

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT}$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application. As an example, to keep full load current capability of 350mA for a 1.5V output voltage option at a high ambient temperature of 85°C, V_{IN} has to be kept ≤ 2.7V:

$V_{IN} ≤ P_D / I_{OUT} + V_{OUT}$ = 421mW / 350mA + 1.5V = 2.7V.

The figure below shows the output current derating due to these considerations:

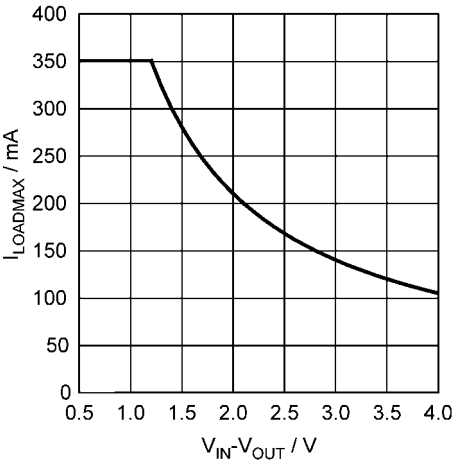

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FIGURE 6: Maximum Load Current vs V_{IN} - V_{OUT}, T_A = 85°C, V_{OUT} = 1.5V, θ_{JA} = 95°C/W

The typical contribution of the bias input voltage supply V_{BATT} to the power dissipation can be neglected:

$P_{D\_VBATT} = V_{BATT} * I_{QVBATT}$ = 5.5V * 50µA = 0.275mW typical.

EXTERNAL CAPACITORS

As is common with most regulators, the LP5952 requires external capacitors to ensure stable operation. The LP5952 is specifically designed for portable applications requiring minimum board space and the smallest size components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

If the LP5952 is used stand alone, an input capacitor at V_{IN} is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP5952 power voltage input pin V_{IN} and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the V_{IN} pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

A capacitor at V_{BATT} is not required if the distance to the supply does not exceed 5cm.

If the device is used in the typical application as post regulator after a DC-DC regulator, no input capacitors are required at all as the capacitors of the DC-DC regulator (C_{IN} and C_{OUT}) are sufficient if both components are mounted close to each other and a proper GND plane is used. If the distance between the output capacitor of the DC-DC regulator and the V_{IN} pin of the LP5952 is larger than 5cm, it's recommended to add the mentioned input capacitor at V_{IN}.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

The ESR (Equivalent Series Resistance) of the input capacitor should be in the range of 3mΩ to 300mΩ. The tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≥ 470nF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP5952 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X7R, Z5U, or Y5V) in the 2.2µF range (up to 10µF) and with an ESR between 3mΩ to 300mΩ is suitable as C_{OUT} in the LP5952 application circuit.

This capacitor must be located a distance of not more than 1cm from the V_{OUT} pin and returned to a clean analogue ground.

It is also possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

CAPACITOR CHARACTERISTICS

The LP5952 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 1µF to 4.7µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1µF ceramic capacitor is in the range of 3mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP5952.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. The example shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.47/1.5µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

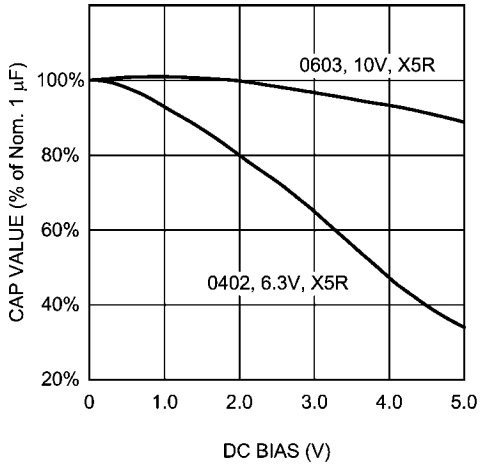

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FIGURE 7: Graph Showing A Typical Variation In Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

NO-LOAD STABILITY

The LP5952 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

ENABLE OPERATION

The LP5952 may be switched ON or OFF by a logic input at the Enable pin, V_{EN}. A logic high at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 0.1µA.

If the application does not require the Enable switching feature, the V_{EN} pin should be tied to V_{BATT} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under Enable Control Characteristics, V_{IL} and V_{IH}.

FAST TURN ON

Fast turn-on is guaranteed by an optimized architecture allowing a fast ramp of the output voltage to reach the target voltage while the inrush current is controlled low at 120mA typical (for a C_{OUT} of 2.2µF).

SHORT-CIRCUIT PROTECTION

The LP5952 is short circuit protected and in the event of a peak over-current condition, the output current through the NFET pass device will be limited.

If the over-current condition exists for a longer time, the average power dissipation will increase depending on the input to output voltage difference until the thermal shutdown circuitry will turn off the NFET.

Please refer to the section on thermal information for power dissipation calculations.

THERMAL-OVERLOAD PROTECTION

Thermal-Overload Protection limits the total power dissipation in the LP5952. When the junction temperature exceeds T_J = 165°C typ., the shutdown logic is triggered and the NFET is turned off, allowing the device to cool down. After the junction temperature dropped by 20°C (temperature hysteresis) typical, the NFET is activated again. This results in a pulsed output voltage during continuous thermal-overload conditions.

The Thermal-Overload Protection is designed to protect the LP5952 in the event of a fault condition. For normal, continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C (see Absolute Maximum Ratings).

REVERSE CURRENT PATH

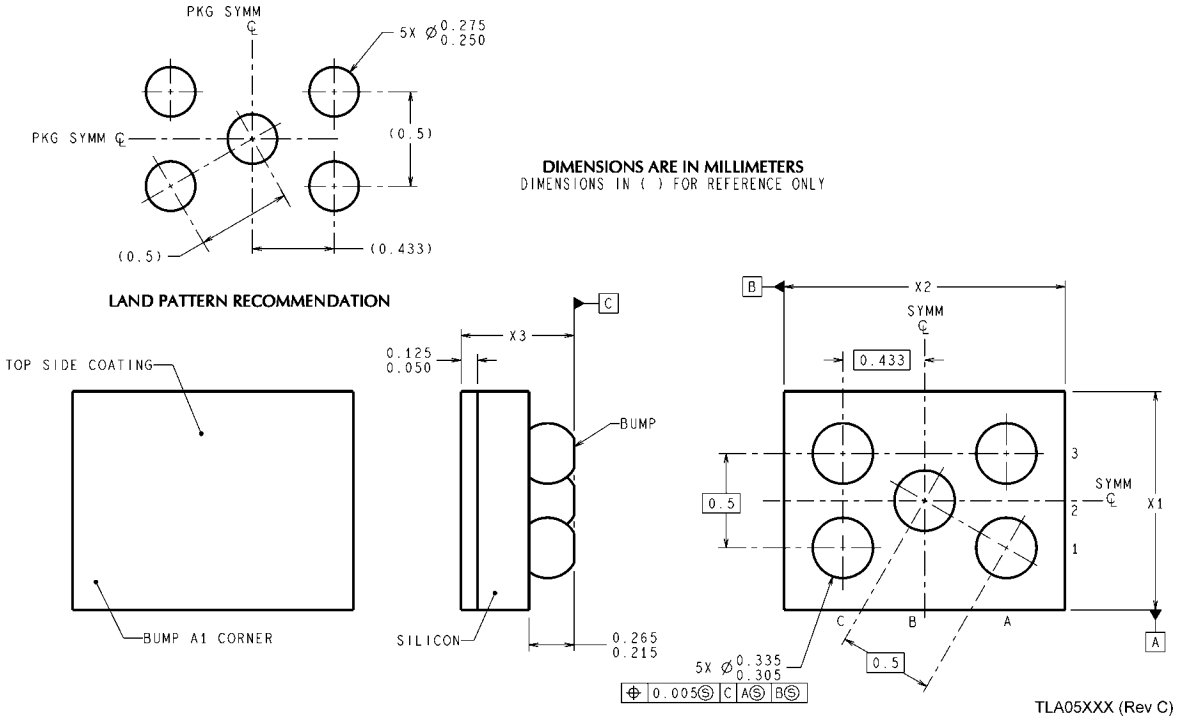
The internal NFET pass device in LP5952 has an inherent parasitic body diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 50mA. For currents above this limit an external Schottky diode must be connected from V_{OUT} to V_{IN} (cathode on V_{IN}, anode on V_{OUT}).

EVALUATION BOARDS

For availability of evaluation boards please refer to the Product Folder of LP5952 at www.national.com.

For information regarding evaluation boards, please refer to Application Note: AN-1531.

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number TLA05Z1A
X1 = 955 µm ±30µm
X2 = 1335µm ±30µm
X3 = 600µm ±75µm
5-Bump Thin Micro SMD Package, Large Bump

For most accurate revision please refer to www.national.com/packaging/parts/

Notes

Notes

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