FUNCTIONAL DESCRIPTION

The XRK4993 is a 3.3V High-Speed Low-Voltage Programmable Skew Clock Buffer. It is intended for high-performance computer systems and offers user selectable control over system clock functions to optimize timing. Eight ouputs, arranged in four banks, can each drive 75Ω terminated transmission lines while delivering minimal and specified output skews and full-swing Low Voltage TTL logic levels.

Banks A, B, C (two outputs per bank) can be individually selected for one of nine delay or function configurations through two dedicated three-level inputs. These outputs are able to lead or lag the CLKIN input reference clock by up to 6 time units from their nominal "zero" skew position. The integrated PLL allows external load and transmission line delay effects to be canceled achieving zero delay capability. Combining the zero delay capability with the selectable output skew functions, output-to-output delays of up to ±12 time units can be created.

The XRK4993's divide functions (divide-by-two and divide-by-four) allow distribution of a low-frequency clock that can be multiplied by two or four at the clock destination. This feature facilitates clock distribution while allowing maximum system clock flexibility.

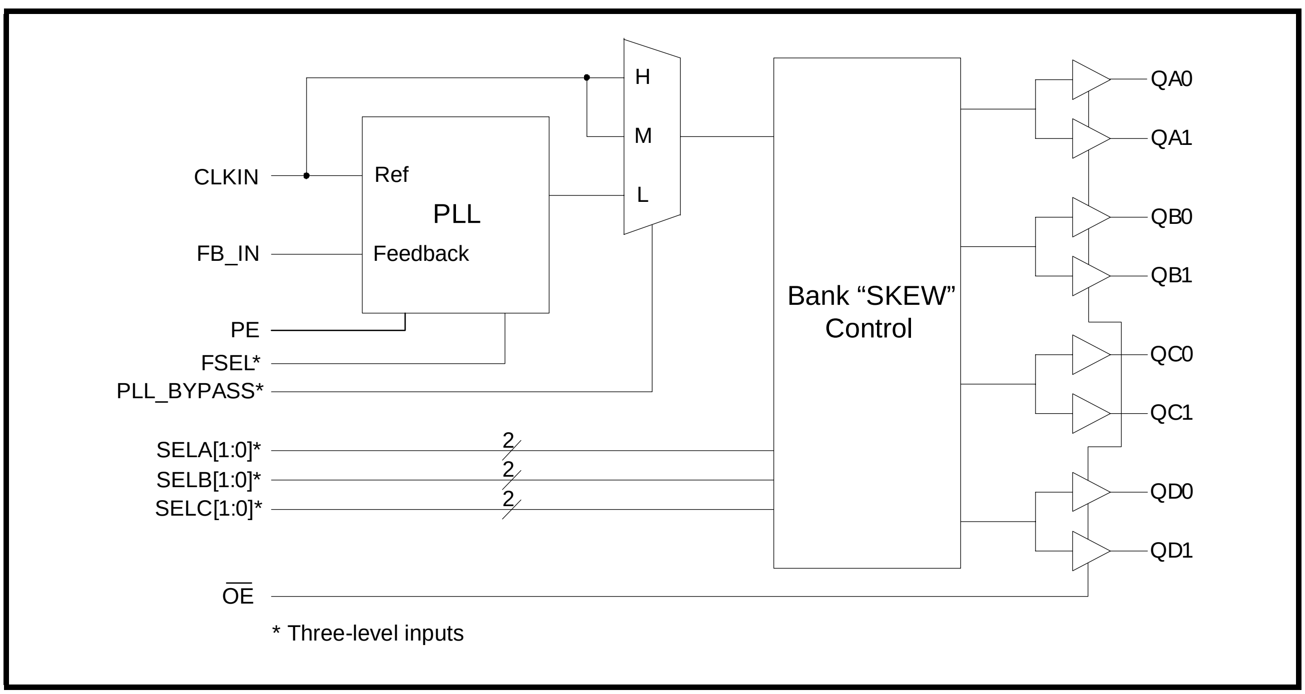
When the $\overline{OE}$ pin is held low, all the outputs are synchronously enabled. However, if $\overline{OE}$ is held high, all the outputs except QC0 and QC1 are synchronously disabled.

When PE is held high, all the outputs are synchronized with the positive edge of the CLKIN clock input. When PE is held low, all the outputs are synchronized with the negative edge of CLKIN. The device has LVTTL outputs with 12mA balanced drive.

FEATURES

- 3 pairs of programmable skew outputs
- Low skew: 200ps same pair, 250ps all outputs
- Selectable positive or negative edge synchronization: Excellent for DSP applications
- Synchronous output enable
- Output frequency: 3.75MHz to 85MHz
- 2x, 4x, 1/2, and 1/4 output frequencies
- 3 skew grades
- 3-level inputs for skew and PLL range control
- PLL bypass mode
- External feedback, internal loop filter
- 12mA balanced drive outputs
- Available in 28 pin QSOP package
- Jitter < 200 ps peak-to-peak
- CLKIN input is 5V tolerant

FIGURE 1. BLOCK DIAGRAM OF THE XRK4993



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	ACCURACY	OPERATING TEMPERATURE RANGE
XRK4993IR-2	250 ps	-40°C to +85°C
XRK4993CR-2	250 ps	0°C to +70°C
XRK4993IR-5	500 ps	-40°C to +85°C
XRK4993CR-5	500 ps	0°C to +70°C
XRK4993IR-7	750 ps	-40°C to +85°C
XRK4993CR-7	750 ps	0°C to +70°C

FIGURE 2. PIN OUT OF THE XRK4993

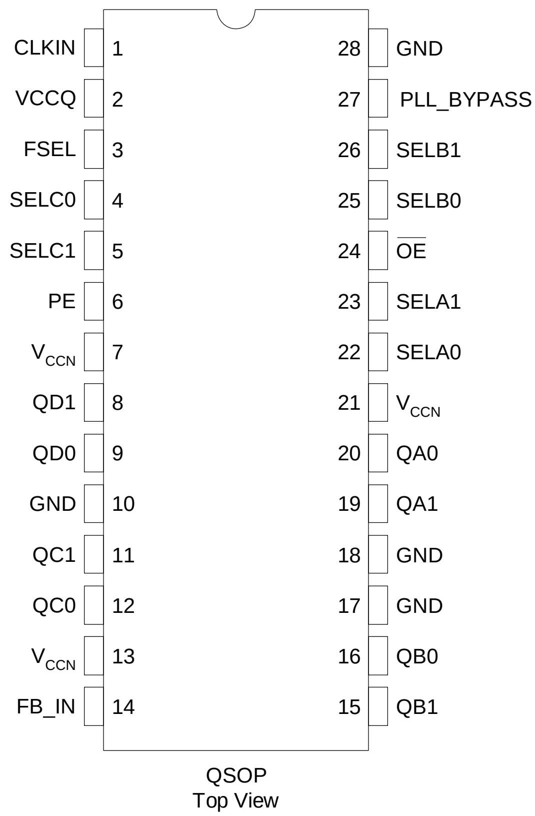


TABLE 1: FREQUENCY RANGE SELECT AND t_U CALCULATION [1]

FSEL[2,3]	f_{NOM} (MHz) MIN	f_{NOM} (MHz) MAX	$t_U = 1 / (f_{NOM} \times N)$ WHERE N =	APPROXIMATE FREQUENCY (MHZ) AT WHICH t_U = 1.0ns
LOW	15	35	44	22.7
MID	25	60	26	38.5
HIGH	40	85	16	62.5

PIN DESCRIPTIONS

PIN NAME	PIN #	TYPE	DESCRIPTION
CLKIN	1	Input	Reference Clock Input
FB_IN	14	Input	Feedback Input
PLL_BYPASS	27	Three-level Input	When MID or HIGH, disables PLL (see Special Functions). CLKIN goes to all outputs. Skew Selections (see Control Summary Table) remain in effect. Set LOW for normal operations.
$\overline{OE}$	24	Input	Synchronous Output Enable. When HIGH, it stops clock outputs (except QC[1:0]). QC[1:0] may be used as the feedback signal to maintain phase lock. Set $\overline{OE}$ LOW for normal operation.
PE	6	Input	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the falling/rising edge of the reference clock.
SELA0 SELA1	22 23	Three-level Input	3-level inputs for selecting 1 of 9 skew taps or frequency functions.
SELB0 SELB1	25 26	Three-level Input	
SELC0 SELC1	4 5	Three-level Input	
FSEL	3	Three-level Input	Selects appropriate oscillator circuit based on anticipated frequency range. (See PLL Programmable Skew Range.)
QA0 QA1	20 19	Output	Three output banks of two outputs with programmable skew (QA[1:0], QB[1:0], QC[1:0]). QD[1:0] outputs have fixed zero skew outputs.
QB0 QB1	16 15	Output	
QC0 QC1	12 11	Output	
QD0 QD1	9 8	Output	
V_{CCN}	7 13 21	PWR	Power supply for output buffers.
V_{CCQ}	2	PWR	Power supply for phase locked loop and other internal circuitry.
GND	10 17 18 28	PWR	Ground.

SKEW SELECT CONTROL

The skew select control consists of four independent sections. Each bank has two low-skew, high-fanout drivers (Qx0, Qx1), and two corresponding three-level function select (SELx0, SELx1) inputs. The nine possible output states for each bank as shown in Table 2 as determined by each bank's select inputs. All timing measurements are made with respect to the CLKIN input assuming that the output connected to the FB_IN input configured for 0 t_U operation.

TABLE 2: PROGRAMMABLE SKEW CONFIGURATIONS [1]

FUNCTION SELECTS		OUTPUT FUNCTIONS	
SELx1	**SELx0**	**QA[1:0], QB[1:0]**	**QC[1:0]**
LOW	LOW	$-4t_U$	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4

NOTES:

1. *For all three-level (three-state) inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.*
2. *The level to be set on FSEL is determined by the "normal" operating frequency (f_{NOM}) of the PLL. Nominal frequency (f_{NOM}) always appears at QA0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the CLKIN and FB_IN inputs will be f_{NOM} when the output connected to FB_IN is undivided. The frequency of the CLKIN and FB_IN inputs will be $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication.*
3. *When the FSEL pin is selected HIGH, the CLKIN input must not transition upon power-up until V_{CC} has reached 2.8V.*
4. *QD[1:0] fixed at zero skew.*

BYPASS MODE

BYPASS mode allows the chip to be used in applications where the relative timing between outputs is maintained but the system clocking is interrupted or at a much lower frequency. An example might be "single-stepping" the system for diagnostics.

The PLL_BYPASS pin is normally held at Ground (Low). To accommodate low frequency (below the PLL lock range) or infrequent pulses, the PLL_BYPASS, in conjunction with the FSEL pin (see Table 3) can be used to by-pass the PLL and generate an output sequence for the CLKIN signal. Relative timing as set by the SEL(x)1:0 for the various banks will be maintained. The relative timing includes plus and minus n tu and divide-by (2 or 4) settings. There will be a propagation delay as shown in Table 3. A tu will be approximately 2.5nS with PLL_BYPASS at Mid voltage and 0.4nS in the High state.

In the PLL_BYPASS mode the PE input can be used to invert the outputs. Thus, for a 20% (High) duty cycle input, all outputs will retain the 20% high condition with PE High. For PE Low, however, they will be 80% High. PE does not effect the duty cycle of the divided outputs.

TABLE 3: TYPICAL PROPAGATION DELAY WITH ZERO SKEW SETTING

PLL_BYPASS INPUT	FSEL INPUT	TOTAL PROPAGATION DELAY
Mid	Low or Mid	52nS
	High	29nS
High	Low or Mid	12nS
	High	10nS

SPECIAL FUNCTIONS

The following special functions have been implemented in the chip.

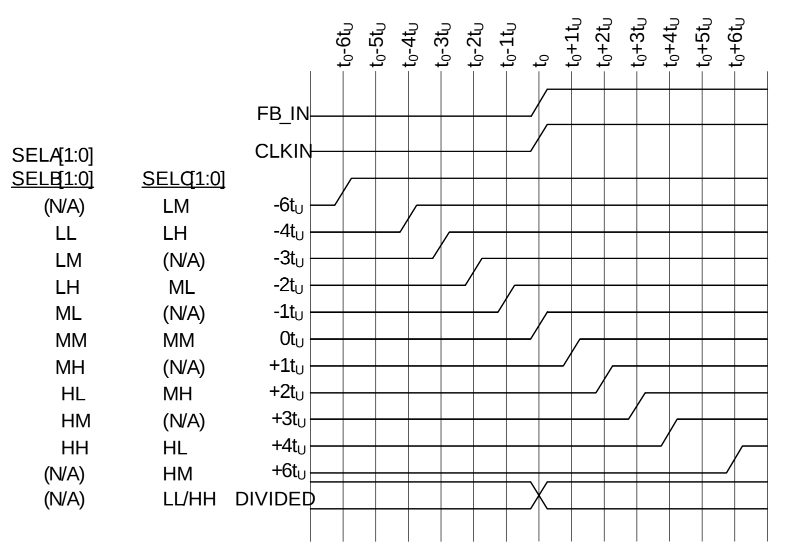
PE pin:

- In Normal operation, PE controls the "alignment" edge of the CLKIN and the FB-IN signals. (All other output signals are aligned to the Feedback). PE=Low, aligns the FB_IN faliing edge to the CLKIN falling edge. PE=High, aligns rising edges.
- In the "disabled output mode (see below), the disabled state is forced to the opposite state of PE. This keeps the off condition in a low-noise state.
- In PLL_BYPASS mode, PE controls the duty cycle (inversion) of the outputs (see PLL_BYPASS mode above).

$\overline{OE}$ pin:

- In Normal mode, $\overline{OE}$ is used to disable all outputs except QC[1,0]. These are maintained to provide PLL Feedback to keep frequency lock. $\overline{OE}$ is kept low to enable the outputs and High to disable them. This is a synchronized operation to prevent "partial" clocks When $\overline{OE}$ goes high, the outputs will go to their disabled level at the end of the next active clock cycle. The level is determined by the state of PE. If PE is high, the output will go low at the end of the cycle and remain there until $\overline{OE}$ return to a low state. If PE is low, at the end of the next clock high state it will continue to remain high until $\overline{OE}$ returns low.
- If $\overline{OE}$ is high when PLL_BYPASS is at the Mid level, the PLL is enabled to provide an individual bank output control. In this mode, taking both SEL(x)1 & 0 to the Low state will disable that bank's outputs.

FIGURE 3. TYPICAL OUTPUTS WITH FB_IN CONNECTED TO A ZERO-SKEW OUTPUT



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
Output Current into Outputs (LOW)	64 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current.	>200 mA

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	VCC
Industrial	-40°C to +85°C	3.3 $\pm$ 10%
Commercial	0°C to +70°C	3.3 $\pm$ 10%

ELECTRICAL CHARACTERISTICS *OVER THE 3.3V $\pm$ 10% OPERATING RANGE*

SYMBOL	DESCRIPTION	MIN	MAX	UNIT	CONDITION
V_{OH}	Output HIGH Voltage	2.4		V	V_{CC} = Min., I_{OH} = -18mA
V_{OL}	Output LOW Voltage		0.45	V	V_{CC} = Min., I_{OL} = 35mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	V	CLKIN, FB_IN, PE, and $\overline{OE}$
V_{IL}	Input LOW Voltage	-0.5	0.8	V	
V_{IHH}	Three-Level Input HIGH Voltage (PLL_Bypass, FSEL, SELx[1:0]) [5]	0.87*V_{CC}	V_{CC}	V	Min. $\leq V_{CC} \leq$ Max.
V_{IMM}	Three-Level Input MID Voltage (PLL_Bypass, FSEL, SELx[1:0]) [5]	0.47*V_{CC}	0.53 * V_{CC}	V	Min. $\leq V_{CC} \leq$ Max.
V_{ILL}	Three-Level Input LOW Voltage (PLL_Bypass, FSEL, SELx[1:0]) [5]	0.0	0.13 * V_{CC}	V	Min. $\leq V_{CC} \leq$ Max.
I_{IH}	Input HIGH Leakage Current (CLKIN and FB_IN inputs only)		20	µA	V_{CC} = Max., V_{IN} = Max.
I_{IL}	Input LOW Leakage Current (CLKIN and FB_IN inputs only)	-20		µA	V_{CC} = Max., V_{IN} = 0.4V
I_{IHH}	Input HIGH Current (PLL_Bypass, FSEL, SELx[1:0])		400	µA	$V_{IN} = V_{CC}$
I_{IMM}	Input MID Current (PLL_Bypass, FSEL, SELx[1:0])	-200	200	µA	$V_{IN} = V_{CC}/2$
I_{ILL}	Input LOW Current PLL_Bypass, FSEL, SELx[1:0]		-400	µA	V_{IN} = GND

ELECTRICAL CHARACTERISTICS *OVER THE 3.3V ± 10% OPERATING RANGE*

SYMBOL	DESCRIPTION		MIN	MAX	UNIT	CONDITION
I_{OS}	Short Circuit Current [6]			-200	mA	V_{CC} = Max, V_{OUT} = GND (25°C only)
I_{CCQ}	Operating Current Used by Internal Circuitry	Com'l		95	mA	V_{CCN} = V_{CCQ} = Max., All Inputs Selects Open
		Ind		100		
I_{CCN}	Output Buffer Current per Output Pair			19	mA	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Inputs Selects Open, f_{MAX}
PD	Power Dissipation per Output Pair			104	mW	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}

CAPACITANCE[7]

SYMBOL	DESCRIPTION	MAX.	UNIT	CONDITION
C_{IN}	Input Capacitance	10	pF	T_A = 25°C, f=1MHz, V_{CC}=3.3V

NOTES:

5. *These inputs are normally wired to V_{CC}, GND or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an addtional t_{LOCK} time before all data sheet limits are achieved.*
6. *XRK4993 should be tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.*
7. *Applies to CLKIN and FB_IN inputs only.*

FIGURE 4. AC TEST LOAD

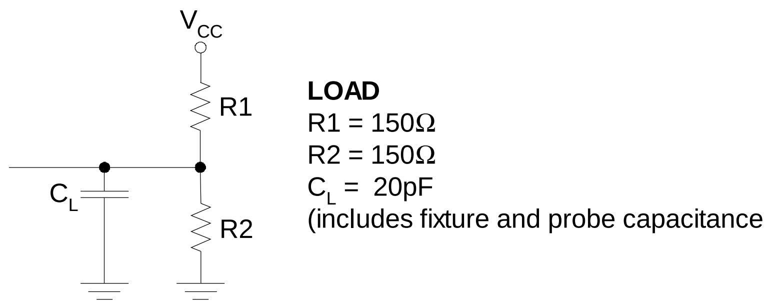
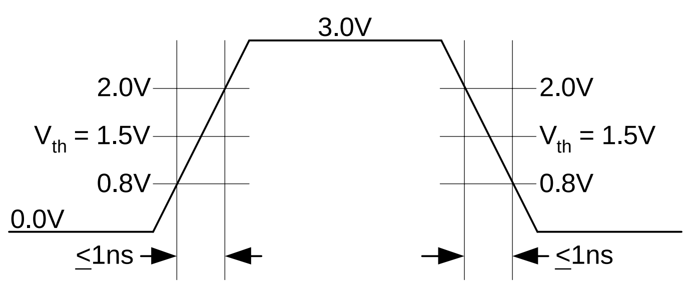


FIGURE 5. INPUT/OUTPUT TEST WAVEFORM



SWITCHING CHARACTERISTICS OVER THE OPERATING RANGE [2,8]

SYMBOL	DESCRIPTION		MIN	MAX	UNIT
f_{NOM}	Operating Clock Frequency in MHz	FSEL = LOW [1, 2]	15	35	MHz
		FSEL = MID [1, 2]	25	60	
		FSEL = HIGH [1, 2, 3]	40	85	

SWITCHING CHARACTERISTICS *OVER THE 3.3V ± 10% OPERATING RANGE [2,8]*

SYMBOL	DESCRIPTION		XRK4993-2			XRK4993-5			XRK4993-7			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{RPWH}	CLKIN Pulse Width HIGH		4			4			4			ns
t_{RPWL}	CLKIN Pulse Width LOW		4			4			4			ns
t_u	Programmable Skew Unit		See Table 1									
t_{SKEWPR}	Zero Output Matched-Pair Skew (Qx[1:0]) [10, 11]			0.05	0.2		0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs) [10, 12]			0.1	0.25		0.25	0.5		0.3	0.75	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[10, 13]			0.25	0.5		0.6	0.7		0.6	1	ns
t_{SKEW2}	Output Skew (Rise-Fall) [10, 13]			0.3	1		0.5	1		1	1.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) [10, 13]			0.25	0.5		0.5	0.7		0.7	1.2	ns
t_{SKEW4}	Output Skew (Nominal-Divided) [10, 13]			0.5	0.9		0.5	1		1.2	1.7	ns
t_{DEV}	Device-to-Device Skew [9, 14]				0.75			1.25			1.65	ns
t_{PD}	Propagation Delay, CLKIN Rise to FB_IN Rise		-0.25	0	0.25	-0.5	0	0.5	-0.7	0	0.7	ns
t_{ODCV}	Output Duty Cycle Variation [15]		-1	0	1	-1	0	1	-1.2	0	1.2	ns
t_{PWH}	Output HIGH Time Deviation from 50% [16]				2			2.5			3	ns
t_{PWL}	Output LOW Time Deviation from 50% [16]				1.5			3			3.5	ns
t_{ORISE}	Output Rise Time [16, 17]		0.15	1	1.2	0.15	1	1.5	0.15	1.5	2.5	ns
t_{OFALL}	Output Fall Time [16, 17]		0.15	1	1.2	0.15	1	1.5	0.15	1.5	2.5	ns
t_{LOCK}	PLL Lock Time [18]				0.5			0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS [9]			25			25			25	ps
		Peak-to-Peak [9]			200			200			200	

NOTES:

8. *Test measurement levels for the XRK4993 are TTL levels (1.5V to 1.5V). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.*
9. *Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.*
10. *SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 20pF and terminated with 75Ω to $V_{CC}/2$ (XRK4993).*

11. *t_{SKEWPR} is defined as the skew between a pair of outputs (Qx0 and Qx1) when all eight outputs are selected for $0t_U$.*
12. *t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided, but not shifted.*
13. *There are two classes of outputs: Nominal (multiple of t_U delay) and Divided (QC[1:0] or Divide-by-4 mode).*
14. *t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, etc.)*
15. *t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.*
16. *Specified with outputs loaded with 20pF for the XRK4993 devices. Devices are terminated through 75Ω to $V_{CC}/2$. t_{PWH} is measured at 2.0V. t_{PWL} is measured at 0.8V.*
17. *t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V.*
18. *t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at CLKIN or FB_IN until t_{PD} is within specified limits*

FIGURE 6. AC TIMING DIAGRAM (SHOWN WITH PE=HIGH)

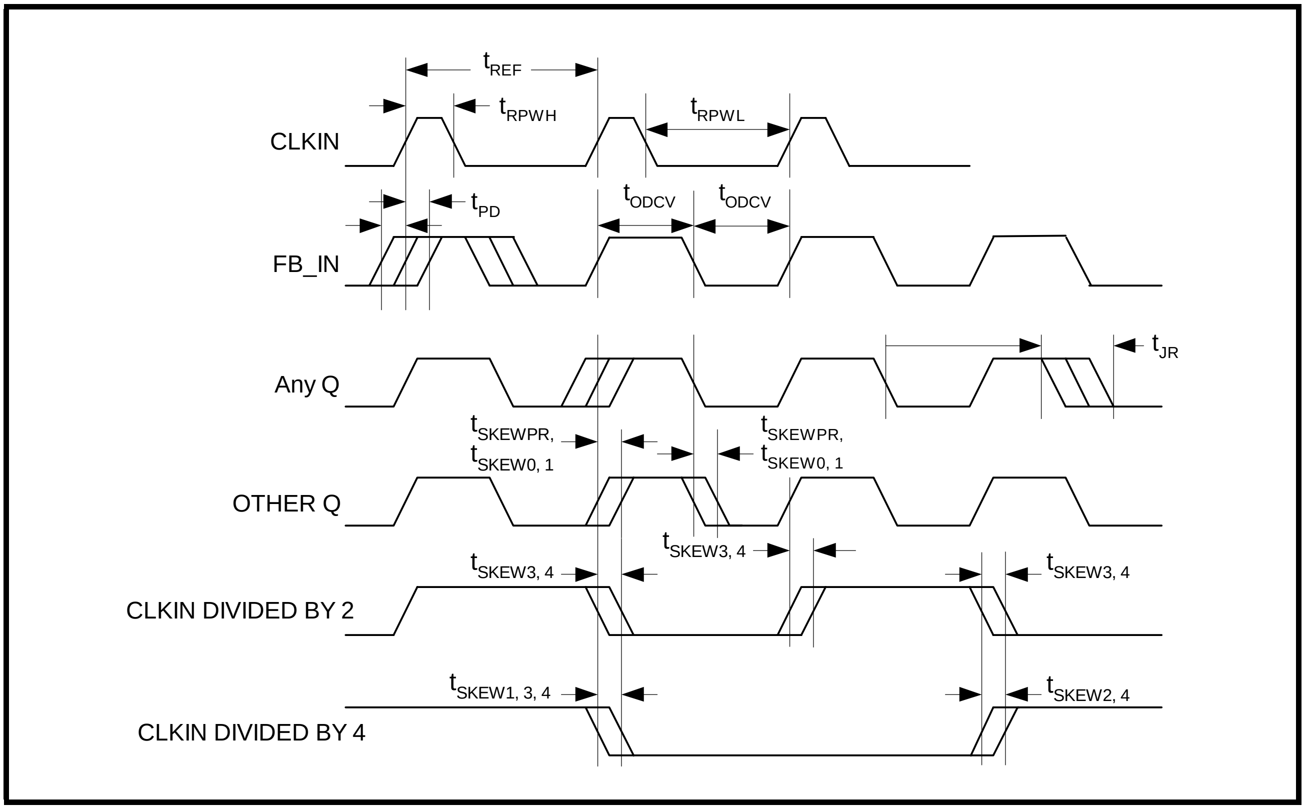
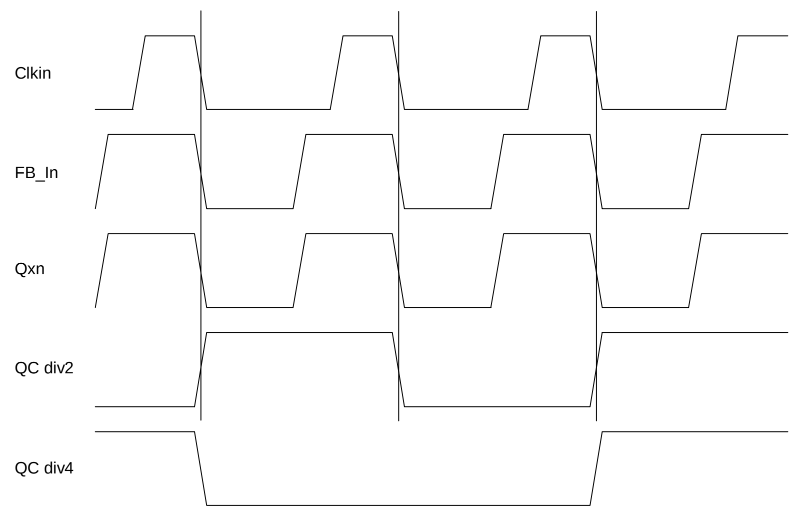


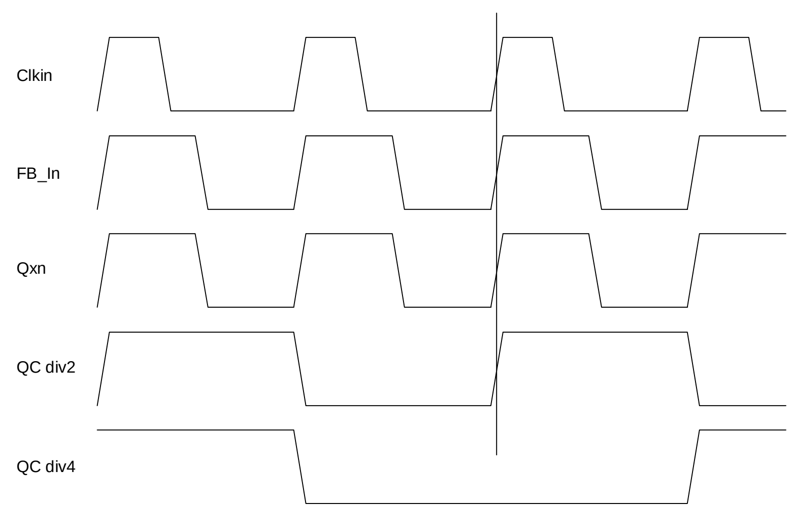
FIGURE 7. TIMING DIAGRAM PE=LOW



PE = LOW TIMING:

All output changes occur on the falling edge of the Clkin reference signal. Programmable skews are made relative to this edge.

FIGURE 8. TIMING DIAGRAM PE=HIGH

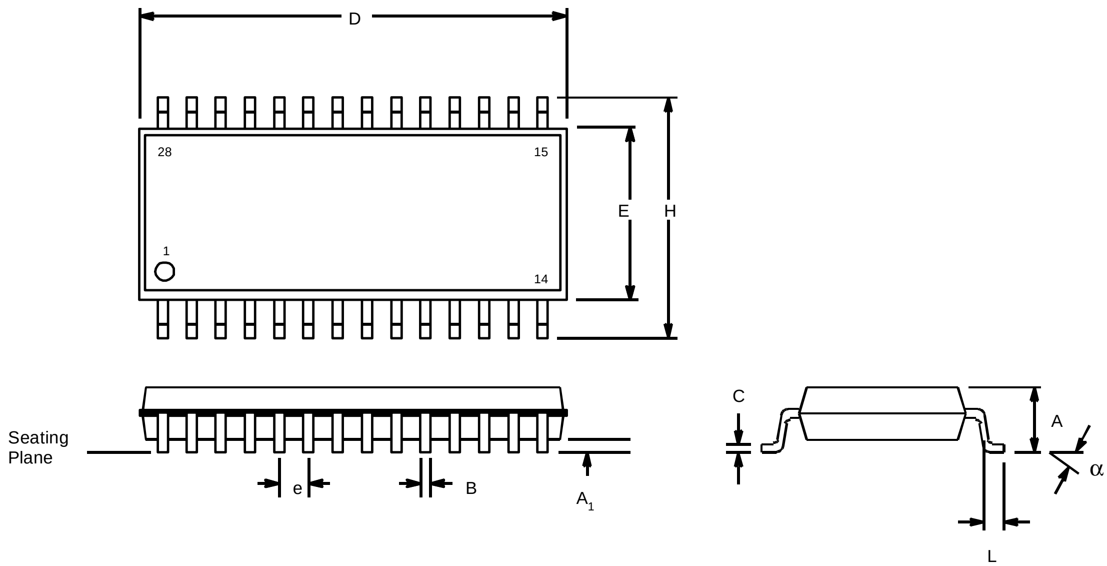


PE=HIGH TIMING:

When the PE pin is High, all changes begin relative to the rising edge of the Clkin reference signal. This includes not only the "zero tu" signals but also the divided output signals. The divided-by-two outputs will change on each rising edge. As QD can only be 0tu, QC is the only "divide by" output providing either divide-by- two or divide-by-four, not both.

PACKAGE DIMENSIONS

28 LEAD SHRINK SMALL OUTLINE PACKAGE
(QSOP 150 mils body)
Rev. 1.00



SYMBOL	MIN	MAX	MIN	MAX
A	0.053	0.068	1.35	1.73
A1	0.004	0.010	0.10	0.25
B	0.008	0.012	0.20	0.30
C	0.006	0.010	0.15	0.25
D	0.380	0.400	9.65	10.16
E	0.144	0.164	3.66	4.17
e	0.0256 BSC		0.65 BSC	
H	0.220	0.250	5.59	6.35
L	0.016	0.050	0.54	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	February 2007	Initial release.

NOTICE