



## UC3842G

### LINEAR INTEGRATED CIRCUIT

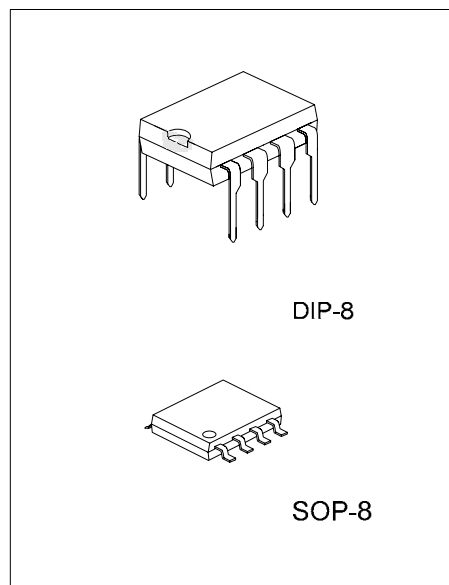
## HIGH PERFORMANCE CURRENT MODE CONTROLLER

### DESCRIPTION

The UTC **UC3842G** of high performance current mode controller is specifically designed for off-line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. This integrated circuit features approximately 300 $\mu$ A start up current, a precision reference trimmed the error amplifier input. Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and so on.

### FEATURES

- \* Low startup and operating current
- \* User defined switching frequency(Norm is 52kHz)
- \* Power-saving mode for low power
- \* Under voltage lockout with hysteresis
- \* Over voltage protection
- \* Latching PWM for Cycle-By-Cycle current limiting
- \* Internally trimmed reference with undervoltage lockout



\*Pb-free plating product number:  
UC3842GL

### ORDERING INFORMATION

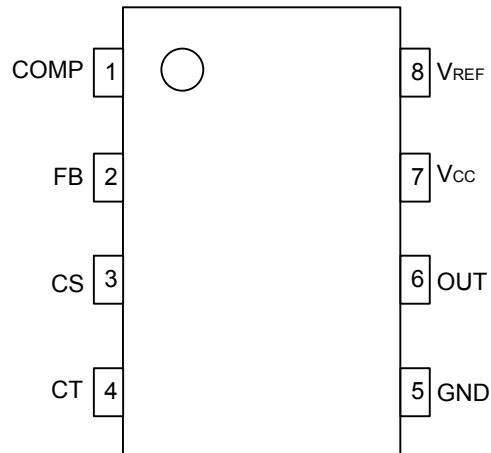
Ordering Number		Package	Packing
Normal	Lead Free Plating		
UC3842G-D08-T	UC3842GL-D08-T	DIP-8	Tube
UC3842G-S08-R	UC3842GL-S08-R	SOP-8	Tape Reel
UC3842G-S08-T	UC3842GL-S08-T	SOP-8	Tube

UC3842GL-D08-T

- (1)Packing Type
- (2)Package Type
- (3)Lead Plating

- (1) T: Tube, R: Tape Reel
- (2) D08: DIP-8, S08: SOP-8
- (3) L: Lead Free Plating, Blank: Pb/Sn

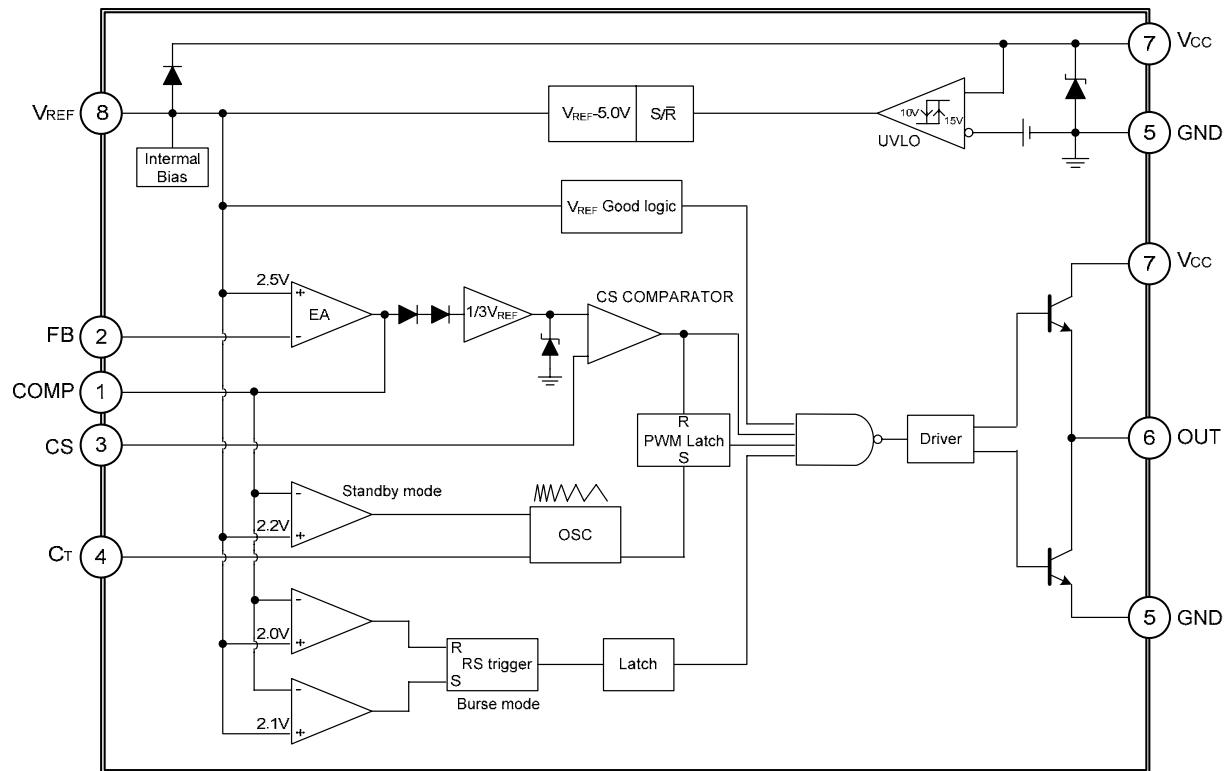
■ PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	Function
1	COMP	O	This pin is error amplifier output
2	FB	I	The error amplifier inverting input
3	CS	I	Current sense input
4	CT	I	The capacitor controlling switch frequency
5	GND		Ground
6	OUT	O	Output to the gate of external power MOS
7	V <sub>CC</sub>		Supply voltage
8	V <sub>REF</sub>	O	Inter 5V reference voltage output

### BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (Low Impedance Source)	V <sub>CC</sub>	30	V
Supply Voltage (I <sub>CC</sub> <30mA)	V <sub>CC</sub>	Self Limiting	V
Output Current (Peak)	I <sub>O(PEAK)</sub>	±1	A
Output Energy (Capacity load)		5	μJ
Junction Temperature	T <sub>J</sub>	+150	°C
Operating Temperature	T <sub>OPR</sub>	-40 ~ +125	°C
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ ELECTRICAL CHARACTERISTICS

(0°C Ta 70°C, V<sub>CC</sub>=15V, C<sub>T</sub>=3.3n, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>STANDBY SECTION</b>						
Reduce Frequency Point of Standby Mode	V <sub>COMP</sub>	Right load		2.2		V
<b>REFERENCE SECTION</b>						
Reference Output Voltage	V <sub>REF</sub>	I <sub>OUT</sub> =1.0mA	4.95	5.0	5.05	V
Line Regulation	ΔV <sub>REF</sub>	12V≤V <sub>CC</sub> ≤25V		3	20	mV
Load Regulation	ΔV <sub>REF</sub>	I <sub>OUT</sub> =1.0mA to 20mA		8	25	mV
Output Short Circuit Current	I <sub>SC</sub>		-30	-65	-180	mA
<b>OSCILLATOR SECTION</b>						
Frequency	f <sub>OSC1</sub>	Normal	49	52	55	KHz
Frequency	f <sub>OSC2</sub>	No load or right load		14		KHz
Frequency Change	Δf <sub>OSC</sub> /ΔV	12V≤V <sub>CC</sub> ≤25V		0.2	1.0	%
Oscillator Voltage	V <sub>OSC(P-P)</sub>			1.6		V
	V <sub>OSCL</sub>			1.2		V
	V <sub>OSCH</sub>			2.8		V
<b>ERROR AMPLIFIER SECTION</b>						
Input Voltage	V <sub>I(EA)</sub>	V <sub>COMP</sub> =2.5V	2.42	2.50	2.58	V
Input Bias Current	I <sub>I(BIAS)</sub>	V <sub>FB</sub> =5V		-0.3	-2	μA
AVOL		2V≤V <sub>OUT</sub> ≤4V	60	90		dB
Unity Gain Bandwidth		T <sub>J</sub> =25°C(Note1)	0.7	1		MHz
PSRR		12V≤V <sub>CC</sub> ≤25V	60	70		dB
Output Sink Current	I <sub>SINK</sub>	V <sub>FB</sub> =2.7V, V <sub>COMP</sub> =1.1V	2	4		mA
Output Source Current	I <sub>SOURCE</sub>	V <sub>FB</sub> =2.3V, V <sub>COMP</sub> =5V	-0.5	-0.7		mA
V <sub>OUT</sub> High	V <sub>OH</sub>	V <sub>FB</sub> =2.3V, R <sub>L</sub> =15K to GND	5.0	5.6		V
V <sub>OUT</sub> Low	V <sub>OL</sub>	V <sub>FB</sub> =2.7V, R <sub>L</sub> =15K to V <sub>REF</sub>		0.8	1.1	V
<b>CURRENT SENSE SECTION</b>						
Gain	G <sub>V</sub>	(Note2,3)	2.85	3	3.15	V/V
Maximum Input Signal	V <sub>I(MAX)</sub>	V <sub>COMP</sub> =5V(Note2)	0.9	1	1.1	V
PSRR		12V≤V <sub>CC</sub> ≤25V		70		dB
Input Bias Current	I <sub>BIAS</sub>			-2	-10	μA
Delay to Output				150	300	nS

## ■ ELECTRICAL CHARACTERISTICS (Cont.)

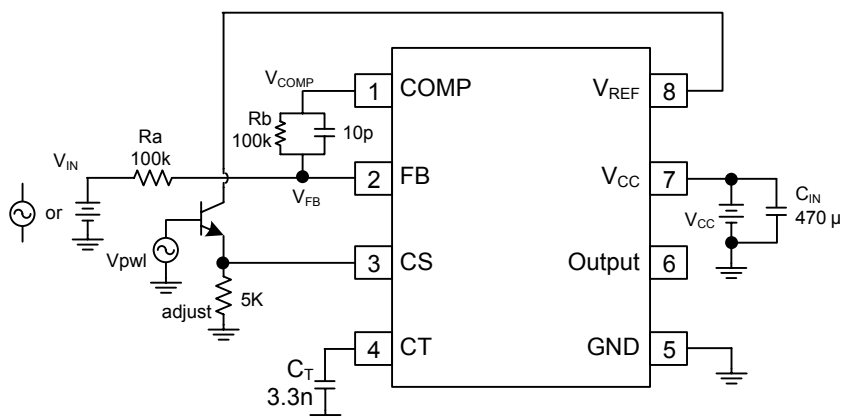
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
OUTPUT SECTION						
Output Voltage With UVLO Active	V <sub>OL(UVLO)</sub>	V <sub>CC</sub> =6V,I <sub>SINK</sub> =1mA		0.8	1.1	V
Output Voltage	V <sub>OL</sub>	I <sub>SINK</sub> =20mA		0.1	0.4	V
		I <sub>SINK</sub> =200mA		1.6	2.2	V
	V <sub>OH</sub>	I <sub>SOURCE</sub> =20mA	13	14.5		V
		I <sub>SOURCE</sub> =200mA	12	14.6		V
Output Voltage Rise and Fall time	t <sub>R</sub>	C <sub>L</sub> =1.0nF(Note1)		100	150	nS
	t <sub>F</sub>	C <sub>L</sub> =1.0nF(Note1)		100	150	
UNDER VOLTAGE LOCKOUT SECTION						
Startup Threshold	V <sub>TH(STAR-UP)</sub>		13.5	15	16.5	V
Min Operating Voltage	V <sub>OPR(MIN)</sub>	After Turn-ON	8.5	10	11.5	V
PWM SECTION						
Max Duty Cycle	D <sub>MAX</sub>		92	94		%
Minimum Duty Cycle	D <sub>MIN</sub>				0	%
TOTAL DEVICE						
Power Supply Zener Voltage	V <sub>Z</sub>	I <sub>CC</sub> =25mA	30	39		V
Power Operating Supply Current	I <sub>CC</sub>	Note2		7	10	mA
Startup Current	I <sub>START-UP</sub>	V <sub>CC</sub> =14V,UVLO Active		150	300	μA

Note: 1. These parameters, although guaranteed, are not 100% tested in production.

2. Parameters measured at trip point of latch with  $V_{FB}=0$ .

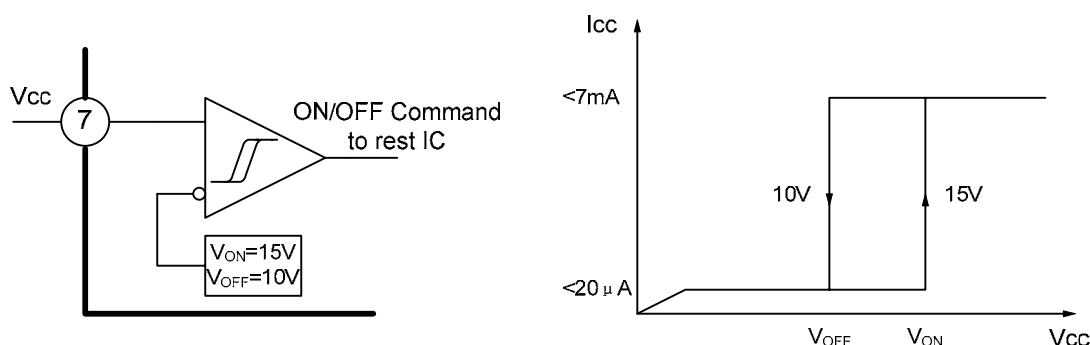
3. Gain defined as:  $A = V_{COMP} / V_{CS}$ ; 0  $V_{CS}$  0.8V

### ■ OPEN-LOOP TEST CIRCUIT



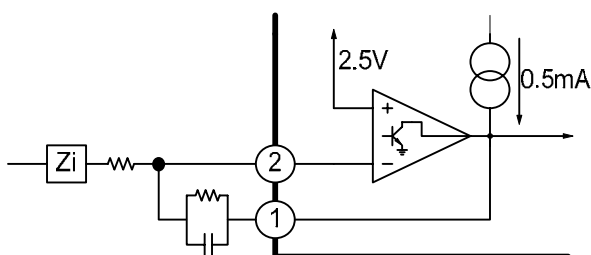
High peak current associated with capacity loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin5 in single point GND.

### ■ UNDER-VOLTAGE LOCKOUT



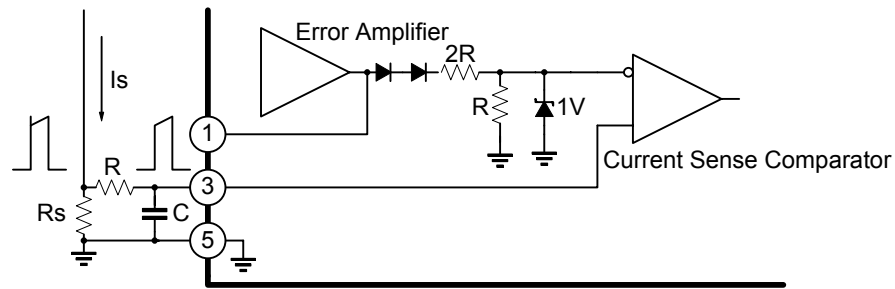
During Under-Voltage Lockout, the output driver is biased to a high impedance state. Pin6 should be shunt to GND with a bleeder resistor to prevent activating the power switch with output leakage currents.

### ■ ERROR AMPLIFIER CONFIGURATION



Error amplifier can source or sink up to 0.5mA

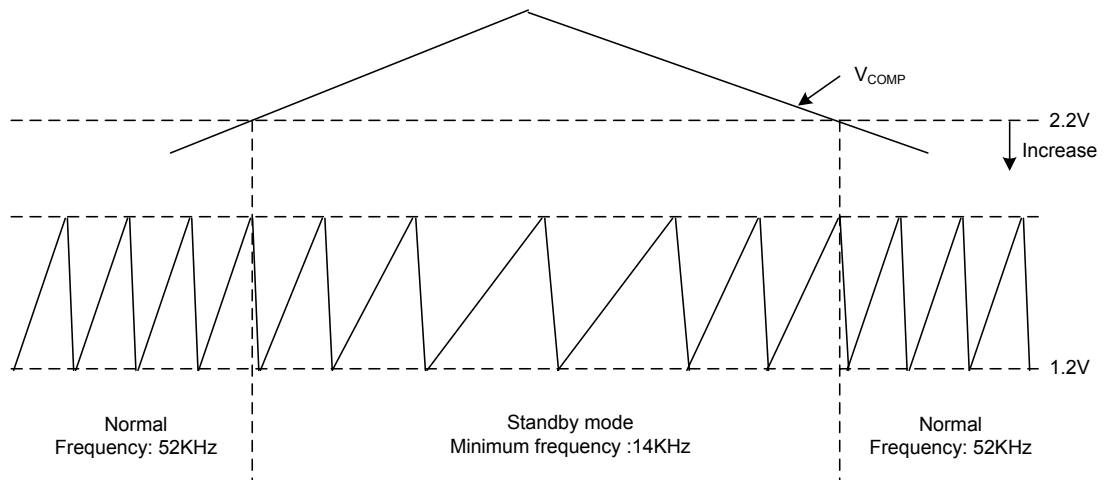
### ■ CURRENT SENSE CIRCUIT



Peak current ( $I_s$ ) determined by the formula:  $I_{sMAX} = 1V/R_s$ . A small RC filter be required to suppress switch transients

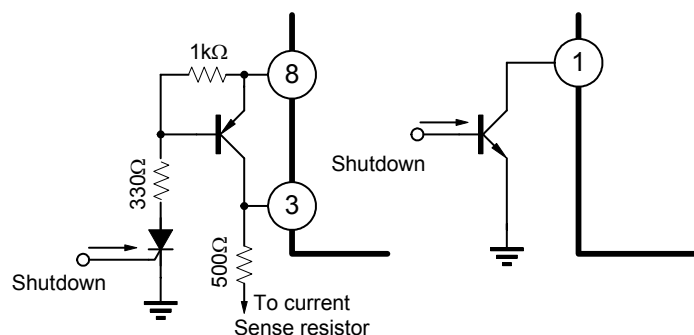
### ■ OSCILLATOR AND STANDBY MODE

We can judge the state of output load through the voltage of PIN1. In order to reduce the standby power, it will reduce the OSC frequency at right load. When  $V_{COMP}$  2.2V, the OSC frequency begins to reduce. The normal frequency is 52KHz, the minimum frequency is 14KHz.



OSC triangle wave

## ■ SHUTDOWN TECHNIQUE



Shutdown UTC **UC3842G** can be accomplished by two methods; either raise pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.