

CMOS BCD RATE MULTIPLIER

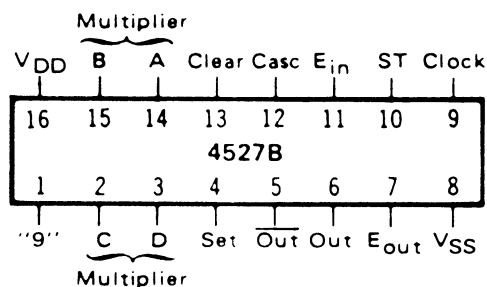
FEATURES

- ◆ Internally Synchronous for High Speed
- ◆ Strobe for Enabling or Inhibiting Outputs
- ◆ Enable and Cascade Inputs
- ◆ "9" Output Available for Cascading
- ◆ Complementary Outputs
- ◆ Clear and Set-To-Nine Inputs

DESCRIPTION

The 4527B is a BCD Digital Rate Multiplier (DRM) which provides an output pulse rate of the clock input pulse rate multiplied by 1/10 of the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. The output is clocked on the negative-going edge of the input clock. This device may be used to perform arithmetic operations, solve algebraic and differential equations, generate logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

CONNECTION DIAGRAM (all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C -55 to +125 °C

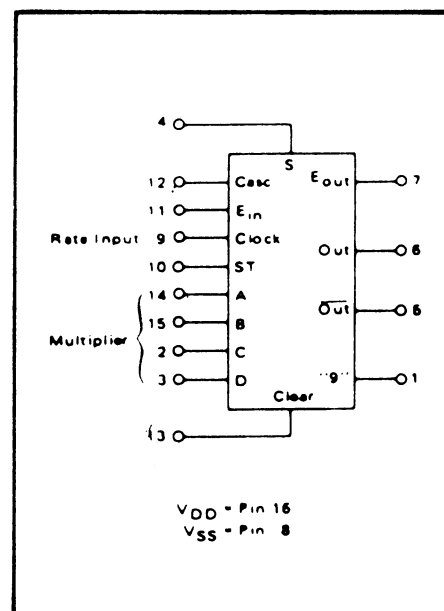
E -40 to +85 °C

TRUTH TABLE

Inputs										Number of Pulses or Output Logic Level (H or L)			
D	C	B	A	No. of Clock Pulses	E_{in}	Strobe	Cascade	Clear	Set	Pin 6 OUT	Pin 5 OUT	Pin 7 EOUT	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0				
X	X	X	X	10	0	0	1	0	0				
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μA _{dc}
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

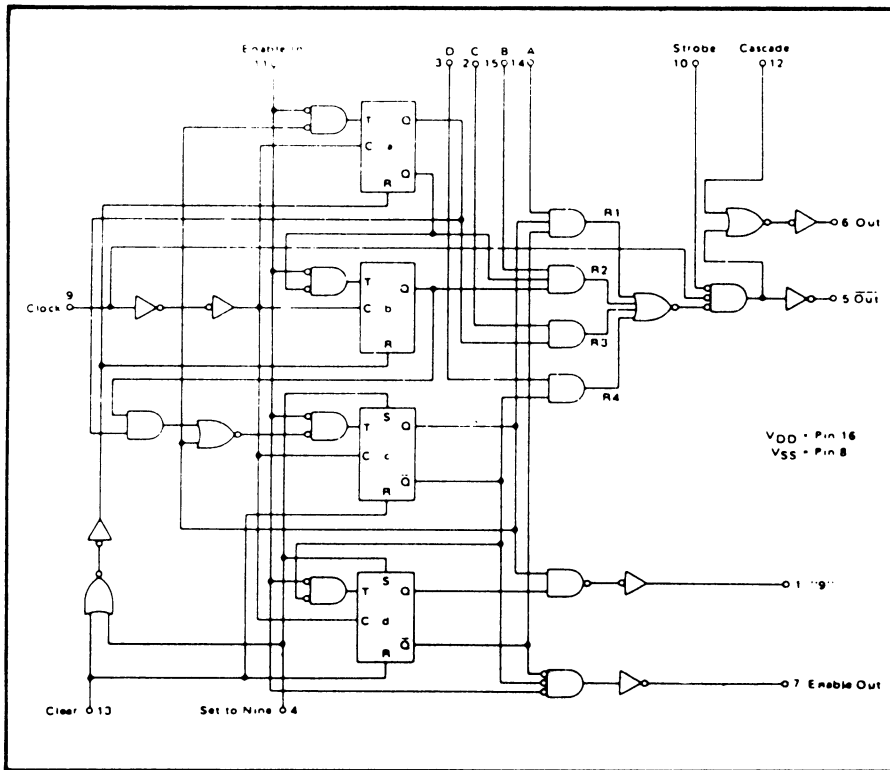
² T_{LOW} = -55°C for C
 = -40°C for E
 T_{HIGH} = +125°C for C
 = + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

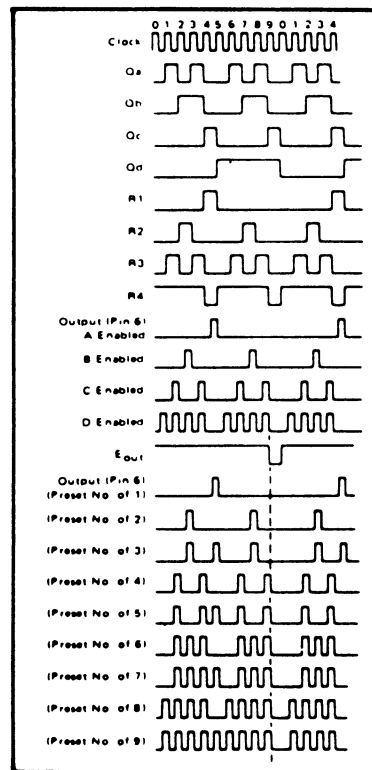
PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units			
CLOCKED OPERATION									
PROPAGATION DELAY TIME Clock to Out Clock to Out Clock to E _{out} Clock to "G" Cascade to Out Strobe to Out	t _{PLH} , t _{PHL}	5	—	150	300	ns			
		10	—	75	150				
		15	—	60	120				
		5	—	95	190	ns			
		10	—	50	100				
		15	—	35	70				
		5	—	250	500	ns			
		10	—	100	200				
		15	—	75	150				
		5	—	300	600	ns			
		10	—	125	250				
		15	—	100	200				
		5	—	95	190	ns			
		10	—	50	100				
		15	—	35	70				
		5	—	175	350	ns			
		10	—	80	160				
		15	—	60	120				
		OUTPUT TRANSITION TIME		t _{TLH} , t _{THL}	5	—	130	260	ns
					10	—	65	130	
					15	—	50	100	
		MINIMUM CLOCK PULSE WIDTH		PW _{CL}	5	—	165	330	ns
					10	—	85	170	
					15	—	65	130	
MAXIMUM CLOCK FREQUENCY		f _{CL}	5	1.5	3.0	—	MHz		
			10	3.0	6.0	—			
			15	4.0	8	—			
MAXIMUM CLOCK RISE AND FALL TIME ¹		t _{rCL} , t _{fCL}	5	15	—	—	μs		
			10	15	—	—			
			15	15	—	—			
MINIMUM ENABLE IN SETUP TIME		t _{setup}	5	—	175	350	ns		
			10	—	60	120			
			15	—	45	90			
SET OR CLEAR OPERATION									
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	350	700	ns			
		10	—	150	300				
		15	—	115	230				
MINIMUM SET OR CLEAR PULSE WIDTH	PW _S , PW _C	5	—	90	180	ns			
		10	—	35	70				
		15	—	30	60				
SET OR CLEAR REMOVAL TIME	t _{rem}	5	—	20	0	ns			
		10	—	10	0				
		15	—	7.5	0				

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

LOGIC DIAGRAM



TIMING DIAGRAM

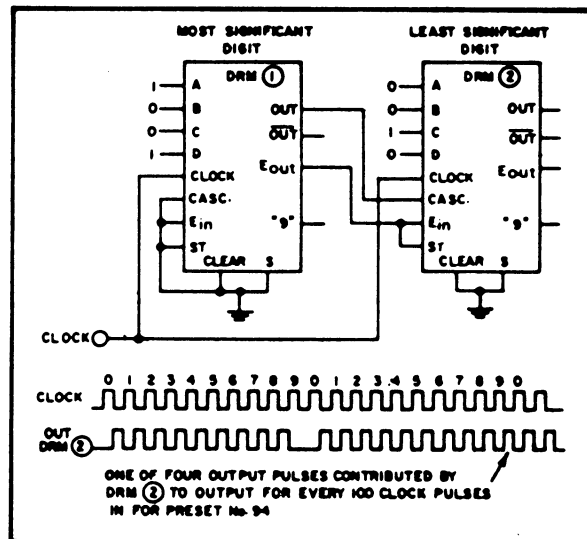


APPLICATIONS INFORMATION

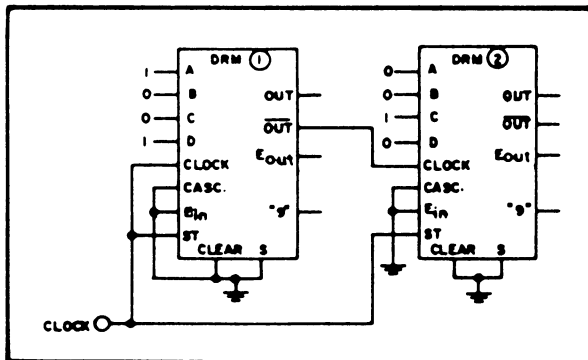
Cascading Connections

For words of more than one digit, 4527B devices may be cascaded in two different modes: an Add mode and a Multiply mode.

In the Add mode, some of the gaps left by the more significant unit at the count of 9 are filled in by the less significant units. Output Rate = Clock Rate X (0.1 BCD₁ + 0.01 BCD₂ + ...)



Two 4527B's cascaded in the "Add" mode with a preset number of 94.



Two 4527B's cascaded in the "Multiply" mode with a preset number of 36.

In the Multiply mode, the fraction programmed into the first DRM is multiplied by the fraction programmed into the second one.

$$\text{Output Rate} = \text{Clock Rate} \times \frac{\text{BCD}_1}{10} \times \frac{\text{BCD}_2}{10} \times \dots$$

