

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 16, 17, 32, 33, 48, 49, 64	V _{CCO}	Power		Output supply pins for LVPECL outputs.
2, 3, 12, 13	nc	Unused		No connect.
4	V _{CC}	Power		Core supply pin for LVPECL outputs.
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Pulled to $\frac{2}{3} V_{CC}$.
7	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTTL interface levels.
8	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
9	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. Pulled to $\frac{2}{3} V_{CC}$.
10	V _{EE}	Power		Negative supply pin.
11	OE	Input	Pullup	Output enable. When logic HIGH, the outputs are enabled (default). When logic LOW, the outputs are disabled and drive differential low: Qx = LOW, nQx = HIGH. LVCMOS / LVTTTL interface levels.
14, 15	nQ21, Q21	Output		Differential clock outputs. LVPECL interface Levels.
18, 19	nQ20, Q20	Output		Differential clock outputs. LVPECL interface Levels.
20, 21	nQ19, Q19	Output		Differential clock outputs. LVPECL interface Levels.
22, 23	nQ18, Q18	Output		Differential clock outputs. LVPECL interface Levels.
24, 25	nQ17, Q17	Output		Differential clock outputs. LVPECL interface Levels.
26, 27	nQ16, Q16	Output		Differential clock outputs. LVPECL interface Levels.
28, 29	nQ15, Q15	Output		Differential clock outputs. LVPECL interface Levels.
30, 31	nQ14, Q14	Output		Differential clock outputs. LVPECL interface Levels.
34, 35	nQ13, Q13	Output		Differential clock outputs. LVPECL interface Levels.
36, 37	nQ12, Q12	Output		Differential clock outputs. LVPECL interface Levels.
38, 39	nQ11, Q11	Output		Differential clock outputs. LVPECL interface Levels.
40, 41	nQ10, Q10	Output		Differential clock outputs. LVPECL interface Levels.
42, 43	nQ9, Q9	Output		Differential clock outputs. LVPECL interface Levels.
44, 45	nQ8, Q8	Output		Differential clock outputs. LVPECL interface Levels.
46, 47	nQ7, Q7	Output		Differential clock outputs. LVPECL interface Levels.
50, 51	nQ6, Q6	Output		Differential clock outputs. LVPECL interface Levels.
52, 53	nQ5, Q5	Output		Differential clock outputs. LVPECL interface Levels.
54, 55	nQ4, Q4	Output		Differential clock outputs. LVPECL interface Levels.
56, 57	nQ3, Q3	Output		Differential clock outputs. LVPECL interface Levels.
58, 59	nQ2, Q2	Output		Differential clock outputs. LVPECL interface Levels.
60, 61	nQ1, Q1	Output		Differential clock outputs. LVPECL interface Levels.
59	nQ0, Q0	Output		Differential clock outputs. LVPECL interface Levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			37		$k\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			75		$k\Omega$

Function Table

Table 3. Control Input Function Table.

Inputs		Outputs	
OE	CLK_SEL	Q0:Q21	nQ0:nQ21
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	CLK	nCLK
1	1	PCLK	nPCLK

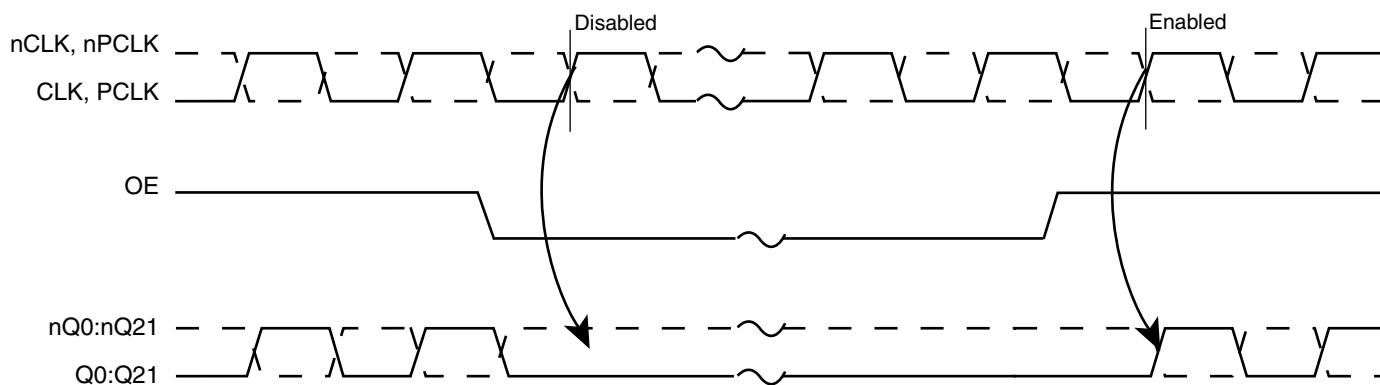


Figure 1. OE Timing Diagram

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to $V_{CC} + 0.5V$
Outputs, I_O (LVPECL) Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, θ_{JA}	22.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				230	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	OE, CLK_SEL $V_{CC} = V_{IN} = 3.465V$			5	μA
I_{IL}	Input Low Current	OE, CLK_SEL $V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			μA

Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN} = 3.465V$		150	μA
		nCLK	$V_{CC} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	CLK	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5		μA
		nCLK	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150		μA
V_{PP}	Peak-to-Peak Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.NOTE 2: Common mode input voltage is defined as V_{IH} .**Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{CC} = V_{IN} = 3.465V$		150	μA
		nPCLK	$V_{CC} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	PCLK	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5		μA
		nPCLK	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150		μA
V_{PP}	Peak-to-Peak Voltage; NOTE 1		0.3		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 1.5$		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 3		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: V_{IL} should not be less than -0.3V.NOTE 2: Common mode input voltage is defined as V_{IH} .NOTE 3: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

AC Electrical Characteristics

Table 5. $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				500	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq 500MHz$	2.0		3.0	ns
$tsk(o)$	Output Skew; NOTE 2, 3				100	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4				700	ps
t_{jit}	Buffer Additive Phase Jitter, RMS, refer to Additive Phase Jitter section; NOTE 5	Integration Range: 12kHz - 20MHz		0.4		ps
t_R / t_F	Output Rise/ Fall Time	20% to 80%	200		700	ps
t_S	Setup Time		1			ns
t_H	Hold Time		0.5			ns
odc	Output Duty Cycle	$f \leq 266MHz$	48		52	%
		$266 < f \leq 500MHz$	46		54	%

All parameters measured at f_{MAX} unless noted otherwise.

Special thermal considerations may be required. See Applications Section.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65. Measured at the output differential cross points.

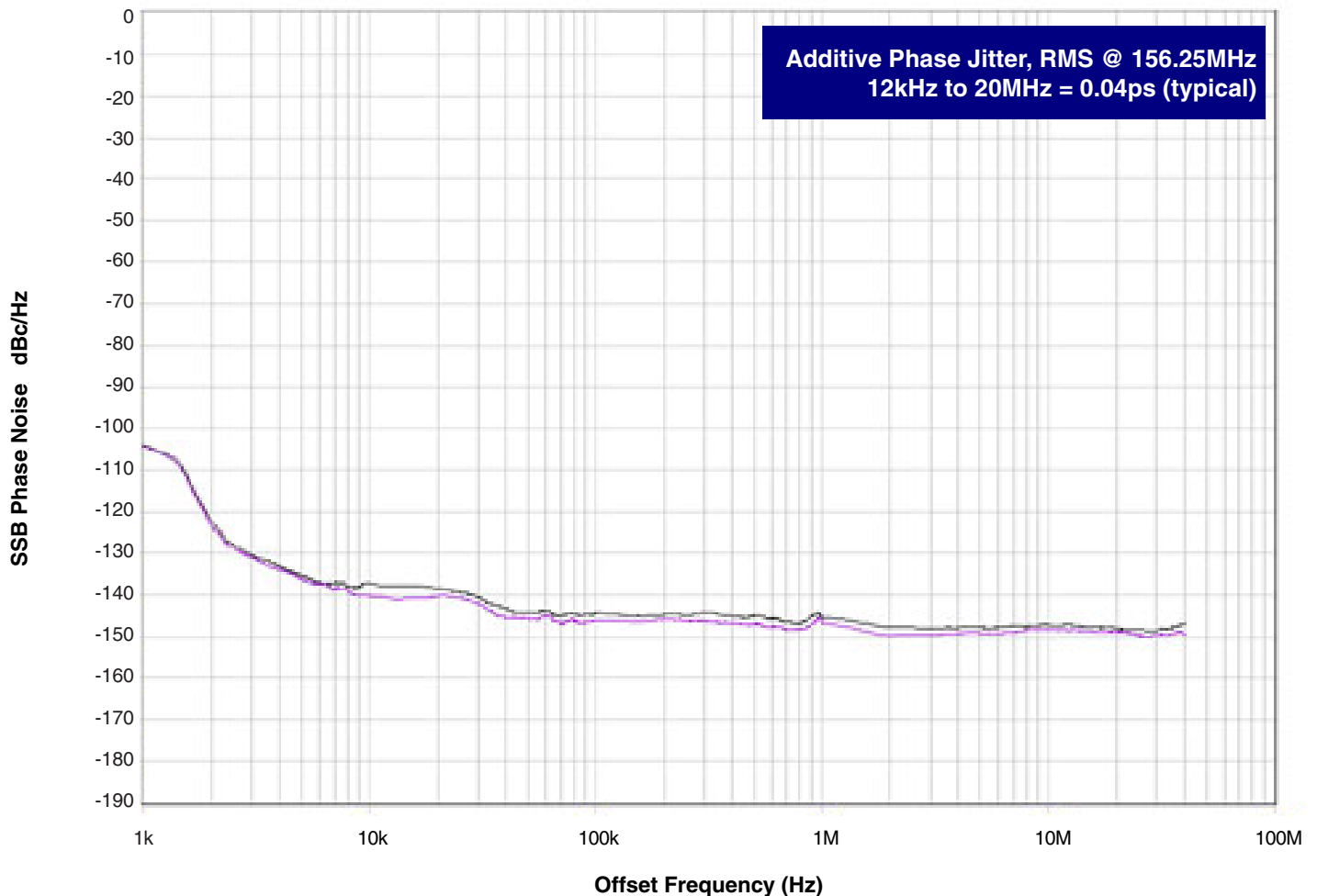
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions at the same temperature. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 5: Driving only one input clock.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band

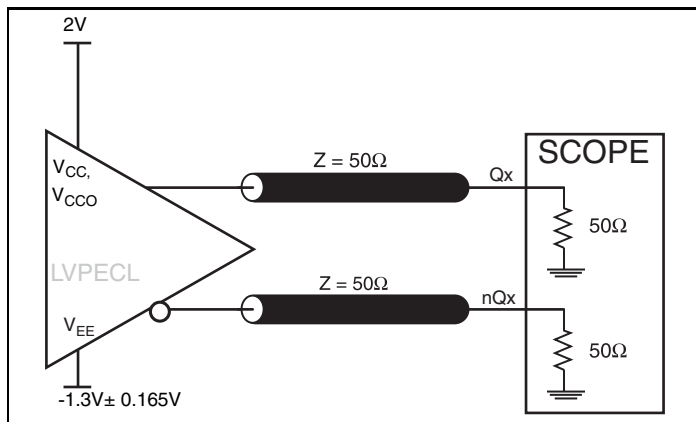
to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



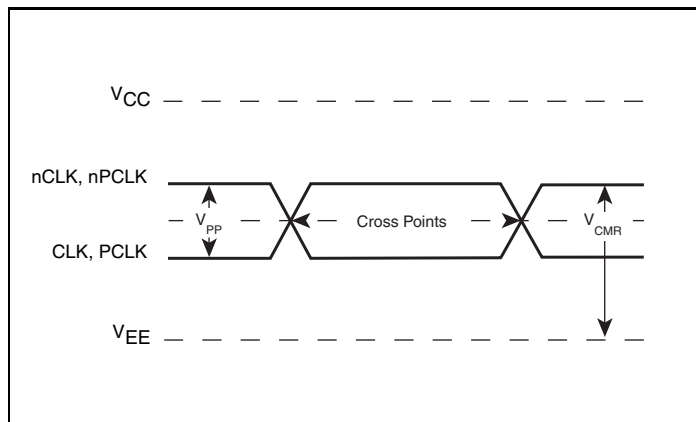
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the

device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

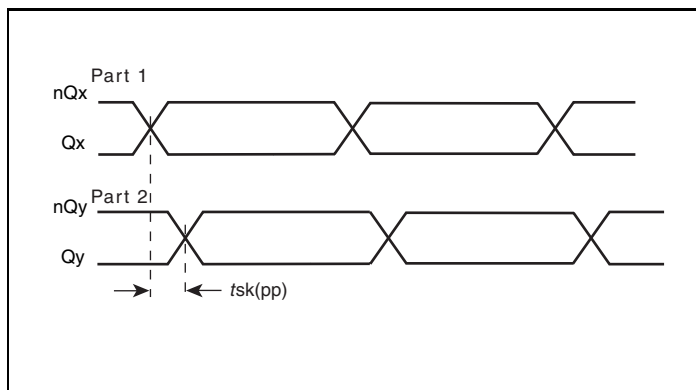
Parameter Measurement Information



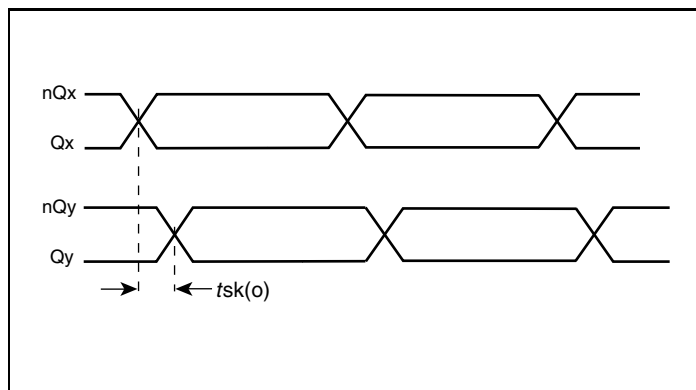
3.3V LVPECL Output Load AC Test Circuit



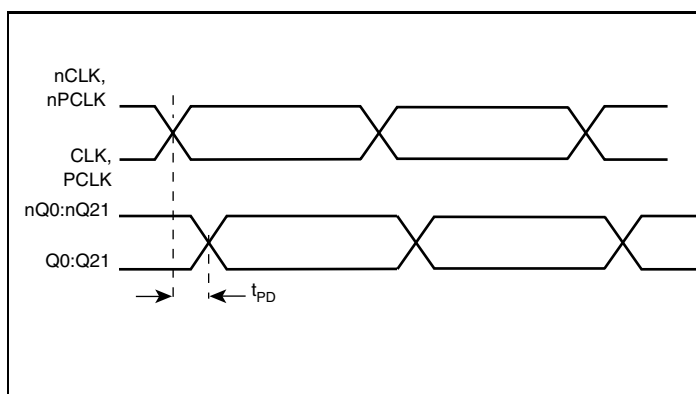
Differential Input Level



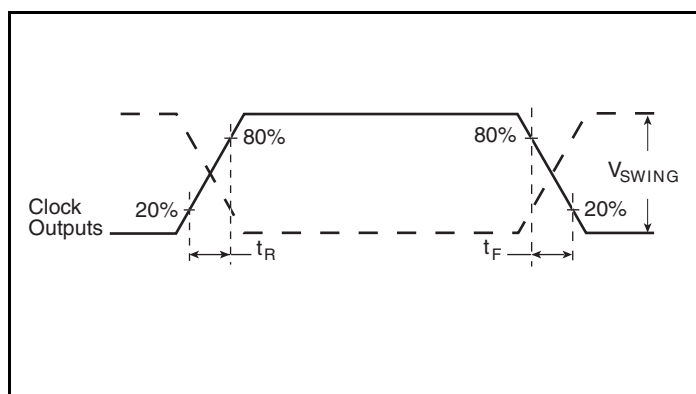
Part-to-Part Skew



Output Skew

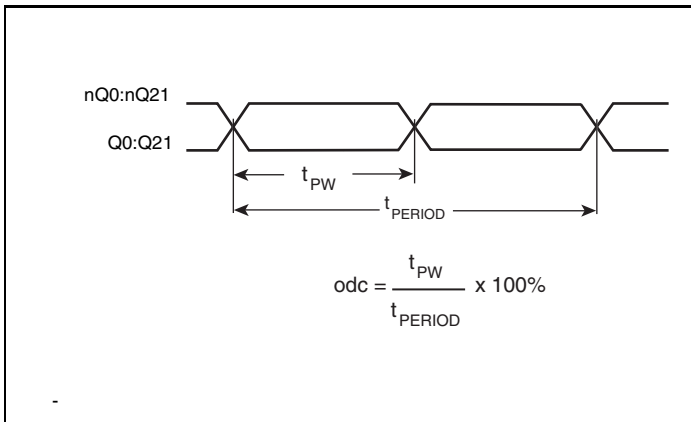


Propagation Delay



Output Rise/Fall Time

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

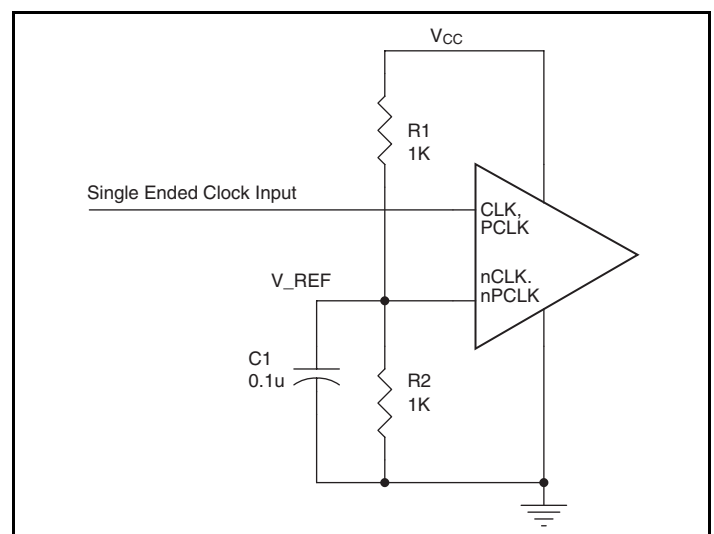


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVPECL, LVDS, LVHSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most

common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

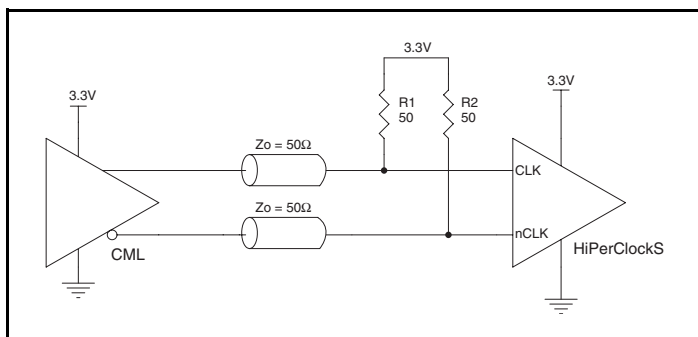


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Collector CML Driver

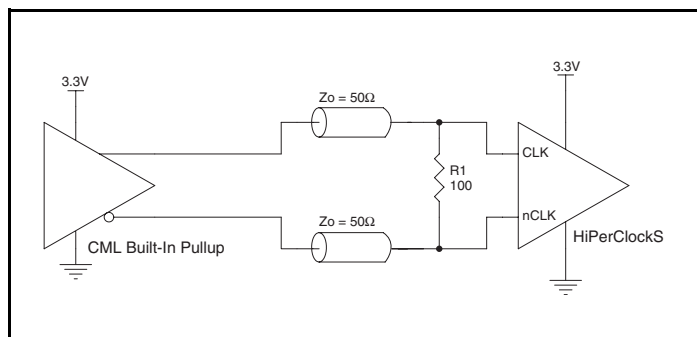


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a Built-In Pullup CML Driver

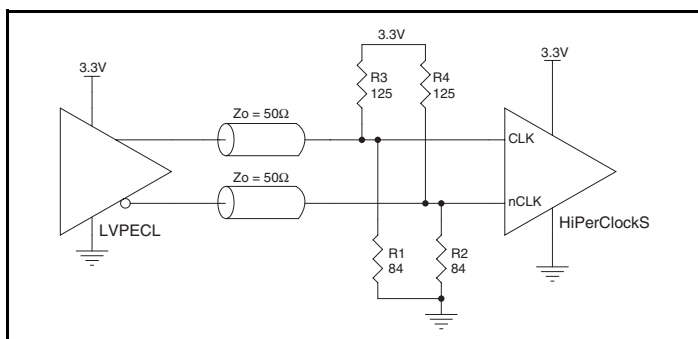


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

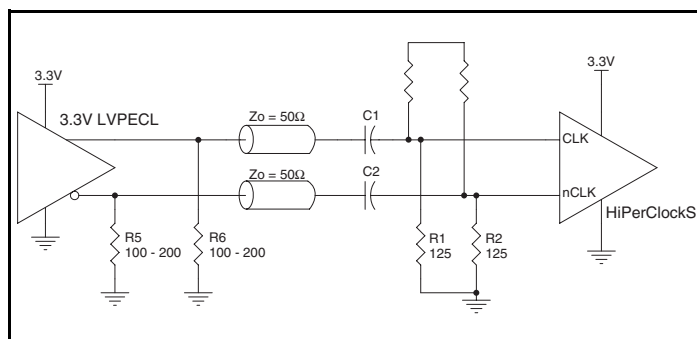


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

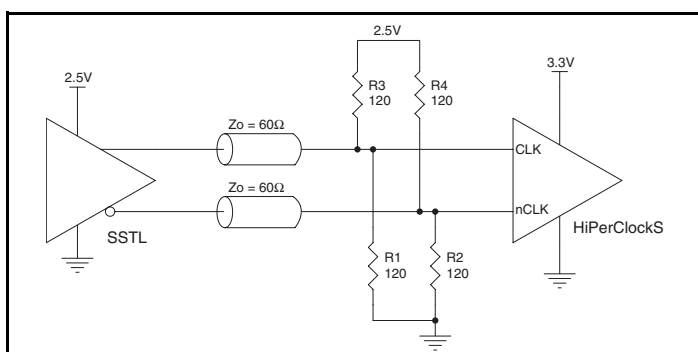


Figure 3E. HiPerClockS CLK/nCLK Input Driven by an SSTL Driver

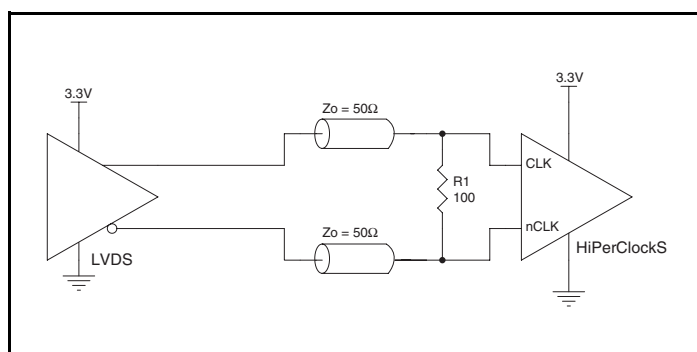


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4F show interface examples for the HiPerClockS PCLK/nPCLK input driven by the

most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

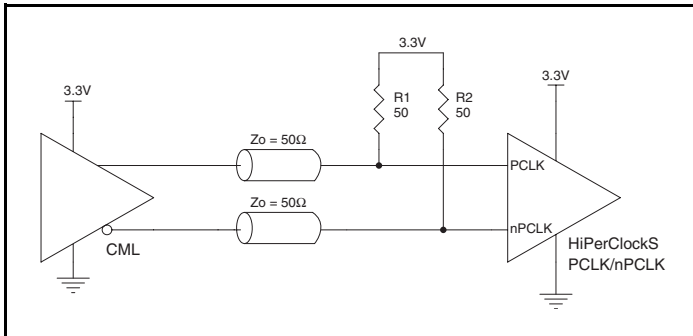


Figure 4A. HiPerClockS PCLK/nPCLK Input Driven by an Open Collector CML Driver

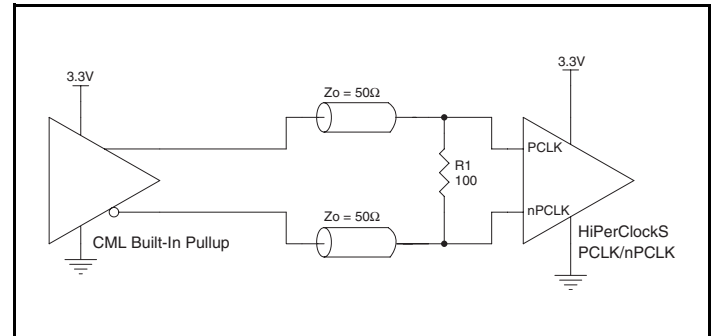


Figure 4B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

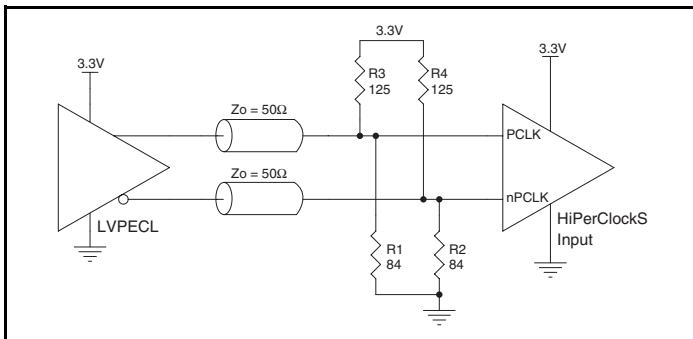


Figure 4C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

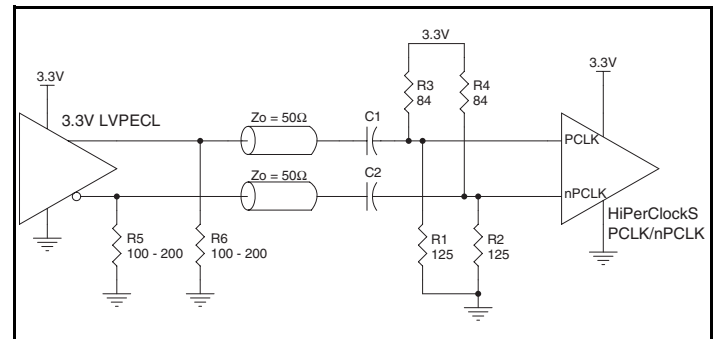


Figure 4D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

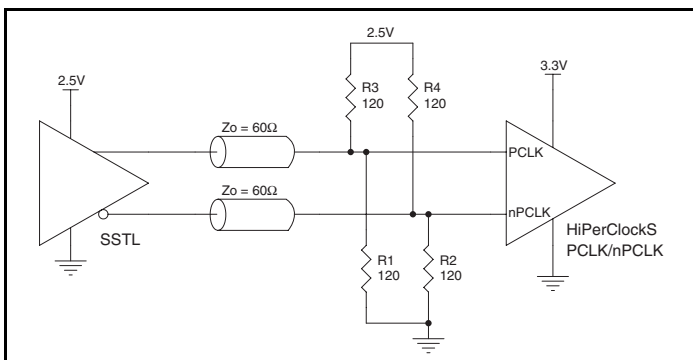


Figure 4E. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver (delete this figure)

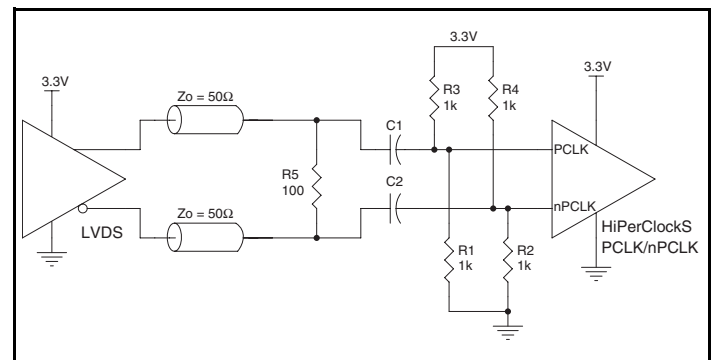


Figure 4F. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from CLK to ground.

PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from PCLK to ground.

LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

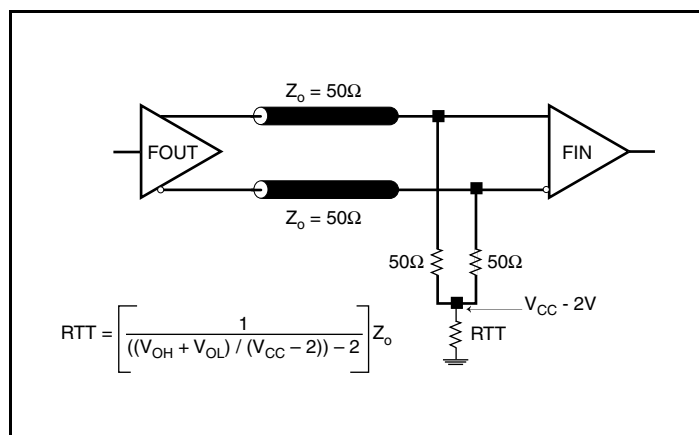


Figure 5A. 3.3V LVPECL Output Termination

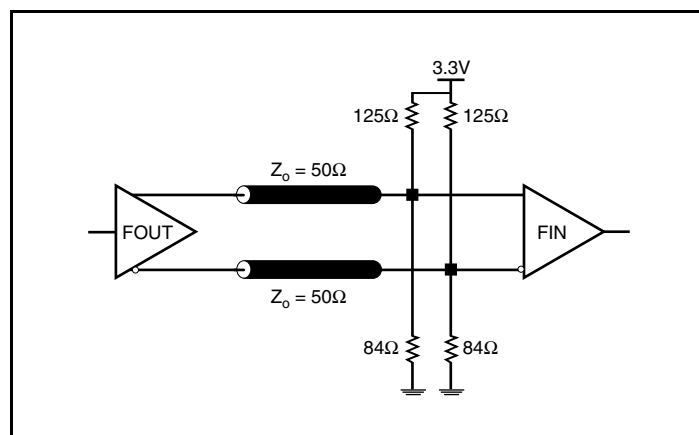


Figure 5B. 3.3V LVPECL Output Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are

application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

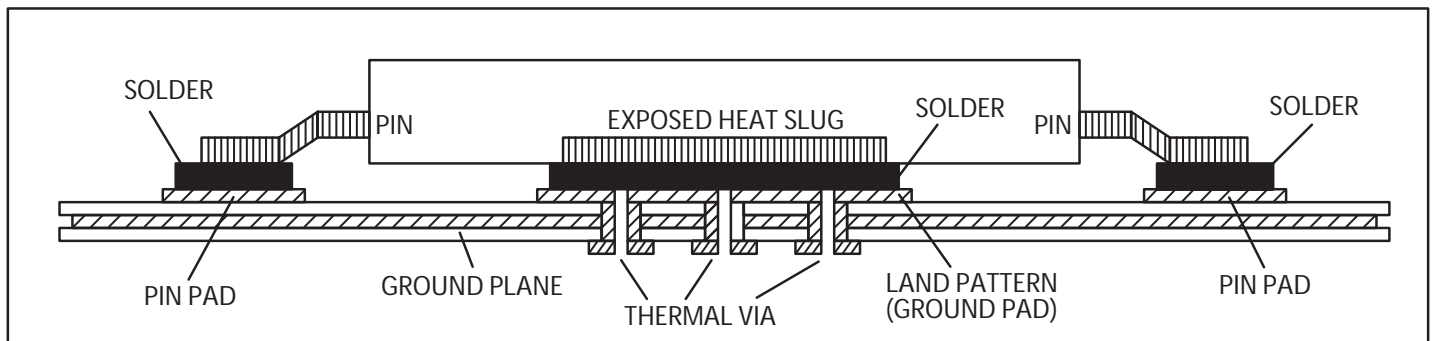


Figure 6. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS5334-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS534-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 230mA = 796.95mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $22 * 30mW = 660mW$

Total Power_{MAX} (3.8V, with all outputs switching) = $796.95mW + 660mW = 153.08mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming 0 air flow and a multi-layer board, the appropriate value is 17.2°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 1.457W * 17.2^\circ C/W = 110.1^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 64 Lead TQFP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	22.3°C/W	17.2°C/W	15.1°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7*.

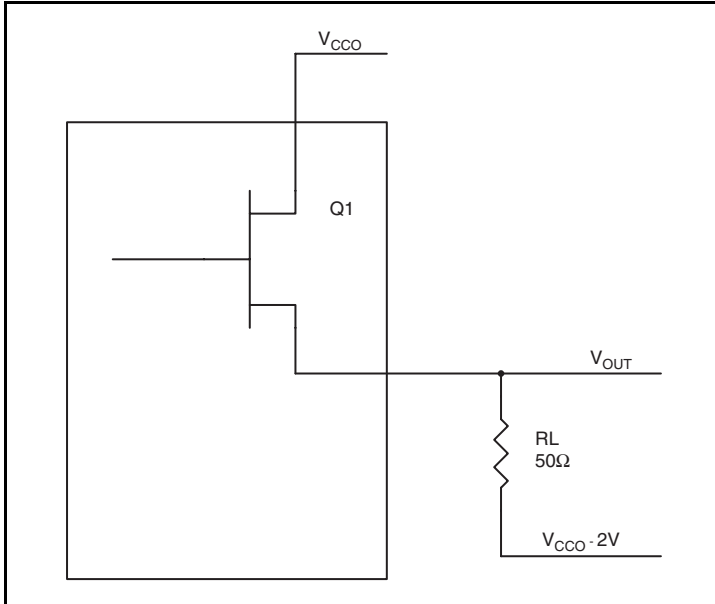


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.9V$
 $(V_{CCO_MAX} - V_{OH_MAX}) = 0.9V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$
 $(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 64 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Linear Feet per Minute	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	22.3°C/W	17.2°C/W	15.1°C/W

Transistor Count

The transistor count for ICS8534-01 is: 1474

Package Outline and Package Dimension

Package Outline - Y Suffix for 64 Lead TQFP, E-Pad

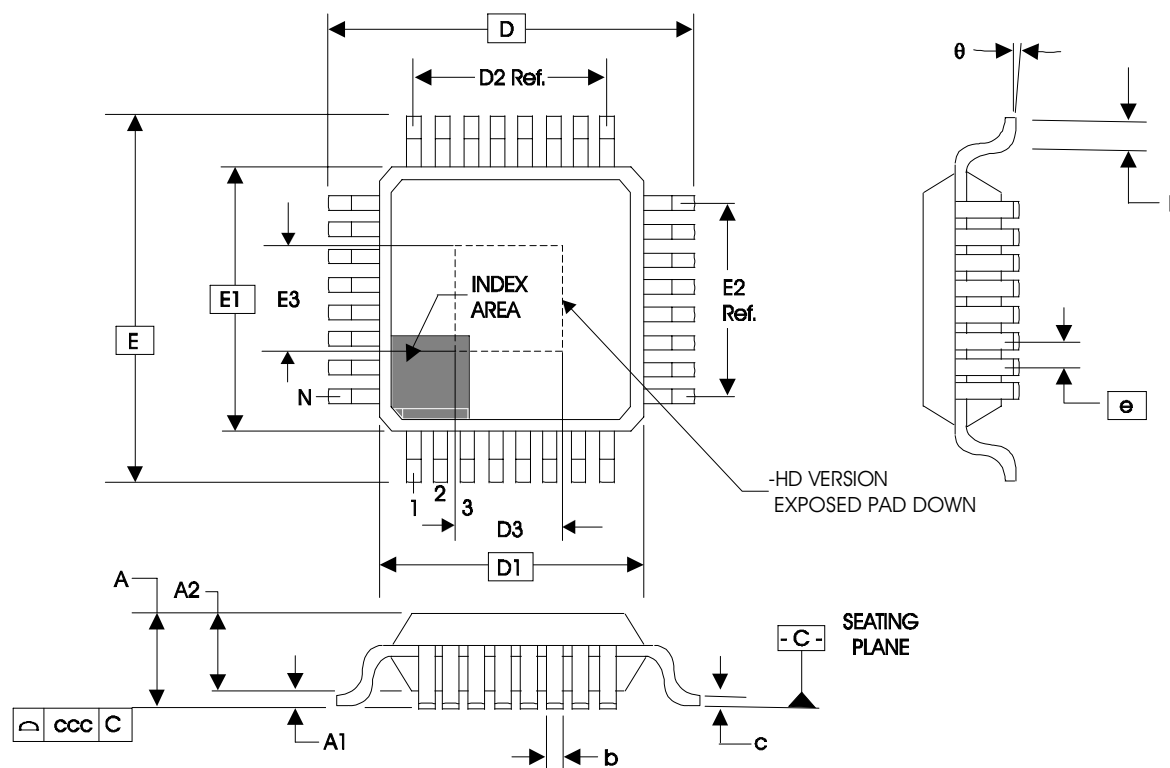


Table 8. Package Dimensions for 64 Lead TQFP, E-Pad

JEDEC Variation: ACD All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	64		
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E	12.00 Basic		
D1 & E1	10.00 Basic		
D2 & E2	7.50 Ref.		
D3 & E3	4.5	5.0	5.5
e	0.50 Basic		
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8534AY-01	ICS8534AY-01	64 Lead TQFP	Tray	0°C to +85°C
ICS8534AY-01T	ICS8534AY-01	64 Lead TQFP	500 Tape & Reel	0°C to +85°C
ICS8534AY-01LF	ICS8534AY-01LF	"Lead-Free" 64 Lead TQFP	Tray	0°C to +85°C
ICS8534AY-01LFT	ICS8534AY-01LF	"Lead-Free" 64 Lead TQFP	500 Tape & Reel	0°C to +85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature ranges, high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		15	Updated Package Outline and Package Dimensions.	11/19/04
A	T9	1 12 13 18	Features Section - added lead-free bullet. Added <i>Recommendations for Unused Input and Output Pins</i> section. Updated <i>EPad Thermal Release Path</i> section. Ordering Information Table. Added lead-free part number, marking and note. Updated format throughout the datasheet.	12/06/07

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

netcom@idt.com
480-763-2056

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan

Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe

IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851