CYV15G0104EQ

Multi Rate Video Cable Equalizer

Features

- Multi rate adaptive equalization
- Operates from 143 to 1485 Mbps serial data rate
- SMPTE 292M, SMPTE 344M, and SMPTE 259M compliant
- Supports DVB-ASI at 270 Mbps
- Maximum cable length adjustment for HD-SDI and SD-SDI data rates
- Carrier detect and mute functionality for HD-SDI and SD-SDI data rates
- Equalizer bypass mode
- Seamless connection with HOTLink II™ family
- Equalizes up to 350m of Belden 1694A and Canare L-5CFB coaxial cable at 270 Mbps
- Typically equalizes up to 200m of Belden 1694A and Canare L-5CFB coaxial cable at 1.485 Gbps
- Low power: 160 mW at 3.3V
- Single 3.3V supply
- 16-pin Quad Flat No Lead (QFN) package
- 0.18 μm CMOS technology
- Pb-free and RoHS compliant
- Pin compatible to existing QFN equalizer devices
- Uses Cypress CLEANLink™ technology

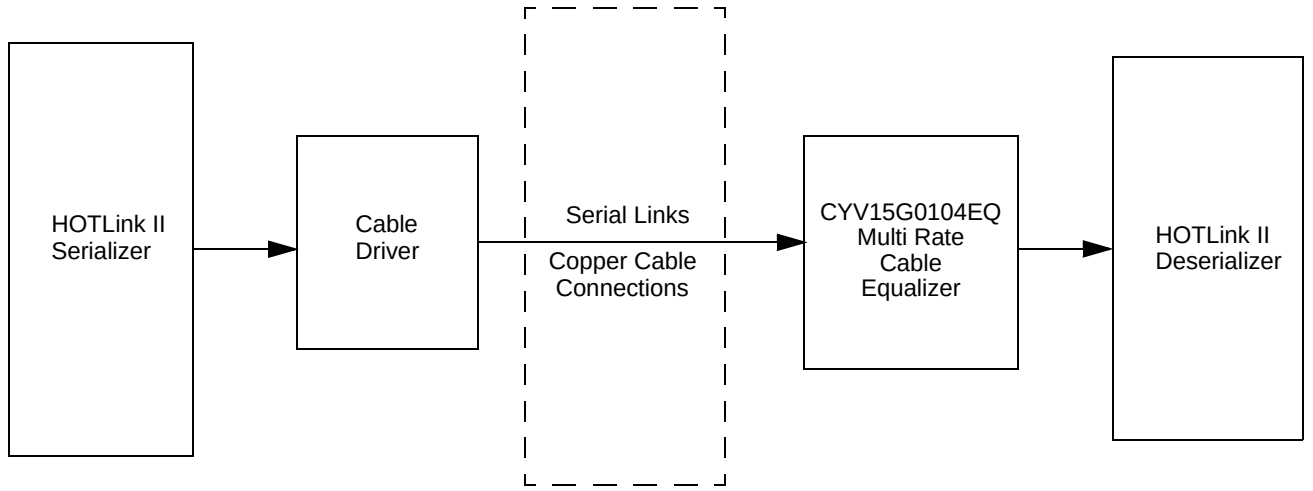
Functional Description

The CYV15G0104EQ is a multi rate adaptive equalizer designed to equalize and restore signals received over 75Ω coaxial cable. The equalizer meets SMPTE 292M, SMPTE 344M, and SMPTE 259M data rates. The CYV15G0104EQ is optimized to equalize up to 350m of Canare L-5CFB and Belden 1694A coaxial cable at 270 Mbps and typically up to 200m of Canare L-5CFB and Belden 1694A coaxial cable at 1.485 Gbps. The CYV15G0104EQ connects seamlessly to the HOTLink II family of transceiver devices.

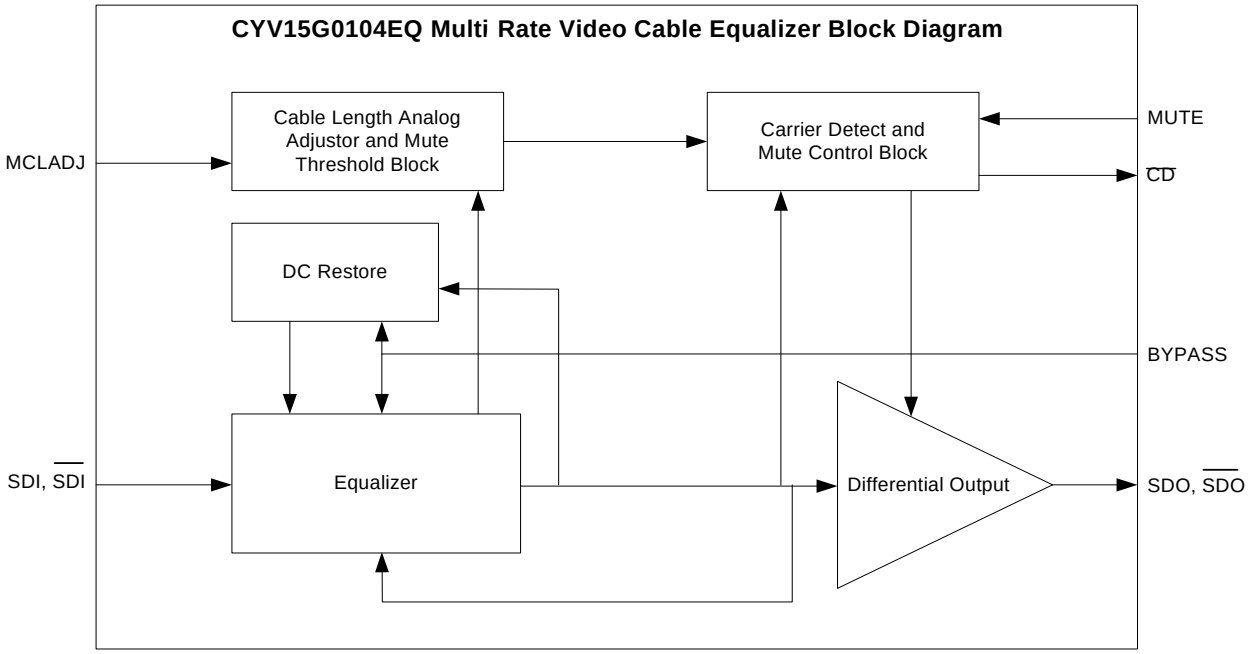
The CYV15G0104EQ has DC restoration to compensate for the DC content of the SMPTE pathological patterns. The maximum cable length adjust (MCLADJ) sets the approximate maximum cable length to equalize at SD and HD data rates. The CYV15G0104EQ's differential serial outputs (SDO, SDO) mute, when the approximate cable length set by MCLADJ is reached, and carrier detect (CD) is tied to MUTE. MUTE pin controls muting the outputs of the equalizer at HD and SD data rates.

Power consumption is typically 160 mW at 3.3V.

Equalizer System Connection Diagram



Equalizer Block Diagram



Pinouts

Figure 1. Pin Diagram - 16 Pin QFN (Top View)

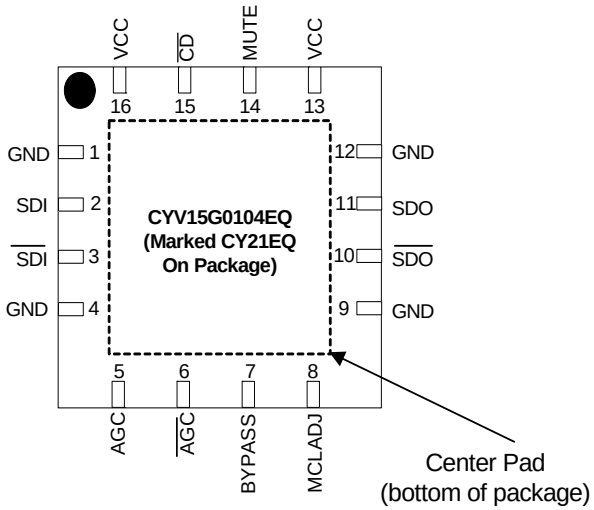


Table 1. Pin Descriptions - CYV15G0104EQ Single Channel Cable Equalizer

Name	IO Characteristics	Signal Description
Control Signals		
MUTE	LVTTL Input	**Mute.** When the MUTE pin is set LOW, the equalizer's differential serial outputs are not muted. When the MUTE pin is set HIGH, the equalizer's differential serial outputs are muted. BYPASS setting is ignored when MUTE is HIGH. Connecting $\overline{CD}$ to MUTE pin enables automatic muting of the equalizer upon loss of signal. Do not leave unused MUTE pin floating. Always drive it to a known state.
$\overline{CD}$	LVTTL Output	**Carrier Detect.** When the incoming data stream is present and maximum cable length does not exceed that set by MCLADJ, $\overline{CD}$ outputs a voltage less than 0.8V. When the incoming data stream is not present or maximum cable length exceeds that set by MCLADJ, $\overline{CD}$ outputs a voltage greater than 2.8V. Connecting $\overline{CD}$ to MUTE pin enables automatic muting of the equalizer upon loss of signal.
MCLADJ	Analog Input	**Maximum Cable Length Adjust.** The maximum equalized cable length is set by the voltage applied to the MCLADJ input. When the maximum cable length set by MCLADJ is reached, the $\overline{CD}$ indicator is deasserted. If MCLADJ functionality is not needed, this pin should be left floating or tied to ground to allow maximum equalized cable length. MCLADJ works at both SD and HD data rates.
BYPASS	LVTTL Input	**Equalizer Bypass.** When BYPASS is set HIGH, the signal presented at the equalizer's differential serial inputs (SDI, $\overline{SDI}$) is routed to the equalizer's differential serial outputs (SDO, $\overline{SDO}$) without equalizing. When BYPASS is set LOW, the incoming video data stream is equalized and presented at the equalizer's serial differential outputs (SDO, $\overline{SDO}$). When MUTE pin is set HIGH, BYPASS setting is ignored and the serial outputs are muted.
AGC, $\overline{AGC}$	Analog	**Automatic Gain Control.** Place a capacitor of 1 µF between the AGC and $\overline{AGC}$ pins.
SDO, $\overline{SDO}$	Differential Output	**Differential Serial Outputs.** The equalized serial video data stream is presented at the SDO/$\overline{SDO}$ differential serial CML output.
SDI, $\overline{SDI}$	Differential Input	**Differential Serial Inputs.** SDI/$\overline{SDI}$ accepts either a single-ended or differential serial video data stream over 75Ω coaxial cable.
Power		
VCC	Power	**Power Supply for Device.** Connect to +3.3V DC.
GND	Gnd	**Connect to Ground.**
Center Pad	–	**Connect to PCB Ground for Maximum Thermal Dissipation.**

Equalizer Operation

The CYV15G0104EQ is a high speed adaptive cable equalizer designed to equalize standard definition (SD) and high definition (HD) serial digital interface (SDI) video data streams..The CYV15G0104EQ equalizer is optimized to equalize up to 350m of Belden 1694A cable and Canare L-5CFB cable at 270 Mbps and typically up to 200m of Belden 1694A cable and Canare L-5CFB cable at 1.485 Gbps. The CYV15G0104EQ equalizer contains one power supply and typically consumes 160 mW power at 3.3V. The multi rate equalizer meets the SMPTE 259M, SMPTE 292M, SMPTE 344M, and DVB-ASI video standards. It meets all pathological requirements for SMPTE 292M as defined by RP198 and for SMPTE 259M as defined by RP178. The CYV15G0104EQ multi rate cable equalizer operates from 143 Mbps to 1.485 Gbps serial data rate.

The CYV15G0104EQ equalizer has multiple variable gain equalization stages that reverse the attenuation effects of the cable. This equalization is achieved by separate regulation of the lower and higher frequency components in the signal to give a clean output eye diagram. The CYV15G0104EQ has DC restoration to compensate for the DC content of the SMPTE pathological patterns.

SDI, $\overline{\text{SDI}}$

CYV15G0104EQ accepts single-ended or differential serial video data streams over 75Ω coaxial cable. It is recommended to AC couple the SDI, $\overline{\text{SDI}}$ inputs as they are internally biased to 1.2V.

SDO, $\overline{\text{SDO}}$

The CYV15G0104EQ has differential serial output interface drivers that use Current Mode Logic (CML) drivers to provide source matching for the transmission line. These outputs are either AC coupled or DC coupled to HOTLink II receivers.

MCLADJ

Maximum Cable Length Adjust (MCLADJ) sets the approximate maximum amount of cable to be equalized. When the maximum cable length set by MCLADJ is reached, the $\overline{\text{CD}}$ pin is deasserted. To enable automatic muting of the device upon loss of signal, $\overline{\text{CD}}$ should be tied directly to MUTE. MCLADJ works at SD and HD data rates.

Figure 2 on page 7 illustrates the voltage required at MCLADJ input to equalize various Belden 1694A cable lengths. If MCLADJ functionality is not required, this pin should be left floating or tied to ground to enable maximum equalized cable length.

MUTE

MUTE is an input pin that controls the muting of the equalizer's output. MUTE operates for both HD and SD data rates.

If MUTE is set LOW, the equalizer serial outputs are not muted. If MUTE is set HIGH, then the equalizer serial outputs are muted. When MUTE is active, BYPASS setting is also ignored.

Connecting $\overline{\text{CD}}$ to MUTE pin enables automatic muting of the equalizer upon loss of signal.

Do not leave the MUTE pin floating. Always drive it to a known state.

Carrier Detect ($\overline{\text{CD}}$)

Carrier Detect is an active LOW output pin that indicates the presence of a valid incoming data signal. When the incoming data signal is present, and maximum cable length does not exceed that set by MCLADJ, $\overline{\text{CD}}$ outputs a voltage less than 0.8V.

When the incoming data stream is not present, or maximum cable length exceeds that set by MCLADJ, $\overline{\text{CD}}$ outputs a voltage greater than 2.8V.

Connecting $\overline{\text{CD}}$ to MUTE pin enables automatic muting of the equalizer upon loss of signal.

BYPASS

The CYV15G0104EQ has a bypass mode that enables the user to bypass the equalizer's equalization and DC restoration functions. When BYPASS is set HIGH, the signal presented at the equalizer's differential serial inputs (SDI, $\overline{\text{SDI}}$) is routed to the equalizer's differential serial outputs (SDO, $\overline{\text{SDO}}$) without equalizing.

When BYPASS is set LOW, the incoming video data stream is equalized and presented at the equalizer's differential serial outputs (SDO, $\overline{\text{SDO}}$).

AGC

Place a capacitor of 1 μF between the AGC and $\overline{\text{AGC}}$ pins of the CYV15G0104EQ equalizer

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +3.8V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage ..... –0.5V to V_{CC}+0.5V

Electro Static Discharge (ESD) HBM.....> 2000 V (JEDEC EIA/JESD-A114A)

Latch Up Current .....> 200 mA

Power Up Requirements

The CYV15G0104EQ contains one power supply. The voltage on any input or IO pin must not exceed the power pin during power up.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ±5%

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage[1]	–	3.135	3.3	3.465	V
P_D	Power Consumption[2]	–	125	160	190	mW
I_S	Supply Current[1]	–	38	48	60	mA
V_{CMOUT}	Output Common Mode Voltage[1]	Load = 50Ω	–	$V_{CC} - \Delta V_{SDO}/2$ = 2.9	–	V
V_{CMIN}	Input Common Mode Voltage[1] (Bypass = High)	–	1		1.4	V
	Input Common Mode Voltage[1] (Bypass = Low)	–	0		2.9	V
–	Floating MCLADJ DC Voltage[1]	–		1.3		V
–	MCLADJ Range[2]	–	0.4	0.72	1.02	V
$V_{\overline{CD}(OH)}$	$\overline{CD}$ Output Voltage[1]	Carrier Not Present	2.8	–	–	V
$V_{\overline{CD}(OL)}$		Carrier Present	–	–	0.8	V
V_{MUTE}	MUTE Input Voltage Required to Force Outputs to Mute[1]	Min to Mute	2.5		–	V
V_{MUTE}	MUTE Input Voltage Required to Force Active[1]	Max to Activate	–	–	1	V

Notes
1. Production test.
2. Calculated results from production test.

AC Electrical Characteristics

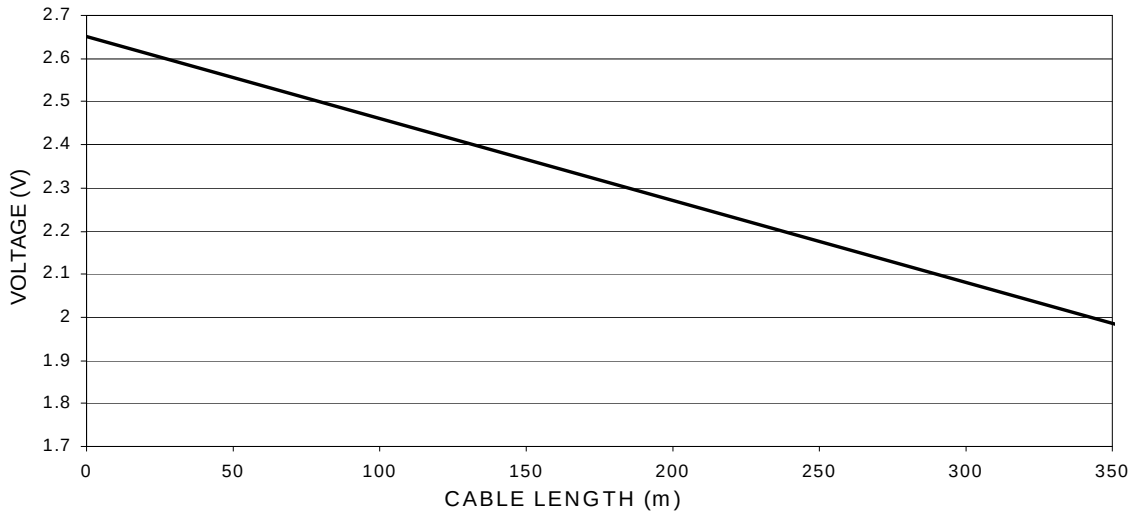
Parameter	Description	Test Conditions	Min	Typ	Max	Unit
–	Serial Input Data Rate[1]	–	143	–	1485	Mbps
V_{SDI}	Input Voltage Swing	Single-ended, at the transmitter, HD data rate	500[5]		1200	mV
V_{SDI}	Input Voltage Swing	Single-ended, at the transmitter, SD data rate	500[6]		1200	mV
ΔV_{SDO}	Output Voltage Swing[1]	Differential$_{p-p}$, 50Ω load	450	700	950	mV
–	Output Jitter for Various Cable Lengths and Data Rates	270 Mbps Belden 1694A: 0-350m Canare L-5CFB: 0-350m 800 mV transmit amplitude Equalizer pathological pattern	–	0.2[1]	–	UI
		1.485 Gbps Belden 1694A: 0-140m Canare L-5CFB: 0-140m 800 mV transmit amplitude Equalizer pathological pattern	–	0.25[1]	–	UI
		1.485 Gbps Belden 1694A: 140-200m Canare L-5CFB: 140-200m 800 mV transmit amplitude Equalizer pathological pattern	–	0.3[7]	–	UI
–	Output Rise/Fall Time[3, 4]	20% - 80%, HD data rate	80	120	220	ps
	Output Rise/Fall Time[3, 4]	20% - 80%, SD data rate	80	120	350	ps
–	Mismatch in Rise/Fall Time[3, 4]	–	–	–	30	ps
–	Duty Cycle Distortion[3, 4]	HD color bar pattern	–	20	–	ps
–	Overshoot[3, 4]	–	–	–	10	%
–	Input Return Loss[3]	–	-15	–	–	dB
–	Input Resistance[3, 4]	Single-ended	–	2.5	–	kΩ
–	Input Capacitance[3, 4]	Single-ended	–	1	–	pF
–	Output Resistance[3, 4]	Single-ended	–	50	–	Ω

Notes
3. Not tested. Based on characterization.
4. Not tested. Guaranteed by design simulations.
5. Based on characterization across temperature and voltage with 140m of Belden 1694A cable, transmitting SMPTE Equalizer Pathological Test Pattern.
6. Based on characterization across temperature and voltage with 350m of Belden 1694A cable, transmitting SMPTE Equalizer Pathological Test Pattern.
7. Based on characterization at T_A = 25°C, V_{CC} = 3.3V

Typical Performance Graphs

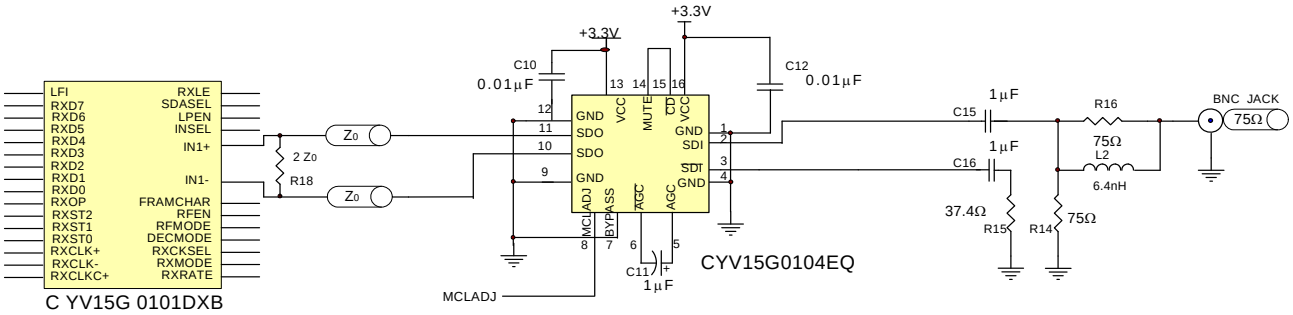
(Unless otherwise stated, V_{CC} = 3.3V, T_A = 25°C)

Figure 2. MCLADJ Input Voltage vs Belden 1694A Cable Length at SD-SDI and HD-SDI Data Rates



Typical Application Circuit

Figure 3. Interfacing CYV15G0104EQ to the HOTLink II SerDes

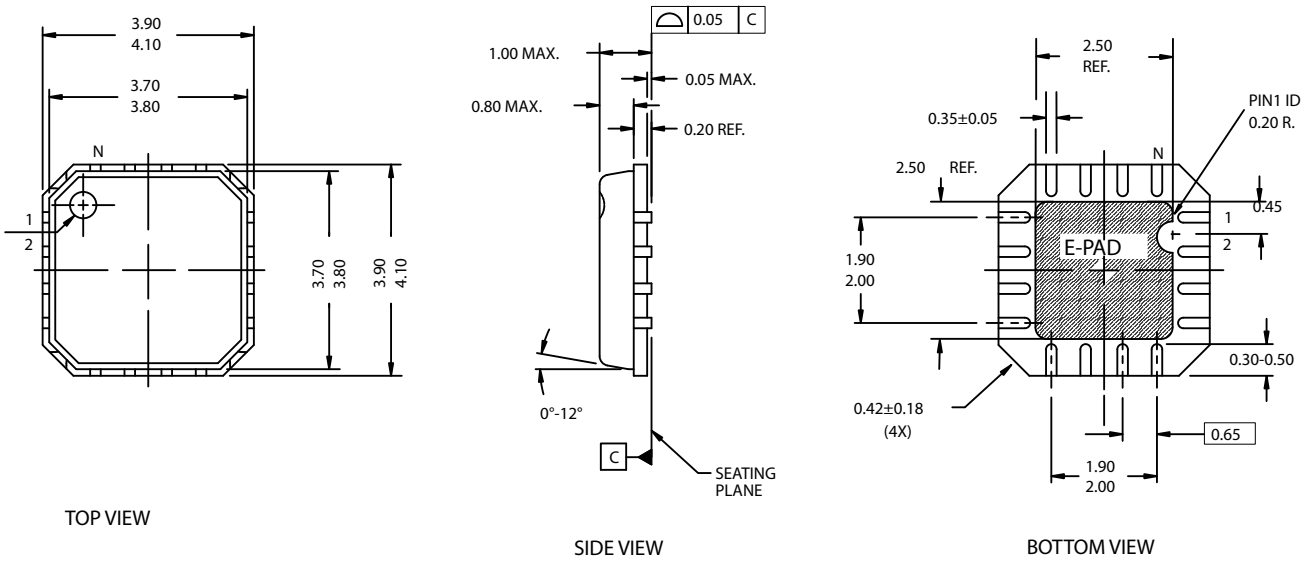


Ordering Information

Ordering Code	Package Marking	Package Name	Package Type	Operating Range
CYV15G0104EQ-LXC	CY21EQ	LY16A	Pb-free 16-Pin QFN	0 to 70°C

Package Dimension

Figure 4. 16-Pin QFN Package LY16A



DIMENSION IN mm MIN.
MAX.

REFERENCE JEDEC MO-220

PKG. WEIGHT 0.04gms

PART #	
LF16A	STANDARD PKG.
LY16A	LEAD FREE PKG.

001-04468-*A

Document History Page

Document Title: CYV15G0104EQ Multi Rate Video Cable Equalizer Document Number: 001-07425				
Rev.	**Ecn No.**	**Issue Date**	**Orig. Of Change**	**Description Of Change**
**	1396423	SEE ECN	UKK/AESA	New datasheet