

Low power dual operational amplifier

Features

- Internally frequency compensated
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1.1MHz (temperature compensated)
- Very low supply current/op (500μA)
- Low input bias current: 20nA (temperature compensated)
- Low input offset current: 2nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to ($V_{CC} - 1.5V$)
- ESD internal protection: 2kV

Description

This circuit consists of two independent, high gain, internally frequency compensated operational-amplifiers, designed specifically for automotive and industrial control system. It operates from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with off the standard +5V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.



N
DIP8
(Plastic package)

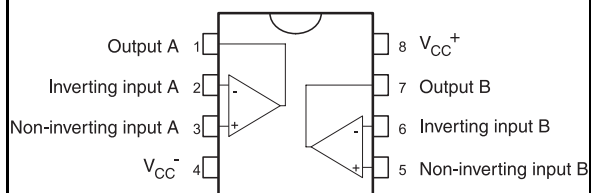


D
SO-8
(Plastic micropackage)



P
TSSOP8
(Thin shrink small outline package)

Pin connections (top view)



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2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+32	V
V_{id}	Differential input voltage	-0.3V to $V_{CC} + 0.3$	V
V_I	Input voltage	-0.3V to $V_{CC} + 0.3$	V
	Output short-circuit duration ⁽¹⁾	Infinite	s
P_{tot}	Power dissipation	500	mW
I_{in}	Input current ⁽²⁾	50	mA
T_{oper}	Operating free-air temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient ^{(3) (4)}		°C/W
	SO-8	125	
	TSSOP8	120	
	DIP-8	85	
R_{thjc}	Thermal resistance junction to case		°C/W
	SO-8	40	
	TSSOP8	37	
	DIP-8	41	
T_{stg}	Storage temperature range	-65 to +150	°C
ESD	HBM: human body model ⁽⁵⁾	2	kV
	MM: machine model ⁽⁶⁾	200	V
	CDM: charged device model ⁽⁷⁾	1.5	kV

1. Short-circuits from the output to V_{CC} can cause excessive heating if $V_{CC}^+ > 15V$. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC} . Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
2. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3V.
3. Short-circuits can cause excessive heating and destructive dissipation.
4. R_{th} are typical values.
5. Human body model: 100pF discharged through a 1.5k Ω resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
6. Machine model: a 200pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
7. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 30	V
V_{icm}	Common mode input voltage range	$V_{CC}^{+} - 1.5$	V

3 Electrical characteristics

Table 3. $V_{CC}^+ = 5V$, $V_{CC}^- = \text{Ground}$, $V_O = 1.4V$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ⁽¹⁾	$T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		2	7 9	mV
I_{io}	Input offset current	$T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		2	30 40	nA
I_{ib}	Input bias current ⁽²⁾	$T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		20	150 200	nA
A_{vd}	Large signal voltage gain	$V_{CC}^+ = +15V$, $R_L = 2k\Omega$, $V_O = 1.4V$ to $11.4V$ $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	50 25	100		V/mV
SVR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$ $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	65 65	100		dB
I_{cc}	Supply current, all Amp, no load	$T_{amb} = 25^\circ C$, $V_{CC} = +5V$ $T_{min} \leq T_{amb} \leq T_{max}$, $V_{CC} = +30V$		0.7	1.2 2	mA
V_{icm}	Input common mode voltage range	$V_{CC} = +30V$ ⁽³⁾ $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	0 0		$V_{CC}^+ - 1.5$ $V_{CC}^+ - 2$	V
CMR	Common-mode rejection ratio	$R_S = 10k\Omega$ $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	70 60	85		dB
I_{source}	Output short-circuit current	$V_{CC} = +15V$, $V_O = +2V$, $V_{id} = +1V$	20	40	60	mA
I_{sink}	Output sink current	$V_O = 2V$, $V_{CC} = +5V$ $V_O = +0.2V$, $V_{CC} = +15V$	10 12	20 50		mA μA
V_{OPP}	Output voltage swing	$R_L = 2k\Omega$ $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	0 0		$V_{CC}^+ - 1.5$ $V_{CC}^+ - 2$	V
V_{OH}	High level output voltage	$V_{CC} + 30V$ $T_{amb} = +25^\circ C$, $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $T_{amb} = +25^\circ C$, $R_L = 10k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$	26 26 27 27	27 28		V
V_{OL}	Low level output voltage	$R_L = 10k\Omega$ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		5	20 20	mV
SR	Slew rate	$V_{CC} = 15V$, $V_i = 0.5$ to $3V$, $R_L = 2k\Omega$ $C_L = 100pF$, unity gain $T_{min} \leq T_{amb} \leq T_{max}$	0.3 0.2	0.6		V/ μs
GBP	Gain bandwidth product	$f = 100kHz$, $V_{CC} = 30V$, $V_{in} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$	0.7	1.1		MHz

Table 3. $V_{CC}^+ = 5V$, $V_{CC}^- = \text{Ground}$, $V_O = 1.4V$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
THD	Total harmonic distortion	$f = 1\text{kHz}$, $A_V = 20\text{dB}$, $R_L = 2\text{k}\Omega$, $V_O = 2\text{Vpp}$, $C_L = 100\text{pF}$, $V_{CC} = 30V$		0.02		%
DV_{io}	Input offset voltage drift			7	30	$\mu V/^\circ C$
DI_{io}	Input offset current drift			10	300	$\text{pA}/^\circ C$
V_{O1}/V_{O2}	Channel separation ⁽⁴⁾	$1\text{kHz} \leq f \leq 20\text{kHz}$		120		dB

- $V_O = 1.4V$, $R_S = 0\Omega$, $5V < V_{CC}^+ < 30V$, $0V < V_{ic} < V_{CC}^+ - 1.5V$
- The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so there is no change in the loading charge on the input lines.
- The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC}^+ - 1.5V$, but either or both inputs can go to +32V without damage.
- Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling. Typically, this can be detected because this type of capacitance increases at higher frequencies.

Figure 2. Open loop frequency response

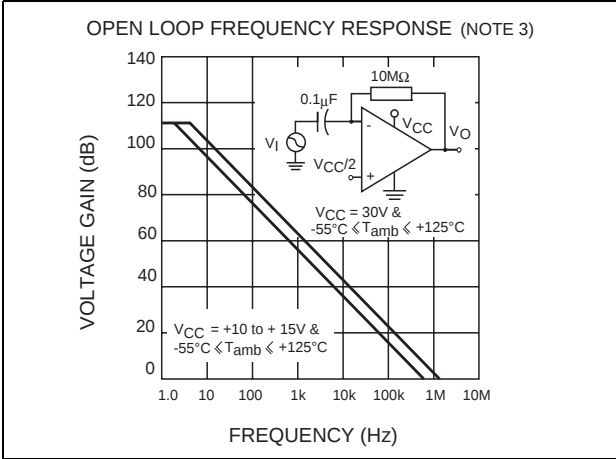


Figure 3. Large signal frequency response

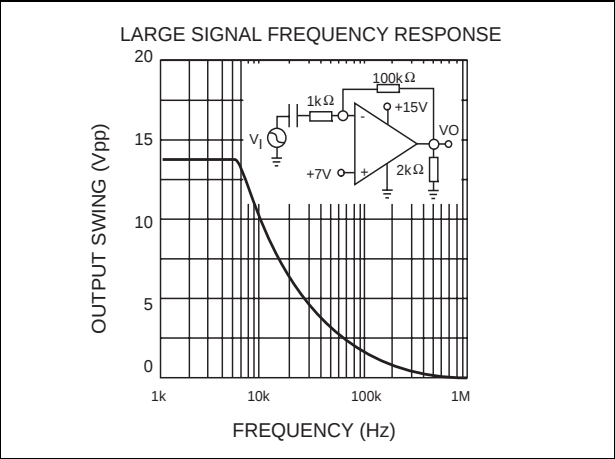


Figure 4. Voltage follower pulse response

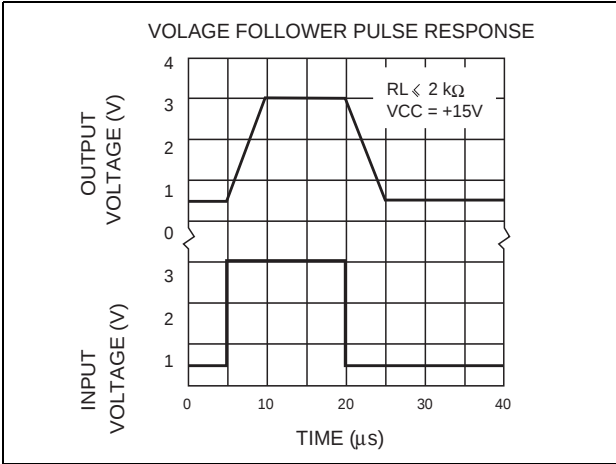


Figure 5. Output characteristics

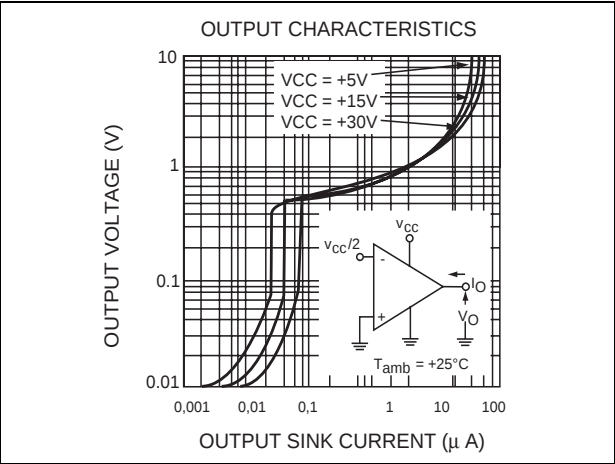


Figure 6. Voltage follower pulse response

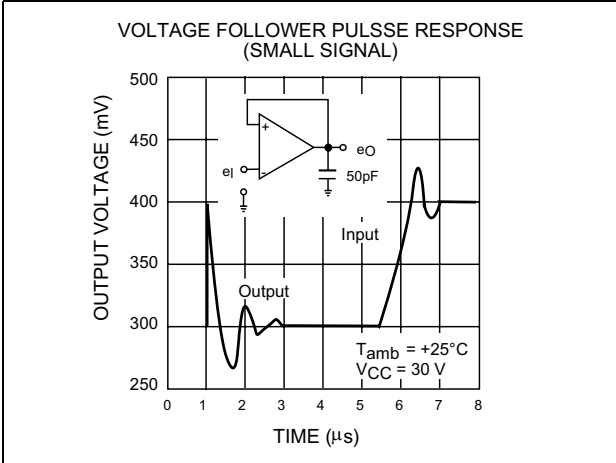


Figure 7. Output characteristics

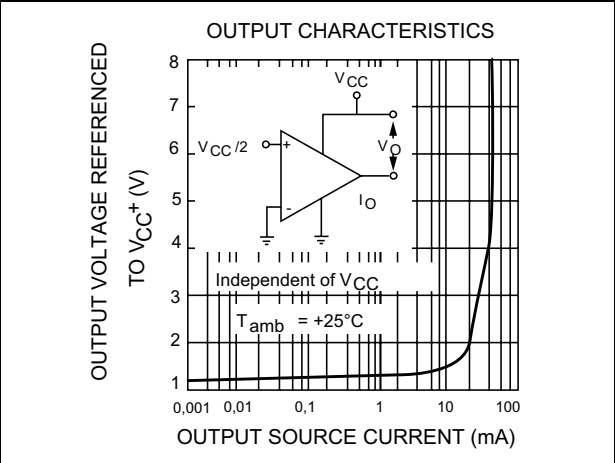


Figure 8. Input current

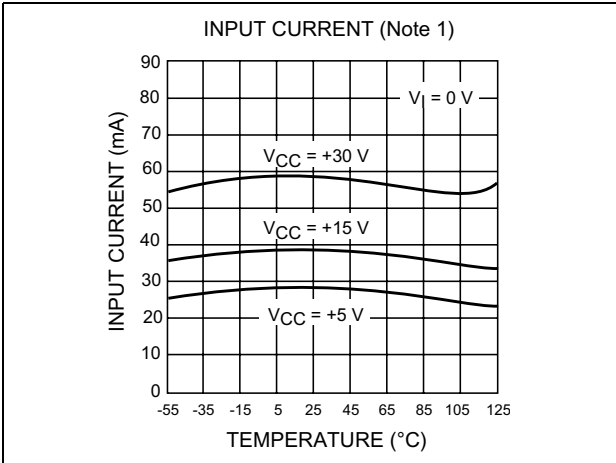


Figure 9. Current limiting

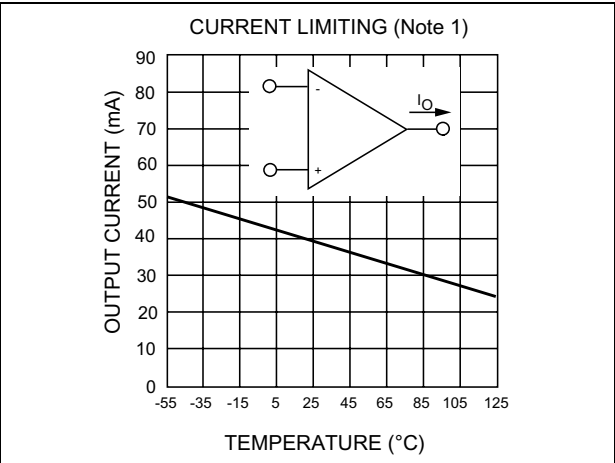


Figure 10. Input voltage range

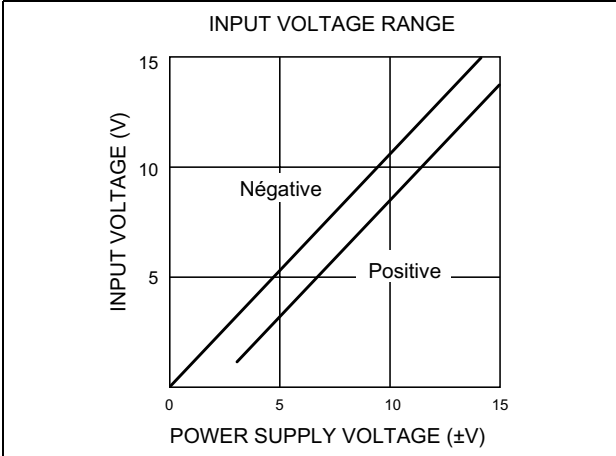


Figure 11. Supply current

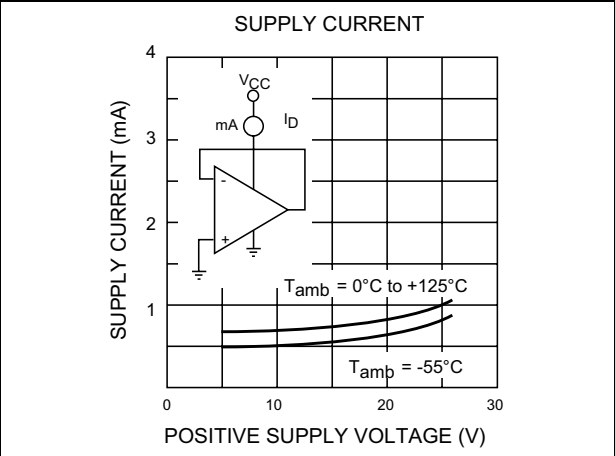


Figure 12. Positive supply voltage

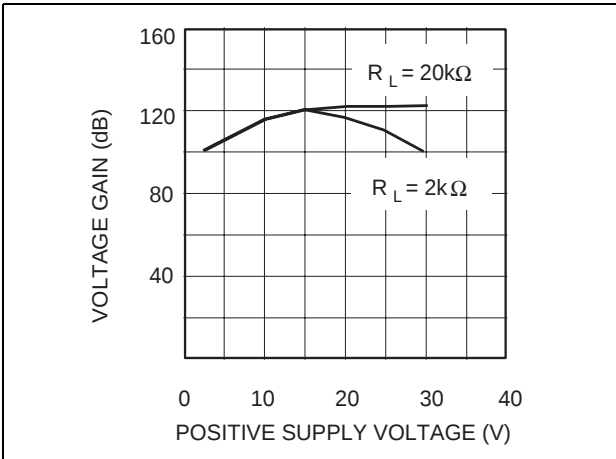


Figure 13. Positive supply voltage

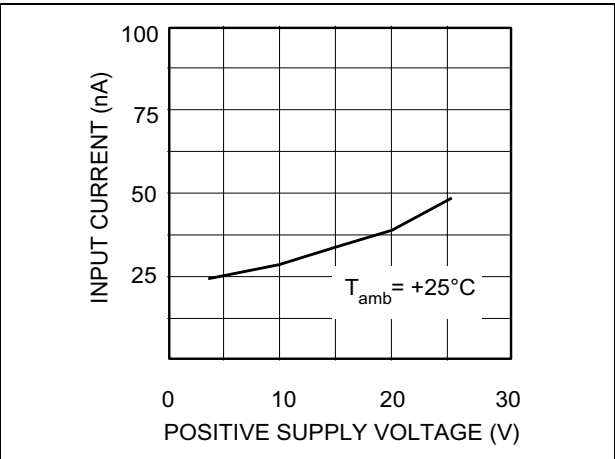


Figure 14. Positive supply voltage

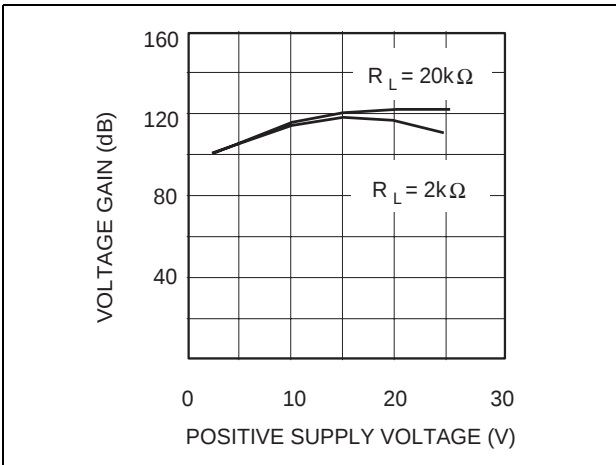


Figure 15. Gain bandwidth product

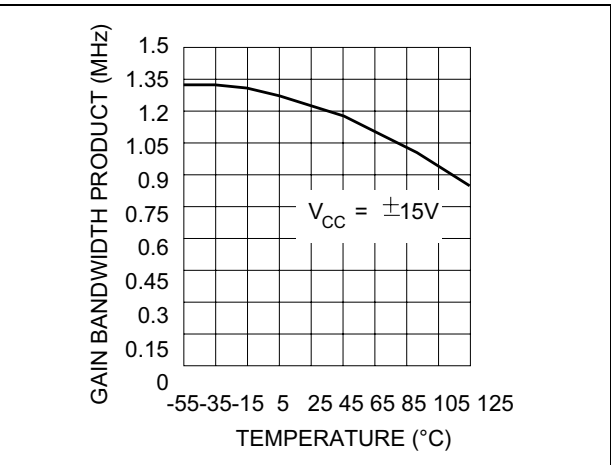


Figure 16. Power supply rejection ratio

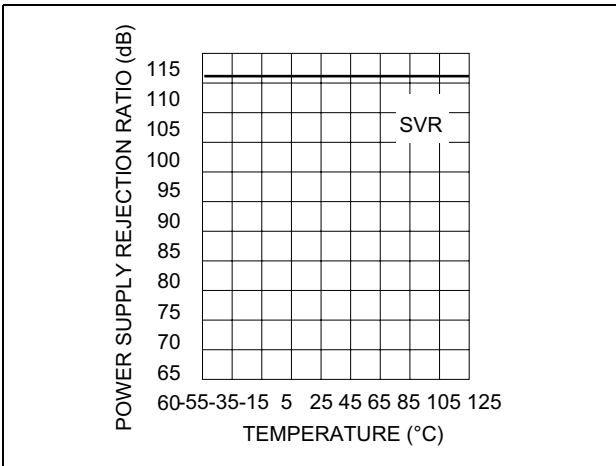


Figure 17. Common mode rejection ratio

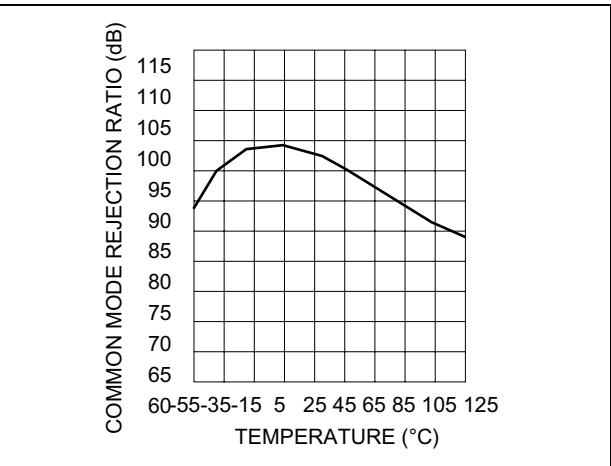
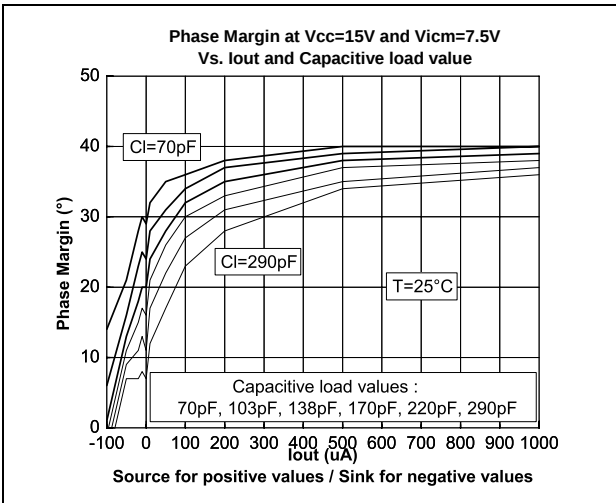


Figure 18. Phase margin vs capacitive load



Typical single-supply applications

Figure 19. AC coupled inverting amplifier

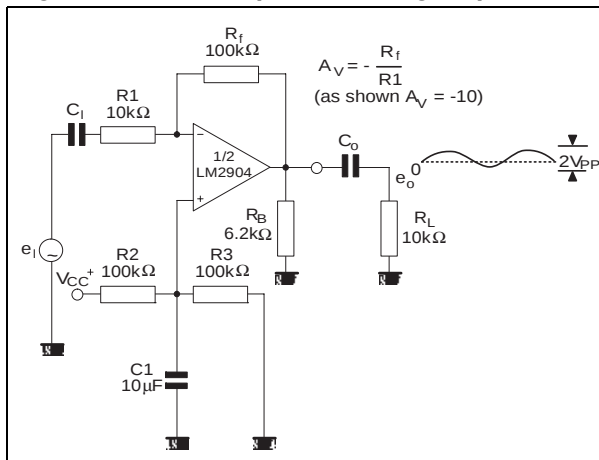


Figure 20. AC coupled non-inverting amplifier

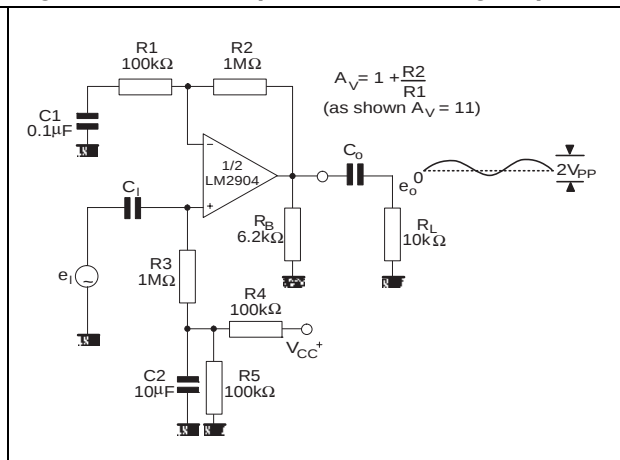


Figure 21. Non-inverting DC gain

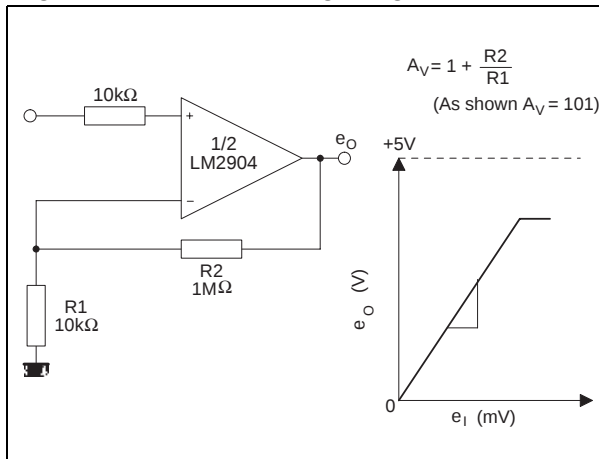


Figure 22. DC summing amplifier

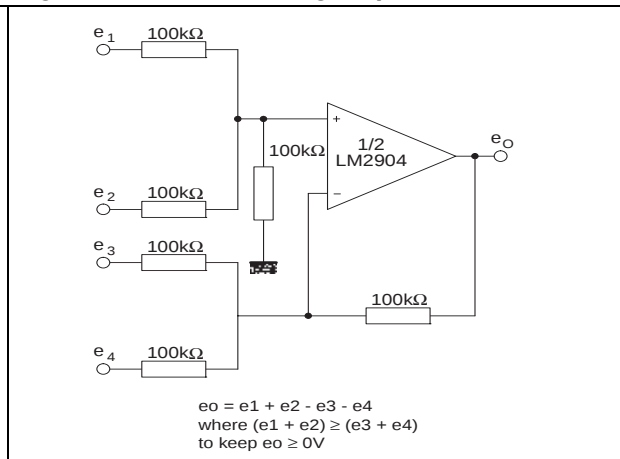


Figure 23. High input Z, DC differential amplifier

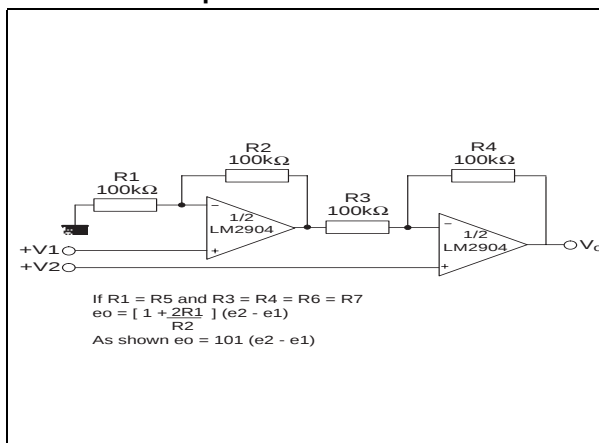


Figure 24. Using symmetrical amplifiers to reduce input current

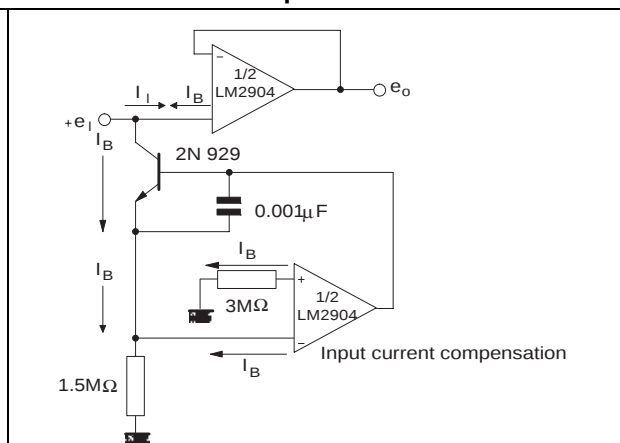


Figure 25. Low drift peak detector

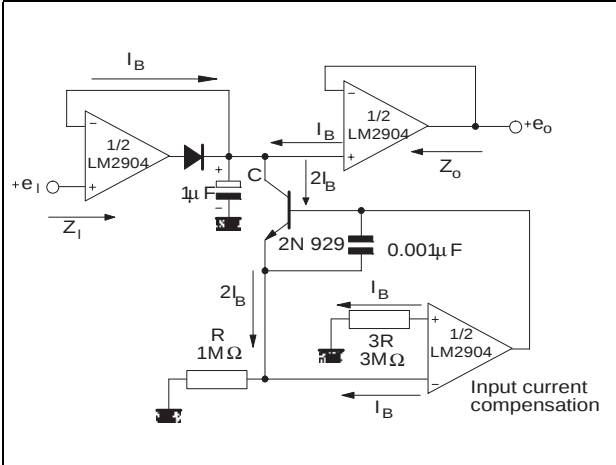
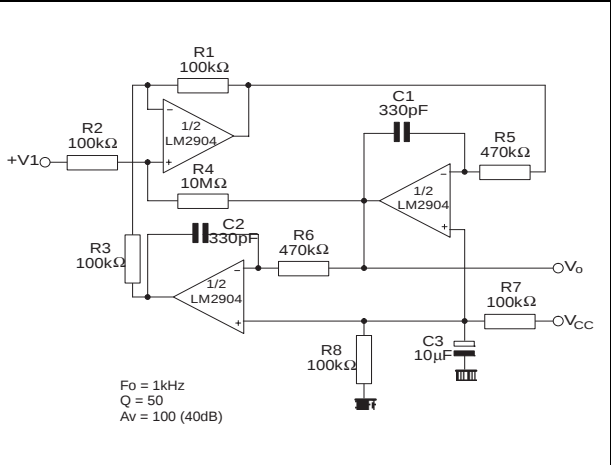


Figure 26. Active bandpass filter



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4.1 SO-8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04

4.2 DIP8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.3			0.130	
a1	0.7			0.28		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.20
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

The image contains three mechanical drawings of the DIP8 package. The top-left drawing is a side view showing dimensions A, a1, B, B1, b, b1, e, e3, e4, F, I, L, and Z. The top-right drawing is an end view showing dimensions e4 and b1. The bottom drawing is a top view showing dimensions D, L, and pin numbers 1, 4, 5, and 8.

4.3 TSSOP8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	

The mechanical drawing illustrates the TSSOP8 package from three perspectives: top, side, and end views. The top view shows the package body with dimensions A (width), A1 (lead width), A2 (lead spacing), b (lead thickness), c (lead height), D (body width), E (body length), E1 (lead length), e (pitch), K (lead angle), L (lead length), and L1 (lead length). The side view shows the package height and the lead profile. The end view shows the package width and the lead profile. A callout indicates a gage plane at 0.25 mm (.010 inch) from the lead tip. A note 'PIN 1 IDENTIFICATION' points to a specific pin on the package.

5 Ordering information

Part number	Temperature range	Package	Packing	Marking
LM2904WN	-40°C, +125°C	DIP8	Tube	LM2904W
LM2904WD/WDT		SO-8	Tube or tape & reel	2904W
LM2904WPT		TSSOP8 (Thin shrink outline package)	Tape & reel	2904W
LM2904WYD/WYDT		SO-8 (automotive grade level)	Tube or tape & reel	2904WY
LM2904WYPT		TSSOP8 (automotive grade level)	Tape & reel	K04WY

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
1-Sep-2003	1	Initial release.
1-Jul-2005	2	PPAP references inserted in the datasheet see Section 5: Ordering information on page 17 . ESD protection inserted in Table 1: Absolute maximum ratings on page 4 .
1-Oct-2005	3	Correction of error in AVD min. value see: Table 3. on page 6
1-Dec-2005	4	LM2904WYPT PPAP reference added in Section 5: Ordering information on page 17 . Information added in Table 1: Absolute maximum ratings on page 4 .
2-May-2006	5	Minimum value of Slew Rate at 25°C and in temperature added in Table 3. on page 6 .
29-Sep-2006	6	ESD tolerance for HBM model improved to 2kV in Table 3. on page 6 . Added Figure 18: Phase margin vs capacitive load on page 10 .

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