

### FEATURES

- 1.5 pF off capacitance
- 0.5 pC charge injection
- 33 V supply range
- 120  $\Omega$  on resistance
- Fully specified at  $\pm 15$  V/+12 V
- 3 V logic-compatible inputs
- Rail-to-rail operation
- Break-before-make switching action
- 16-lead TSSOP, 20-lead TSSOP, and 4 mm  $\times$  4 mm LFCSP
- Typical power consumption ( $<0.03$   $\mu$ W)

### APPLICATIONS

- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Communication systems

### GENERAL DESCRIPTION

The ADG1233 and ADG1234 are monolithic *i*CMOS analog switches comprising three independently selectable single-pole, double throw SPDT switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. An  $\overline{\text{EN}}$  input on the ADG1233 and ADG1234 is used to enable or disable the device. When disabled, all channels are switched off.

The *i*CMOS (industrial-CMOS) modular manufacturing process combines a high voltage complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lowered power consumption, and reduced package size.

The ultralow capacitance and charge injection of these multiplexers make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required.

#### Rev. A

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### FUNCTIONAL BLOCK DIAGRAMS

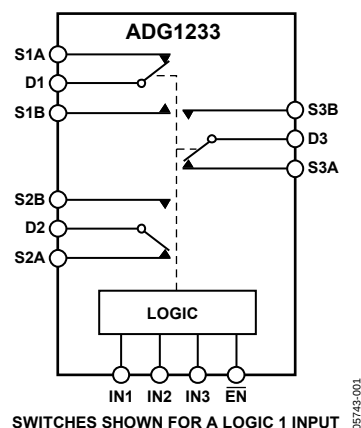


Figure 1.

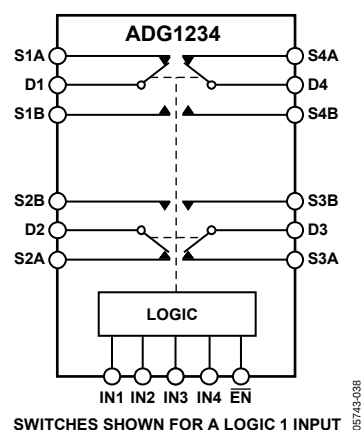


Figure 2.

Fast switching speed coupled with high signal bandwidth make the parts suitable for video signal switching. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

### PRODUCT HIGHLIGHTS

1. 1.5 pF off capacitance ( $\pm 15$  V supply).
2. 0.5 pC charge injection.
3. 3 V logic-compatible digital input,  $V_{IH} = 2.0$  V,  $V_{IL} = 0.8$  V.
4. 16-lead TSSOP, 20-lead TSSOP, and 4 mm  $\times$  4 mm LFCSP.

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REVISION HISTORY

8/06—Rev. 0 to Rev. A

|                           |           |
|---------------------------|-----------|
| Updated Format.....       | Universal |
| Changes to Table 1.....   | 3         |
| Changes to Table 2.....   | 4         |
| Changes to Figure 11..... | 10        |
| Changes to Figure 12..... | 11        |

1/06—Revision 0: Initial Version

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 1.

| Parameter                                                | Y Version <sup>1</sup> |                |                                    | Unit    | Test Conditions/Comments                                                                                                                                                |
|----------------------------------------------------------|------------------------|----------------|------------------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                          | +25°C                  | −40°C to +85°C | −40°C to +125°C                    |         |                                                                                                                                                                         |
| ANALOG SWITCH                                            |                        |                |                                    |         |                                                                                                                                                                         |
| Analog Signal Range                                      |                        |                | V <sub>SS</sub> to V <sub>DD</sub> | V       | V <sub>S</sub> = ±10 V, I <sub>S</sub> = −1 mA; see Figure 24<br>V <sub>DD</sub> = +13.5 V, V <sub>SS</sub> = −13.5 V<br>V <sub>S</sub> = ±10 V, I <sub>S</sub> = −1 mA |
| On Resistance (R <sub>ON</sub> )                         | 120                    |                |                                    | Ω typ   |                                                                                                                                                                         |
|                                                          | 190                    | 230            | 260                                | Ω max   |                                                                                                                                                                         |
| On Resistance Match Between Channels (ΔR <sub>ON</sub> ) | 3.5                    |                |                                    | Ω typ   |                                                                                                                                                                         |
|                                                          | 6                      | 10             | 12                                 | Ω max   | V <sub>S</sub> = −5 V, 0 V, +5 V; I <sub>S</sub> = −1 mA                                                                                                                |
| On Resistance Flatness (R <sub>FLAT (ON)</sub> )         | 20                     |                |                                    | Ω typ   |                                                                                                                                                                         |
|                                                          | 60                     | 72             | 79                                 | Ω max   |                                                                                                                                                                         |
| LEAKAGE CURRENTS                                         |                        |                |                                    |         |                                                                                                                                                                         |
| Source Off Leakage I <sub>S</sub> (Off)                  | ±0.02                  |                |                                    | nA typ  | V <sub>DD</sub> = +16.5 V, V <sub>SS</sub> = −16.5 V<br>V <sub>D</sub> = ±10 V, V <sub>S</sub> = −10 V; see Figure 25                                                   |
|                                                          | ±0.1                   | ±0.6           | ±1                                 | nA max  |                                                                                                                                                                         |
| Drain Off Leakage I <sub>D</sub> (Off)                   | ±0.02                  |                |                                    | nA typ  | V <sub>S</sub> = 1 V/10 V, V <sub>D</sub> = 10 V/1 V;<br>see Figure 25                                                                                                  |
|                                                          | ±0.1                   | ±0.6           | ±1                                 | nA max  |                                                                                                                                                                         |
| Channel On Leakage I <sub>D</sub> , I <sub>S</sub> (On)  | ±0.02                  |                |                                    | nA typ  | V <sub>S</sub> = V <sub>D</sub> = ±10 V; see Figure 26                                                                                                                  |
|                                                          | ±0.2                   | ±0.6           | ±1                                 | nA max  |                                                                                                                                                                         |
| DIGITAL INPUTS                                           |                        |                |                                    |         |                                                                                                                                                                         |
| Input High Voltage, V <sub>INH</sub>                     |                        |                | 2.0                                | V min   | V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>                                                                                                                  |
| Input Low Voltage, V <sub>INL</sub>                      |                        |                | 0.8                                | V max   |                                                                                                                                                                         |
| Input Current                                            |                        |                |                                    |         |                                                                                                                                                                         |
| I <sub>INL</sub> or I <sub>INH</sub>                     | ±0.005                 |                |                                    | μA typ  |                                                                                                                                                                         |
|                                                          |                        |                | ±0.1                               | μA max  |                                                                                                                                                                         |
| Digital Input Capacitance, C <sub>IN</sub>               | 3                      |                |                                    | pF typ  |                                                                                                                                                                         |
| DYNAMIC CHARACTERISTICS <sup>2</sup>                     |                        |                |                                    |         |                                                                                                                                                                         |
| t <sub>TRANSITION</sub>                                  | 110                    |                |                                    | ns typ  | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>V <sub>S</sub> = 10 V; see Figure 27                                                                                  |
|                                                          | 130                    | 150            | 170                                | ns max  |                                                                                                                                                                         |
| t <sub>BBM</sub>                                         | 25                     |                |                                    | ns typ  | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>V <sub>S1</sub> = V <sub>S2</sub> = +10 V; see Figure 28                                                              |
|                                                          |                        |                | 10                                 | ns min  |                                                                                                                                                                         |
| t <sub>ON</sub> ( $\overline{\text{EN}}$ )               | 120                    |                |                                    | ns typ  | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>V <sub>S</sub> = 10 V; see Figure 29                                                                                  |
|                                                          | 140                    | 170            | 195                                | ns max  |                                                                                                                                                                         |
| t <sub>OFF</sub> ( $\overline{\text{EN}}$ )              | 40                     |                |                                    | ns typ  | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>V <sub>S</sub> = 10 V; see Figure 29                                                                                  |
|                                                          | 45                     | 55             | 60                                 | ns max  |                                                                                                                                                                         |
| Charge Injection                                         | 0.5                    |                |                                    | pC typ  | V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF;<br>see Figure 30                                                                                     |
| Off Isolation                                            | −80                    |                |                                    | dB typ  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; see<br>Figure 31                                                                                               |
| Channel-to-Channel Crosstalk                             | −85                    |                |                                    | dB typ  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz;<br>see Figure 33                                                                                               |
| Total Harmonic Distortion, THD + N                       | 0.14                   |                |                                    | % typ   | R <sub>L</sub> = 10 kΩ, 5 V rms, f = 20 Hz to<br>20 kHz; see Figure 34                                                                                                  |
| −3 dB Bandwidth                                          | 900                    |                |                                    | MHz typ | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF; see Figure 32                                                                                                             |
| C <sub>S</sub> (Off)                                     | 1.5                    |                |                                    | pF typ  |                                                                                                                                                                         |
|                                                          | 1.7                    |                |                                    | pF max  | f = 1 MHz; V <sub>S</sub> = 0 V                                                                                                                                         |
| C <sub>D</sub> (Off)                                     | 1.6                    |                |                                    | pF typ  | f = 1 MHz; V <sub>S</sub> = 0 V                                                                                                                                         |
|                                                          | 1.8                    |                |                                    | pF max  | f = 1 MHz; V <sub>S</sub> = 0 V                                                                                                                                         |
| C <sub>D</sub> , C <sub>S</sub> (On)                     | 3.5                    |                |                                    | pF typ  | f = 1 MHz; V <sub>S</sub> = 0 V                                                                                                                                         |
|                                                          | 4                      |                |                                    | pF max  | f = 1 MHz; V <sub>S</sub> = 0 V                                                                                                                                         |

# ADG1233/ADG1234

| Parameter          | Y Version <sup>1</sup> |                |                  | Unit                                   | Test Conditions/Comments                              |
|--------------------|------------------------|----------------|------------------|----------------------------------------|-------------------------------------------------------|
|                    | +25°C                  | –40°C to +85°C | –40°C to +125°C  |                                        |                                                       |
| POWER REQUIREMENTS |                        |                |                  |                                        | $V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ |
| $I_{DD}$           | 0.002                  |                | 1.0              | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 0 V or $V_{DD}$                      |
| $I_{DD}$           | 260                    |                | 420              | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 5 V                                  |
| $I_{SS}$           | 0.002                  |                | 1.0              | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 0 V or $V_{DD}$                      |
| $I_{SS}$           | 0.002                  |                | 1.0              | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 5 V                                  |
| $V_{DD}/V_{SS}$    |                        |                | $\pm 5/\pm 16.5$ | V min/max                              | GND = 0 V                                             |

<sup>1</sup> Temperature range for the Y version: –40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

**SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

| Parameter                                                | Y Version <sup>1</sup> |                |                      | Unit                       | Test Conditions/Comments                                                                                                |
|----------------------------------------------------------|------------------------|----------------|----------------------|----------------------------|-------------------------------------------------------------------------------------------------------------------------|
|                                                          | +25°C                  | –40°C to +85°C | –40°C to +125°C      |                            |                                                                                                                         |
| ANALOG SWITCH                                            |                        |                |                      |                            |                                                                                                                         |
| Analog Signal Range                                      |                        |                | 0 to V <sub>DD</sub> | V                          |                                                                                                                         |
| On Resistance (R <sub>ON</sub> )                         | 300                    |                |                      | Ω typ                      | V <sub>S</sub> = 0 V to 10 V, I <sub>S</sub> = –1 mA; see Figure 24                                                     |
| On Resistance Match Between Channels (ΔR <sub>ON</sub> ) | 475<br>5               | 567            | 625                  | Ω max<br>Ω typ             | V <sub>DD</sub> = 10.8 V, V <sub>SS</sub> = 0 V<br>V <sub>S</sub> = 0 V to 10 V, I <sub>S</sub> = –1 mA                 |
| On Resistance Flatness (R <sub>FLAT (ON)</sub> )         | 16<br>60               | 26             | 27                   | Ω max<br>Ω typ             | V <sub>S</sub> = 3 V, 6 V, 9 V, I <sub>S</sub> = –1 mA                                                                  |
| LEAKAGE CURRENTS                                         |                        |                |                      |                            |                                                                                                                         |
| Source Off Leakage I <sub>S</sub> (Off)                  | ±0.02                  |                |                      | nA typ                     | V <sub>DD</sub> = 13.2 V<br>V <sub>S</sub> = 1 V/10 V, V <sub>D</sub> = 10 V/1 V; see Figure 25                         |
| Drain Off Leakage I <sub>D</sub> (Off)                   | ±0.1<br>±0.02          | ±0.6           | ±1                   | nA max<br>nA typ           | V <sub>S</sub> = 1 V/10 V, V <sub>D</sub> = 10 V/1 V; see Figure 25                                                     |
| Channel On Leakage I <sub>D</sub> , I <sub>S</sub> (On)  | ±0.1<br>±0.02<br>±0.2  | ±0.6           | ±1                   | nA max<br>nA typ<br>nA max | V <sub>S</sub> = V <sub>D</sub> = 1 V or 10 V, see Figure 26                                                            |
| DIGITAL INPUTS                                           |                        |                |                      |                            |                                                                                                                         |
| Input High Voltage, V <sub>INH</sub>                     |                        |                | 2.0                  | V min                      |                                                                                                                         |
| Input Low Voltage, V <sub>INL</sub>                      |                        |                | 0.8                  | V max                      |                                                                                                                         |
| Input Current, I <sub>INL</sub> or I <sub>INH</sub>      | ±0.001                 |                | ±0.1                 | μA typ<br>μA max           | V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>                                                                  |
| Digital Input Capacitance, C <sub>IN</sub>               | 2                      |                |                      | pF typ                     |                                                                                                                         |
| DYNAMIC CHARACTERISTICS <sup>2</sup>                     |                        |                |                      |                            |                                                                                                                         |
| t <sub>TRANSITION</sub>                                  | 135<br>170             | 200            | 230                  | ns typ                     | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>V <sub>S</sub> = 8 V; see Figure 27                                   |
| t <sub>BBM</sub>                                         | 45                     |                | 10                   | ns typ<br>ns min           | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>V <sub>S1</sub> = V <sub>S2</sub> = 8 V; see Figure 28                |
| t <sub>ON</sub> ( $\overline{\text{EN}}$ )               | 150                    |                |                      | ns typ                     | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>V <sub>S</sub> = 8 V; see Figure 29                                   |
| t <sub>OFF</sub> ( $\overline{\text{EN}}$ )              | 195<br>45              | 230            | 265                  | ns typ                     | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>V <sub>S</sub> = 8 V; see Figure 29                                   |
| Charge Injection                                         | 60<br>–0.3             | 70             | 75                   | pC typ                     | V <sub>S</sub> = 8 V; see Figure 29<br>V <sub>S</sub> = 6 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF; see Figure 30 |
| Off Isolation                                            | –80                    |                |                      | dB typ                     | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; see Figure 31                                                  |
| Channel-to-Channel Crosstalk                             | –85                    |                |                      | dB typ                     | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; see Figure 33                                                  |
| –3 dB Bandwidth                                          | 600                    |                |                      | MHz typ                    | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF; see Figure 32                                                             |
| C <sub>S</sub> (Off)                                     | 1.5<br>1.7             |                |                      | pF typ<br>pF max           | f = 1 MHz; V <sub>S</sub> = 6 V<br>f = 1 MHz; V <sub>S</sub> = 6 V                                                      |
| C <sub>D</sub> (Off)                                     | 2<br>2.2               |                |                      | pF typ<br>pF max           | f = 1 MHz; V <sub>S</sub> = 6 V<br>f = 1 MHz; V <sub>S</sub> = 6 V                                                      |
| C <sub>D</sub> , C <sub>S</sub> (On)                     | 4<br>4.5               |                |                      | pF typ<br>pF max           | f = 1 MHz; V <sub>S</sub> = 6 V<br>f = 1 MHz; V <sub>S</sub> = 6 V                                                      |

# ADG1233/ADG1234

| Parameter          | Y Version <sup>1</sup> |                |                 | Unit             | Test Conditions/Comments                                            |
|--------------------|------------------------|----------------|-----------------|------------------|---------------------------------------------------------------------|
|                    | +25°C                  | –40°C to +85°C | –40°C to +125°C |                  |                                                                     |
| POWER REQUIREMENTS |                        |                |                 |                  |                                                                     |
| I <sub>DD</sub>    | 0.002                  |                | 1.0             | μA typ<br>μA max | V <sub>DD</sub> = 13.2 V<br>Digital inputs = 0 V or V <sub>DD</sub> |
| I <sub>DD</sub>    | 260                    |                | 440             | μA typ<br>μA max | Digital inputs = 5 V                                                |
| V <sub>DD</sub>    |                        |                | 5/16.5          | V min/max        | V <sub>SS</sub> = 0 V, GND = 0 V                                    |

<sup>1</sup> Temperature range for the Y version: –40°C to +125°C

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

| Parameter                                                       | Rating                                                                                    |
|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| $V_{DD}$ to $V_{SS}$                                            | 35 V                                                                                      |
| $V_{DD}$ to GND                                                 | –0.3 V to +25 V                                                                           |
| $V_{SS}$ to GND                                                 | +0.3 V to –25 V                                                                           |
| Analog, Digital Inputs <sup>1</sup>                             | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or<br>30 mA, whichever<br>occurs first |
| Continuous Current, S or D                                      | 24 mA                                                                                     |
| Peak Current, S or D (Pulsed at<br>1 ms, 10% Duty Cycle Mximum) | 100 mA                                                                                    |
| Operating Temperature Range                                     |                                                                                           |
| Automotive Temperature Range<br>(Y Version)                     | –40°C to +125°C                                                                           |
| Storage Temperature Range                                       | –65°C to +150°C                                                                           |
| Junction Temperature                                            | 150°C                                                                                     |
| TSSOP, $\theta_{JA}$ , Thermal Impedance                        | 112°C/W                                                                                   |
| LFCSP, $\theta_{JA}$ , Thermal Impedance                        | 30.4°C/W                                                                                  |
| Reflow Soldering Peak Temperature,<br>Pb-Free                   | 260°C                                                                                     |

<sup>1</sup> Overvoltages at A,  $\overline{EN}$ , S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating is applied at any one time.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# ADG1233/ADG1234

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

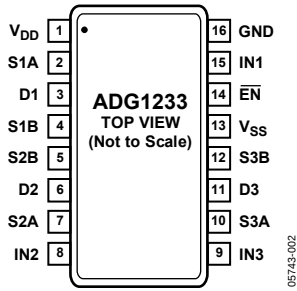


Figure 3. 16-Lead TSSOP Pin Configuration

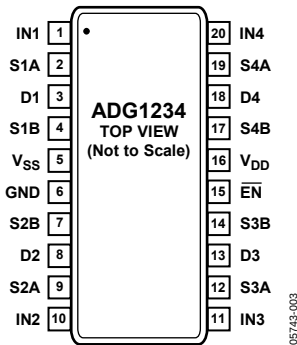


Figure 4. 20-Lead TSSOP Pin Configuration

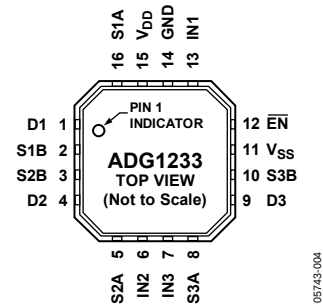


Figure 5. 16-Lead, 4 mm x 4 mm LFCSP Pin Configuration, Exposed Pad Tied to Substrate, V<sub>SS</sub>

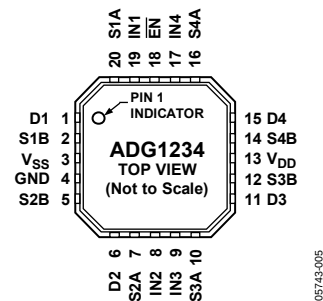


Figure 6. 20-Lead, 4 mm x 4 mm LFCSP Pin Configuration, Exposed Pad Tied to Substrate, V<sub>SS</sub>

Table 4. 16-Lead TSSOP/20-Lead TSSOP Pin Configurations

| Pin No. ADG1233<br>16-Lead TSSOP | Pin No. ADG1234<br>20-Lead TSSOP | Mnemonic        |
|----------------------------------|----------------------------------|-----------------|
| 1                                | 16                               | V <sub>DD</sub> |
| 2                                | 2                                | S1A             |
| 3                                | 3                                | D1              |
| 4                                | 4                                | S1B             |
| 5                                | 7                                | S2B             |
| 6                                | 8                                | D2              |
| 7                                | 9                                | S2A             |
| 8                                | 10                               | IN2             |
| 9                                | 11                               | IN3             |
| 10                               | 12                               | S3A             |
| 11                               | 13                               | D3              |
| 12                               | 14                               | S3B             |
| 13                               | 5                                | V <sub>SS</sub> |
| 14                               | 15                               | EN              |
| 15                               | 1                                | IN1             |
| 16                               | 6                                | GND             |
| N/A                              | 17                               | S4B             |
| N/A                              | 18                               | D4              |
| N/A                              | 19                               | S4A             |
| N/A                              | 20                               | IN4             |

Table 5. 16-Lead LFCSP/20-Lead LFCSP Pin Configurations

| Pin No. ADG1233<br>16-Lead LFCSP | Pin No. ADG1234<br>20-Lead LFCSP | Mnemonic        |
|----------------------------------|----------------------------------|-----------------|
| 1                                | 1                                | D1              |
| 2                                | 2                                | S1B             |
| 3                                | 5                                | S2B             |
| 4                                | 6                                | D2              |
| 5                                | 7                                | S2A             |
| 6                                | 8                                | IN2             |
| 7                                | 9                                | IN3             |
| 8                                | 10                               | S3A             |
| 9                                | 11                               | D3              |
| 10                               | 12                               | S3B             |
| 11                               | 3                                | V <sub>SS</sub> |
| 12                               | 18                               | EN              |
| 13                               | 19                               | IN1             |
| 14                               | 4                                | GND             |
| 15                               | 13                               | V <sub>DD</sub> |
| 16                               | 20                               | S1A             |
| N/A                              | 14                               | S4B             |
| N/A                              | 15                               | D4              |
| N/A                              | 16                               | S4A             |
| N/A                              | 17                               | IN4             |

Table 6. ADG1233/ADG1234 Truth Table

| EN | IN <sub>x</sub> | Switch xA | Switch xB |
|----|-----------------|-----------|-----------|
| 1  | X               | Off       | Off       |
| 0  | 0               | Off       | On        |
| 0  | 1               | On        | Off       |

## TERMINOLOGY

$V_{DD}$

Most positive supply potential.

$V_{SS}$

Most negative power supply potential in dual supplies. In single-supply applications, it can be connected to ground.

**GND**

Ground (0 V) reference.

$R_{ON}$

Ohmic resistance between D and S.

$\Delta R_{ON}$

Difference between the  $R_{ON}$  of any two channels.

$I_S$  (Off)

Source leakage current when switch is off.

$I_D$  (Off)

Drain leakage current when switch is off.

$I_D, I_S$  (On)

Channel leakage current when switch is on.

$V_D, V_S$

Analog voltage on Terminal D, Terminal S.

$C_S$  (Off)

Channel input capacitance for off condition.

$C_D$  (Off)

Channel output capacitance for off condition.

$C_D, C_S$  (On)

On switch capacitance.

$C_{IN}$

Digital input capacitance.

$t_{ON}(\overline{EN})$

Delay time between the 50% and 90% points of the digital input and switch on condition.

$t_{OFF}(\overline{EN})$

Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

$t_{BBM}$

Off time measured between the 80% point of both switches when switching from one address state to another.

$V_{INL}$

Maximum input voltage for Logic 0.

$V_{INH}$

Minimum input voltage for Logic 1.

$I_{INL}, I_{INH}$

Input current of the digital input.

$I_{DD}$

Positive supply current.

$I_{SS}$

Negative supply current.

**Off Isolation**

A measure of an unwanted signal coupling through an off channel.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

**Bandwidth**

Frequency at which the output is attenuated by 3 dB.

**On Response**

Frequency response of the on switch.

**THD + N**

Ratio of the harmonic amplitude plus noise of the signal to the fundamental.

## TYPICAL PERFORMANCE CHARACTERISTICS

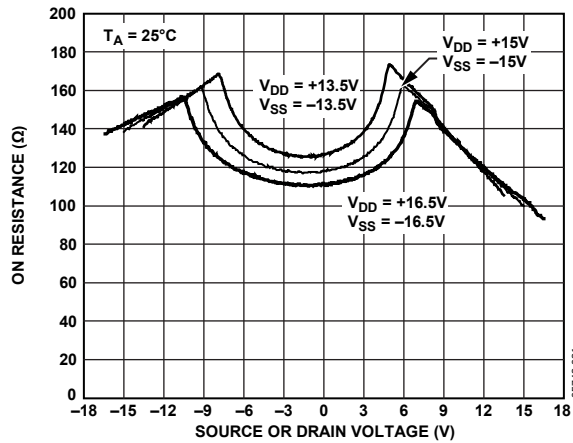


Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

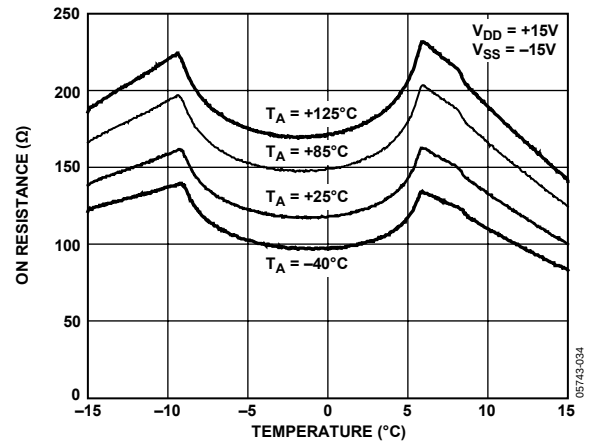


Figure 10. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Dual Supply

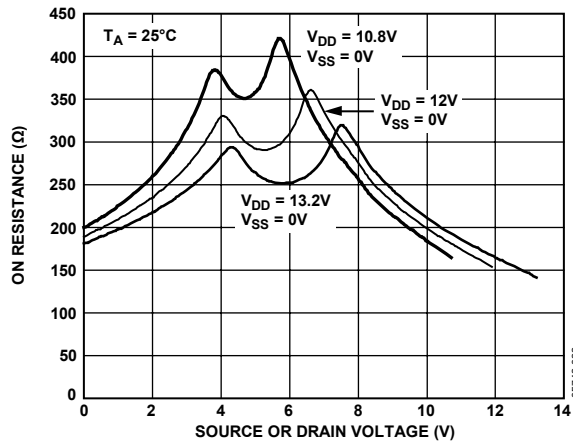


Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

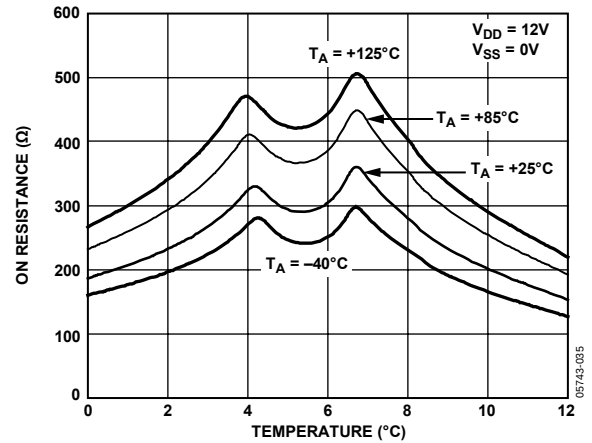


Figure 11. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single Supply

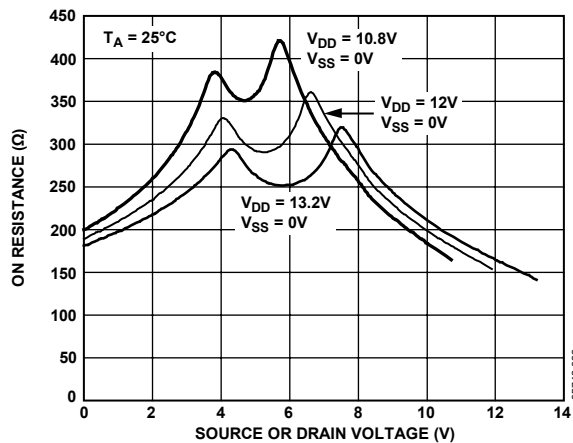


Figure 9. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

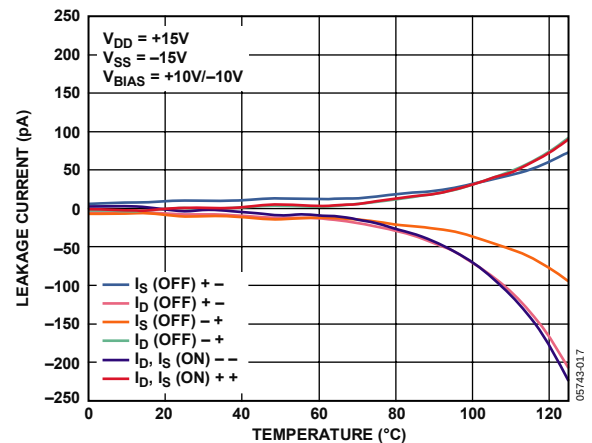


Figure 12. Leakage Currents as a Function of Temperature, Dual Supply

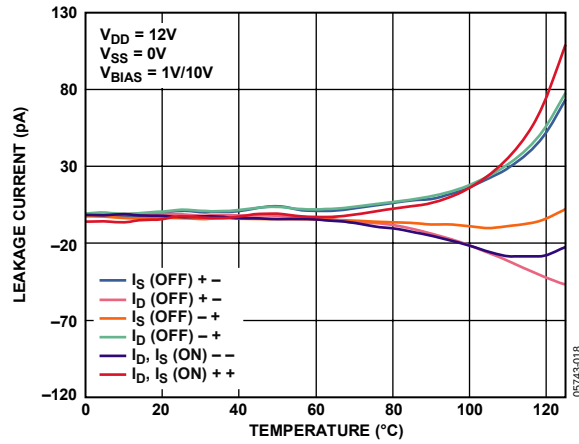


Figure 13. Leakage Currents as a Function of Temperature, Single Supply

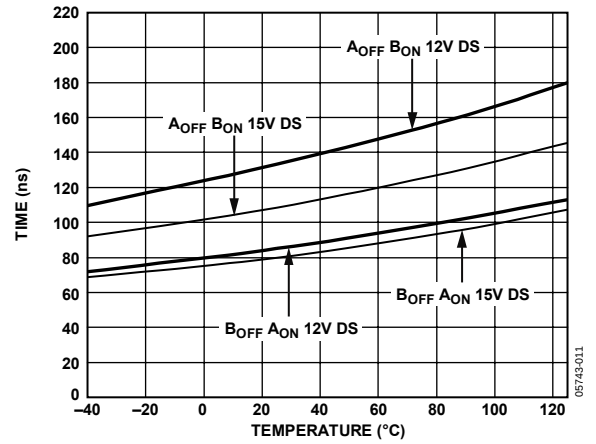


Figure 16.  $t_{\text{TRANSITION}}$  vs. Temperature

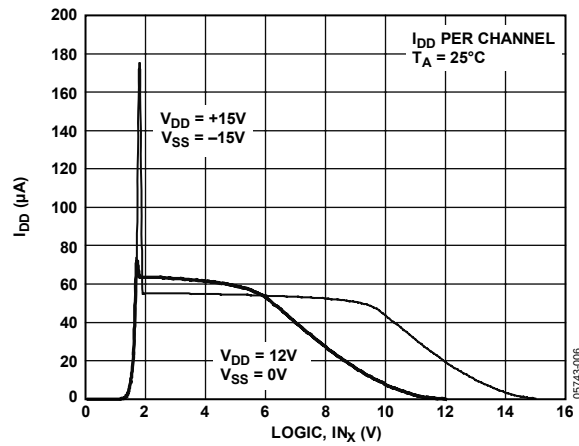


Figure 14.  $I_{\text{DD}}$  vs. Logic Level

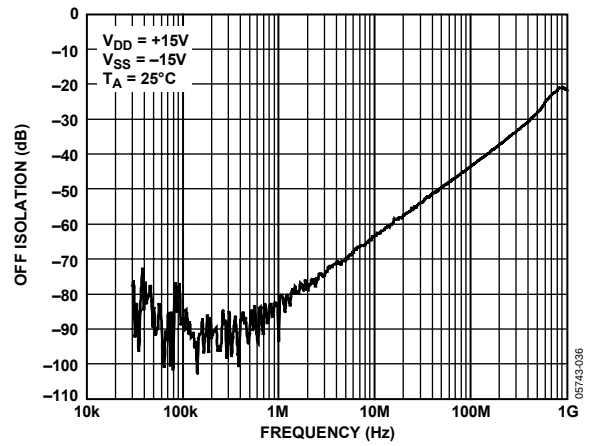


Figure 17. Off Isolation vs. Frequency

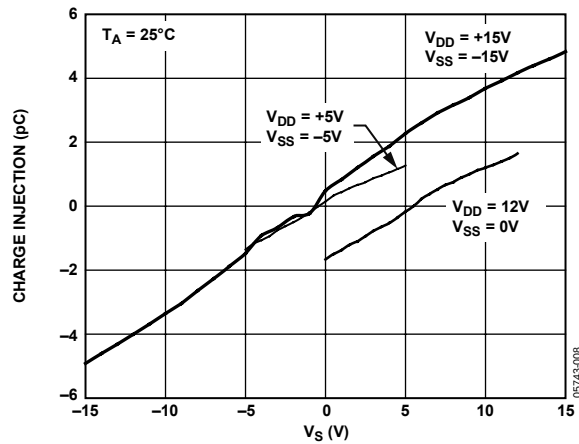


Figure 15. Charge Injection vs. Source Voltage

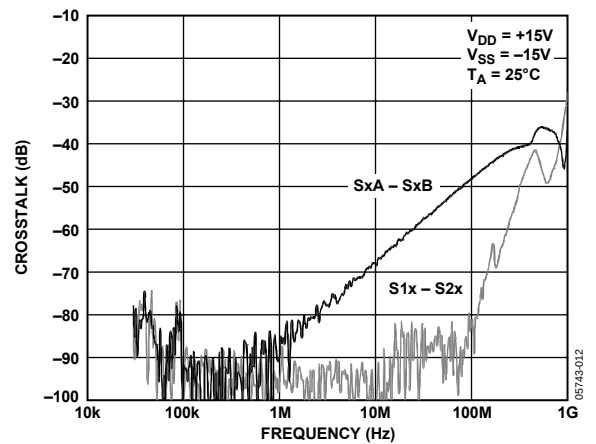


Figure 18. Crosstalk vs. Frequency

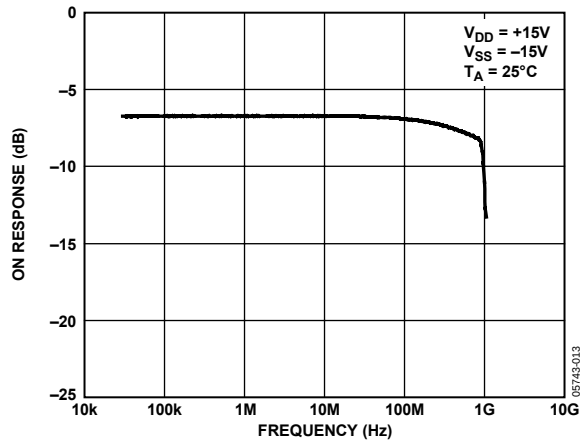


Figure 19. On Response vs. Frequency

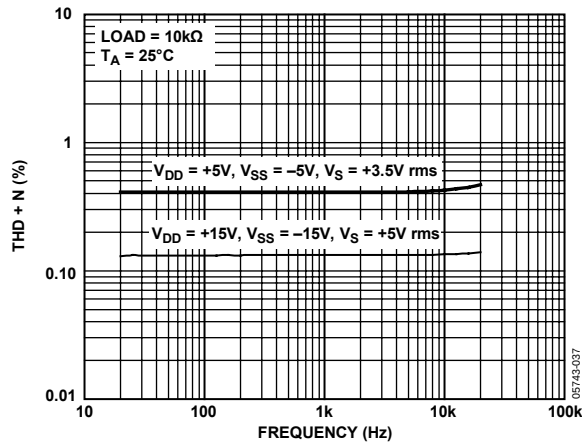


Figure 20. THD + N vs. Frequency

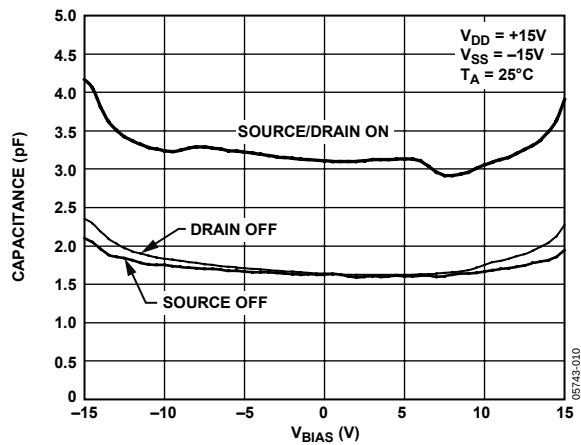


Figure 21. Capacitance vs. Source Voltage for Dual Supply

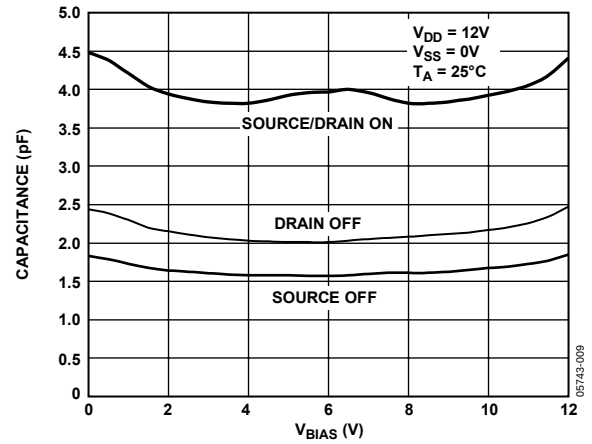


Figure 22. Capacitance vs. Source Voltage for Single Supply

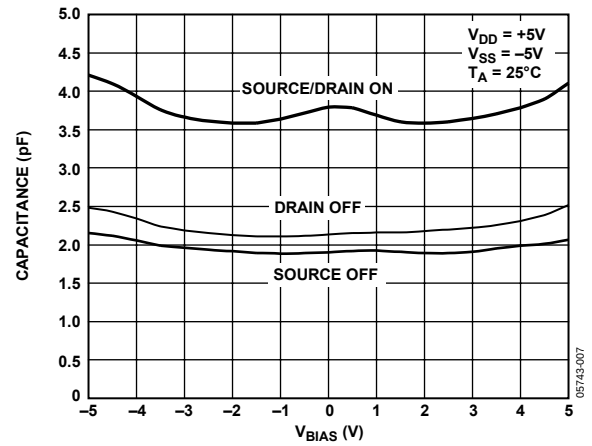


Figure 23. Capacitance vs. Source Voltage for Dual Supply

TEST CIRCUITS

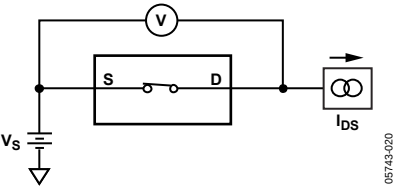


Figure 24. On Resistance

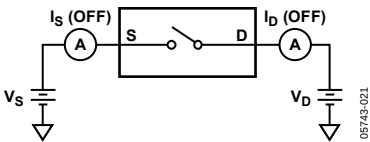


Figure 25. Off Leakage

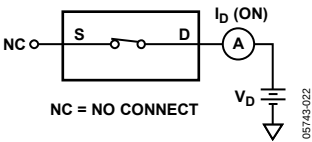


Figure 26. On Leakage

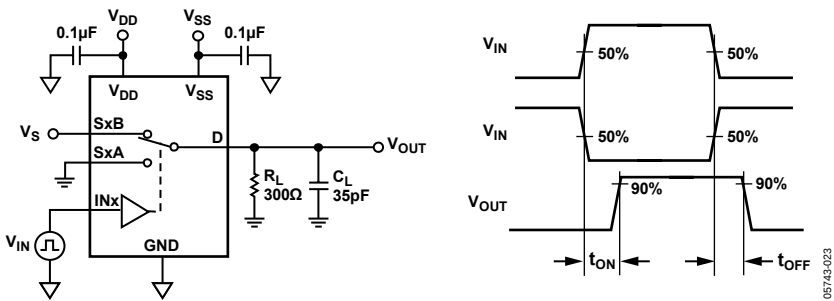


Figure 27. Switching Timing

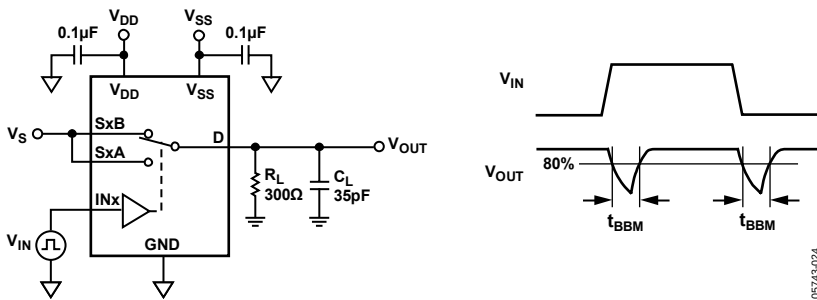
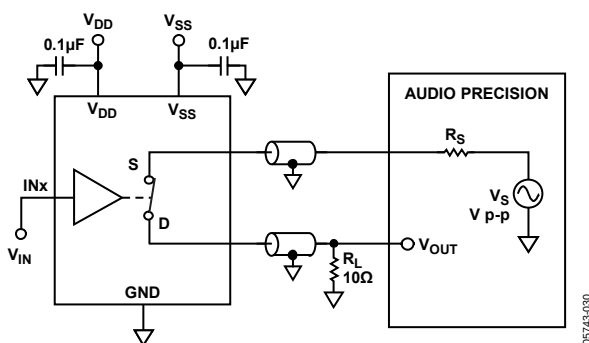
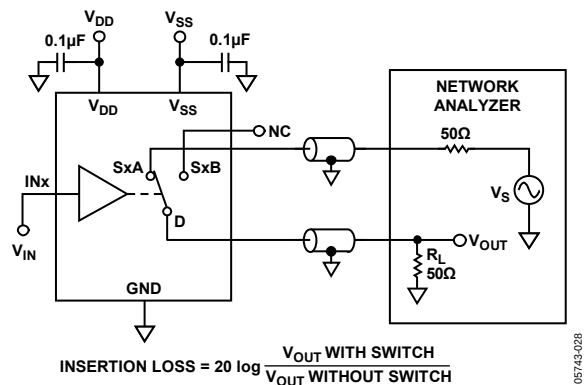
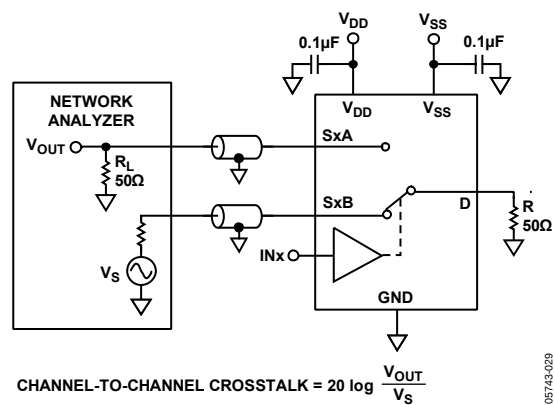
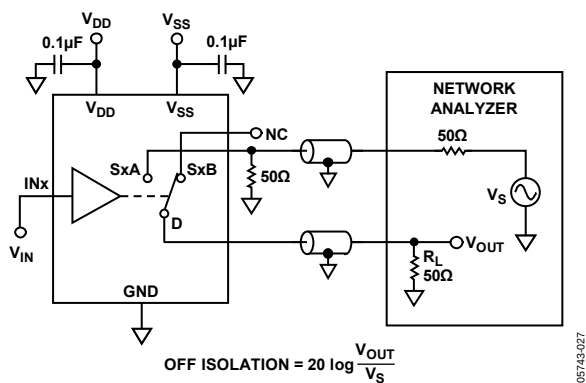
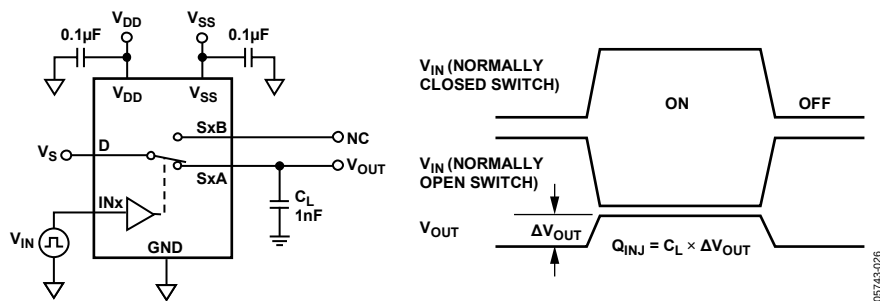
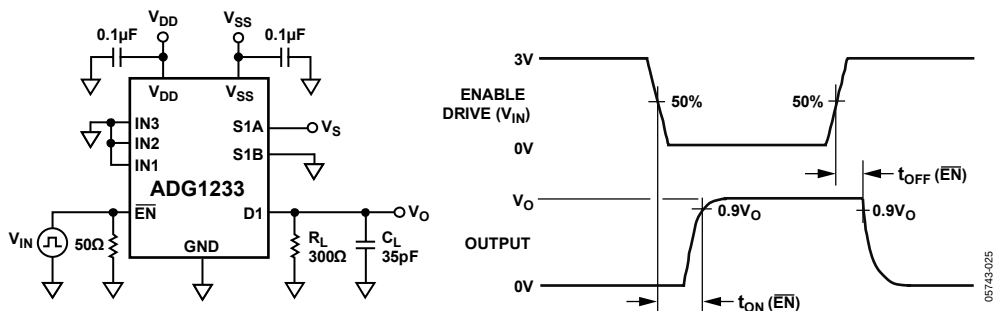
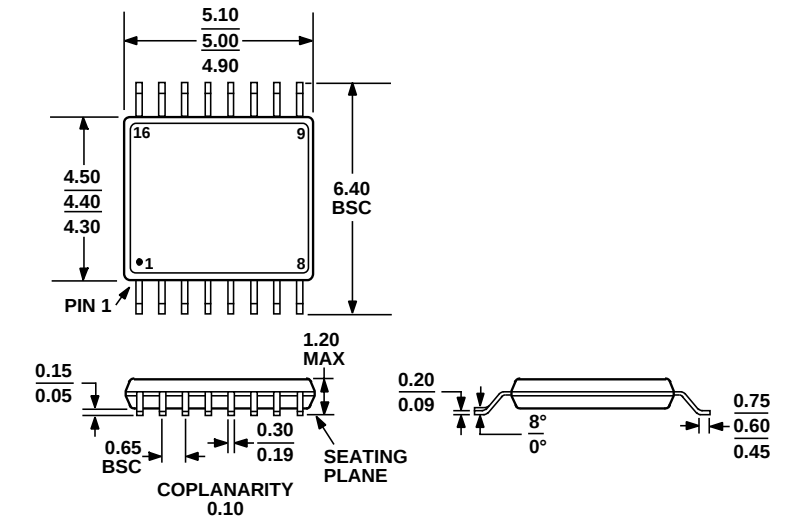


Figure 28. Break-Before-Make Delay

# ADG1233/ADG1234



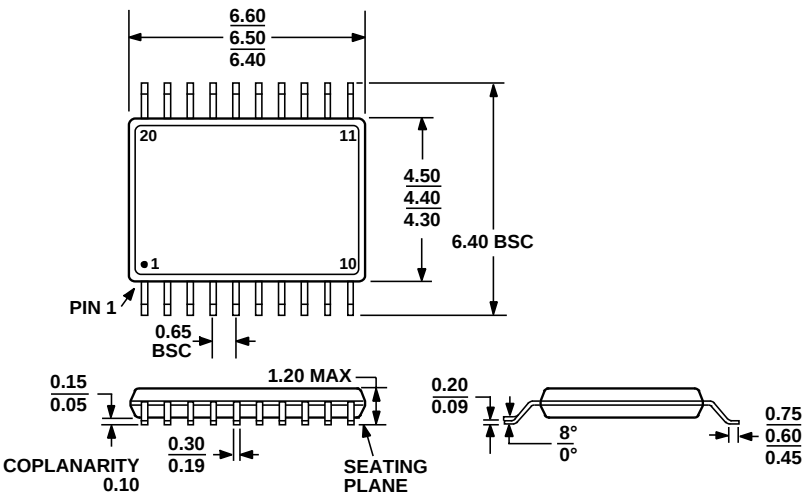
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-16)

Dimensions shown in millimeters

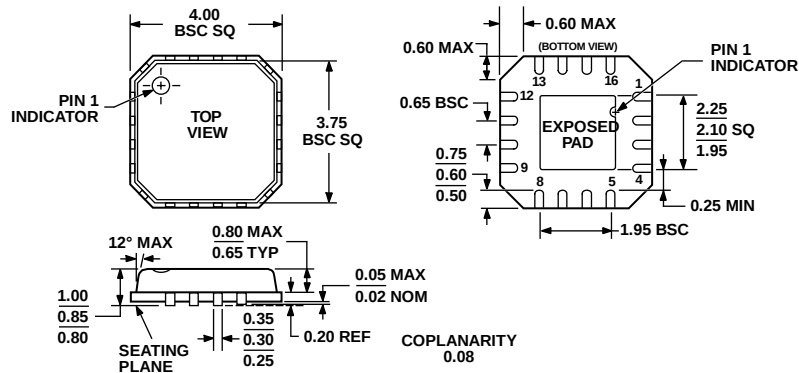


COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 36. 20-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-20)

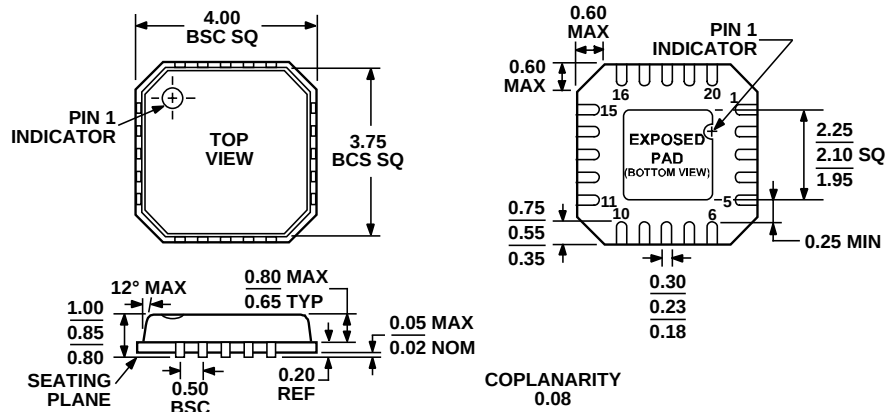
Dimensions shown in millimeters

# ADG1233/ADG1234



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
4 mm × 4 mm Body, Very Thin Quad  
(CP-16-4)  
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 38. 20-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
4 mm × 4 mm Body, Very Thin Quad  
(CP-20-1)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model                          | Temperature Range | Package Description                               | Package Option |
|--------------------------------|-------------------|---------------------------------------------------|----------------|
| ADG1233YRUZ <sup>1</sup>       | –40°C to +125°C   | 16-Lead Thin Shrink Small Outline Package (TSSOP) | RU-16          |
| ADG1233YRUZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 16-Lead Thin Shrink Small Outline Package (TSSOP) | RU-16          |
| ADG1233YCPZ-REEL <sup>1</sup>  | –40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)  | CP-16-4        |
| ADG1233YCPZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)  | CP-16-4        |
| ADG1234YRUZ <sup>1</sup>       | –40°C to +125°C   | 20-Lead Thin Shrink Small Outline Package (TSSOP) | RU-20          |
| ADG1234YRUZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 20-Lead Thin Shrink Small Outline Package (TSSOP) | RU-20          |
| ADG1234YCPZ-REEL <sup>1</sup>  | –40°C to +125°C   | 20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)  | CP-20-1        |
| ADG1234YCPZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)  | CP-20-1        |

<sup>1</sup> Z = Pb-free part.