256K x 36 SSRAM

Flow-Through, Synchronous Burst SRAM

FEATURES

- Organized 256K x 36
- Fast Clock and OE\ access times
- Single +3.3V +0.3V/-0.165V power supply (V_{DD})
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading

OPTIONS — MARKING

- Timing
  - 8.5ns/10ns/100MHz — -8.5*
  - 10ns/15ns/66MHz — -10
- Packages
  - 100-pin TQFP (2-chip enable) — DQ No. 1001
- Pinout
  - 2-chip Enables — A (PRELIMINARY)
  - 3-chip Enables — no indicator
- Operating Temperature Ranges
  - Military (-55°C to +125°C) — XT*
  - Industrial (-40°C to +85°C) — IT

***NOTE:** -8.5/XT combination not available.*

GENERAL DESCRIPTION

The AS5SS256K36 employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

This 8Mb Synchronous Burst SRAM integrates a 256K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE\), two additional chip enables for easy depth expansion (CE2\, CE2), burst control inputs (ADSC\, ADSP\, ADV\), byte write enables (BWx\) and global write (GW\). Note that CE2\ is not available on the A version.

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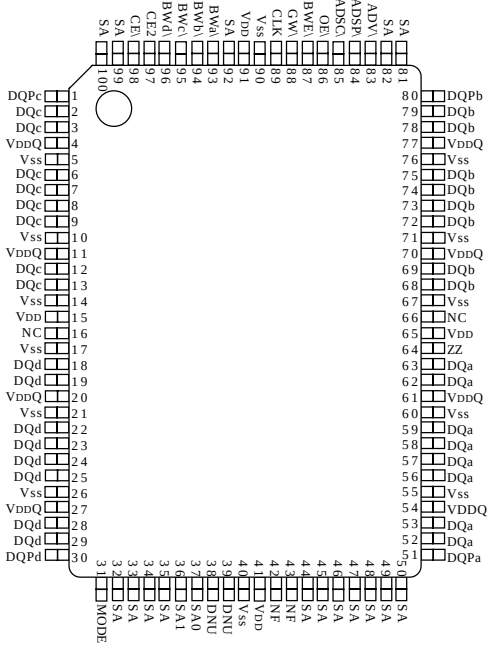
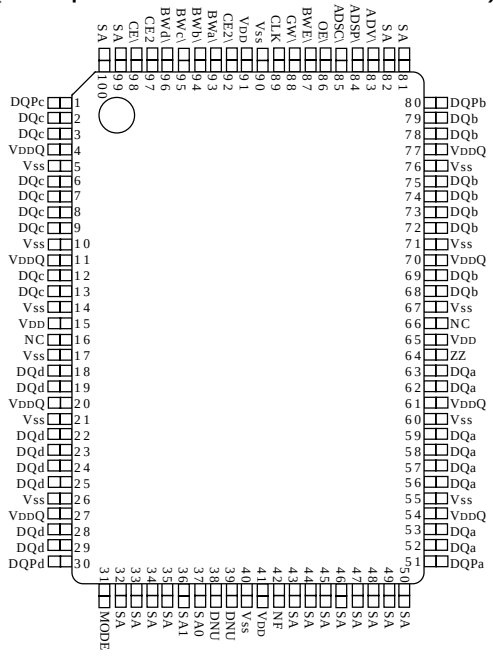
PIN ASSIGNMENT
(Top View)

100-pin TQFP (DQ)
(2-chip enable version, "A" indicator)



100-pin TQFP (DQ)
(3-chip enable version, no indicator)



GENERAL DESCRIPTION (continued)

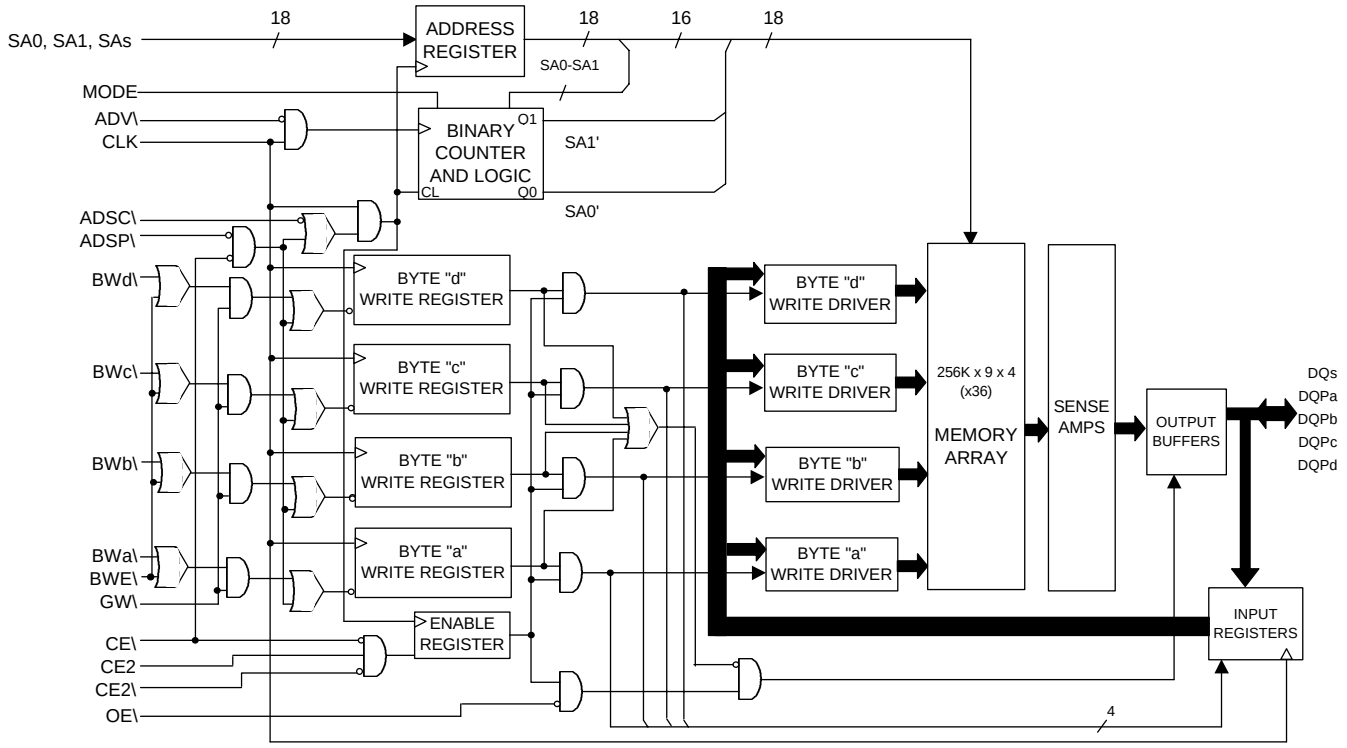
Asynchronous inputs include the output enable (OE\), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE\, is also asynchronous. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP\) or address status controller (ADSC\) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV\).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa\ controls DQa's and DQPa; BWb\ controls DQb's and DQPb; BWc\ controls DQc's and DQPc; BWd\ controls DQd's and DQPd. GW\ LOW causes all bytes to be written. Parity bits are also featured on this device.

This 8Mb Synchronous Burst SRAM operates from a +3.3V V_{DD} power supply, and all inputs and outputs are TTL-compatible. The device is ideally suited for 486, Pentium©, 680x0 and PowerPC™ systems and those systems that benefit from a wide synchronous data bus.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and time diagrams for detailed information.

PIN DESCRIPTION

Pin Number	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-50, 81, 82, 99, 100 92 (A version) 43 (3 CE version)	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Two different pinouts are available for the TQFP packages.
93 94 95 96	BWa\ BWb\ BWc\ BWd\	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. Bwa\ controls DQa pins and DQPa; Bwb\ controls DQb pins and DQPb; Bwc\ controls DQc pins and DQPc; Bwd\ controls DQd pins and DQPd. Parity bits are featured on this device.
87	BWE\	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold items around the rising edge of CLK.
88	GW\	Input	Global Write: This active LOW input allows a full 36-bit WRITE to occur independent of the BWE\ and BWx\ lines and must meet the setup and hold times around the rising edge of CLK.
89	CLK	Input	Clock: CLK registers address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	CE\	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP\. CE\ is sampled only when a new external address is loaded.
92 (3 CE version)	CE2\	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded. CE2\ is only available on the 3 CE version.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
86	OE\	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
83	ADV\	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV\ must be HIGH at the rising edge of the first clock after an ADSP\ cycle is initiated.
85	ADSC\	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE\ is LOW. ADSC\ is also used to place the chip into power-down state when CE\ is HIGH.

PIN DESCRIPTION (continued)

Pin Number	SYMBOL	TYPE	DESCRIPTION
84	ASDP\	Input	Synchronous Address Status Processor: This active LOW inputs interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC\, but dependent upon CE\, CE2 and CE2\. ADSP\ is ignored if CE\ is HIGH. Power-down state is entered if CE2 is LOW or CE2\ is HIGH.
31	MODE	Input	MODE: This inputs selects the burst sequence. A LOW on this pin select "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating.
64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/O's: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
51 80 1 30	NC/DQPa NC/DQPb NC/DQPc NC/DQPd	NC/ I/O	Parity Data I/Os: Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd.
15, 41, 65, 91	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 14, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	Vss	Supply	Ground: GND
38, 39	DNU	---	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
16, 66	NC	---	No Connect: These signals are not internally connected and may be connected to GND to improve package heat dissipation.
42 43 (A version)	NF	---	No Function: These pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals. On the 3 CE version, pin 42 is reserved as an address upgrade pin for the 16Mb Synchronous Burst.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X…X00	X…X01	X…X10	X…X11
X…X01	X…X00	X…X11	X…X10
X…X10	X…X11	X…X00	X…X01
X…X11	X…X10	X…X01	X…X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X…X00	X…X01	X…X10	X…X11
X…X01	X…X10	X…X11	X…X00
X…X10	X…X11	X…X00	X…X01
X…X11	X…X00	X…X01	X…X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS

FUNCTION	GW\	BWE\	BWa\	BWb\	BWc\	BWd\
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte "a"	H	L	L	H	H	H
WRITE All Bytes	H	L	L	L	L	L
WRITE All Bytes	L	X	X	X	X	X

TRUTH TABLE

OPERATION	ADDRESS USED	CE\	CE2\	CE2	ZZ	ADSP\	ADSC\	ADV\	WRITE\	OE\	CLK	DQ
Deselected Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. X means "Don't Care." \ means active LOW. H Means logic HIGH. L means logic LOW.
2. For WRITE\, L means any one or more byte write enable signals (BWa\, BWb\, BWc\, or BWd\) and BWE\ are LOW or GW\ is LOW. WRITE\ = H for all BWx\, BWE\, GW\ HIGH.
3. BWa\ enables WRITEs to DQa pins, DQPa. BWb\ enables WRITEs to DQb pins, DQPb. BWc\ enables WRITEs to DQc pins, DQPc. BWd\ enables WRITEs to DQd pins, DQPd.
4. All inputs except OE\ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, OE\ must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be High-Z during power-up.
8. ADSP\ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE\ LOW or GW\ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature (Plastics) .....-55°C to +150°C
Storage Temperature (Ceramics) .....-55°C to +125°C
Short Circuit Output Current (per I/O). 100mA
Voltage on any Pin Relative to Vss.....-0.5V to +4.6 V
Max Junction Temperature**.....+150°C
V_{IN} (DQx) .....-0.5V to $V_{DD}Q$ +0.5V
V_{IN} (inputs) ....-0.5V to V_{DD} +0.5V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity.

3.3V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(-55°C to +125°C or -40°C to +85°C; V_{DD}, $V_{DD}Q$ = +3.3V +0.3V/-0.165V unless otherwise noted)

PARAMETER	CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$OV \leq V_{IN} \leq Vcc$	IL_I	-2	2	µA	3
Output Leakage Current	Output(s) disabled, $OV \leq V_{OUT} \leq Vcc$	IL_O	-2	2	µA	
Output High Voltage	I_{OH} = -4.0 mA	V_{OH}	2.4	--	V	1, 4
Output Low Voltage	I_{OL} = 8.0 mA	V_{OL}	---	0.4	V	1, 4
Supply Voltage		V_{DD}	3.135	3.6	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	3.135	3.6	V	1, 5

THERMAL RESISTANCE

DESCRIPTION	CONDITIONS		SYM	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	1-layer	θ_{JA}	40	°C/W	6
Thermal Resistance (Junction to Top of Case, Top)			θ_{JC}	9	°C/W	6
Thermal Resistance (Junction to Pins, Bottom)			θ_{JB}	17	°C/W	6

NOTES:

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} < +4.6V$ for $t<t_{KC}/2$ for $I < 20mA$
   Undershoot: $V_{IL} > -0.7V$ for $t<t_{KC}/2$ for $I < 20mA$
   Power-up: $V_{IH} < +3.6V$ and $V_{DD} < 3.135V$ for $t < 200ms$
3. MODE and ZZ pins have internal pull-up resistors, and input leakage = +10µA
4. The load used for V_{OH}, V_{OL} testing is shown in Figure 2 for 3.3V I/O. AC load current is higher than the stated DC values. AC I/O curves are available upon request.
5. $V_{DD}Q$ should never exceed V_{DD}. V_{DD} and $V_{DD}Q$ can be connected together.
6. This parameter is sampled.

I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(-55°C to +125°C or -40°C to +85°C)

DESCRIPTION	CONDITIONS	SYM	MAX -8.5	MAX -10	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; Cycle time $\geq t^{KC}$ MIN; V_{DD} = MAX; Outputs open	I_{DD}	325	250	mA	1, 2, 3
Power Supply Current: Idle	Device selected; V_{DD} = MAX; ADSC\, ADSP\, ADV\, GW\, BWx\ $\geq V_{IH}$; All inputs $\leq$ Vss+ 0.2 or $\geq V_{DD}$ -0.2; Cycle time $\leq t_{KC}$ MIN; Outputs open	I_{DD1}	85	65	mA	1, 2, 3
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs $\leq$ Vss +0.2 or $\geq V_{DD}$ -0.2; All inputs static; CLK frequency = 0	I_{SB2}	15	15	mA	2, 3
TTL Standby	Device deselected; V_{DD} = MAX; All inputs $\leq V_{IL}$ or $\geq V_{IH}$; All inputs static; CLK frequency = 0	I_{SB3}	30	30	mA	2, 3
Clock Running	Device deselected; V_{DD} = MAX; ADSC\, ADSP\, ADV\, GW\, BWx\ $\geq V_{IH}$; All inputs $\leq$ Vss +0.2 or $\geq V_{DD}$ -0.2 Cycle time $\geq t_{KC}$ MIN	I_{SB4}	85	65	mA	2, 3

CAPACITANCE

DESCRIPTION	CONDITIONS	SYM	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1MHz; V_{DD} = 3.3V	C_I	4	pF	4
Input/Output Capacitance (DQ)		C_O	5	pF	4
Address Capacitance		C_A	3.5	pF	4
Clock Capacitance		C_{CK}	3.5	pF	4

NOTES:

1. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
2. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
3. A typical value is measured at 3.3V, 25°C and 15ns cycle time.
4. This parameter is sampled.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 1) (-55°C to +125°C or -40°C to +85°C)

DESCRIPTION	SYMBOL	-8.5		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX		
CLOCK							
Clock cycle time	t_{KC}	10.0		15.0		ns	
Clock frequency	t_{KF}		100		66	MHz	
Clock HIGH time	t_{KH}	3.0		4.0		ns	2
Clock LOW time	t_{KL}	3.0		4.0		ns	2
OUTPUT TIMES							
Clock to output valid	t_{KQ}		8.5		10.0	ns	
Clock to output invalid	t_{KQX}	3.0		3.0		ns	3
Clock to output in Low-Z	t_{KQLZ}	3.0		3.0		ns	3, 4, 5, 6,
Clock to output in High-Z	t_{KQHZ}		5.0		5.0	ns	3, 4, 5, 6,
OE\ to output valid	t_{OEQ}		5.0		5.0	ns	7
OE\ to output in Low-Z	t_{OELZ}	0		0		ns	3, 4, 5, 6,
OE\ to output in High-Z	t_{OEHZ}		5.0		5.0	ns	3, 4, 5, 6,
SETUP TIMES							
Address	t_{AS}	1.8		2.0		ns	8, 9
Address status (ADSC\, ADSP\)	t_{ADSS}	1.8		2.0		ns	8, 9
Address advance (ADV\)	t_{AAS}	1.8		2.0		ns	8, 9
Byte write enables (BWa\ - BWd\, GW\, BWE\)	t_{WS}	1.8		2.0		ns	8, 9
Data-in	t_{DS}	1.8		2.0		ns	8, 9
Chip enable (CE\)	t_{CES}	1.8		2.0		ns	8, 9
HOLD TIMES							
Address	t_{AH}	0.5		0.5		ns	8, 9
Address status (ADSC\, ADSP\)	t_{ADSH}	0.5		0.5		ns	8, 9
Address advance (ADV\)	t_{AAH}	0.5		0.5		ns	8, 9
Byte write enables (BWa\ - BWd\, GW\, BWE\)	t_{WH}	0.5		0.5		ns	8, 9
Data-in	t_{DH}	0.5		0.5		ns	8, 9
Chip enable (CE\)	t_{CEH}	0.5		0.5		ns	8, 9

NOTE:

1. Test conditions as specified with the output loading shown in Figure 1 unless otherwise noted.
2. Measured as HIGH above V_{IH} and LOW below V_{IL}.
3. This parameter is measured with the output loading shown in Figure 2 for 3.3V I/O.
4. This parameter is sampled.
5. Transition is measured +500mV from steady state voltage.
6. Refer to Technical Note TN-58-09, "Synchronous SRAM Bus Contention Design Considerations," for a more thorough discussion on these parameters.
7. OE\ is a "Don't Care" when a byte write enable is sampled LOW.
8. A READ cycle is defined by byte write enables all HIGH or ADSP\ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and ADSP\ HIGH for the required setup and hold times.
9. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP\ or ADSC\ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP\ or ADSC\ is LOW to remain enabled.

AC TEST CONDITIONS

Input Pulse Levels	$V_{IH} = (V_{DD}/2.2) + 1.5V$
	$V_{IL} = (V_{DD}/2.2) - 1.5V$
Input rise and fall times	1ns
Input timing reference levels	$V_{DD}/2.2$
Output reference levels	$V_{DD}Q/2.2$
Output load	See Figures 1 and 2

OUTPUT LOADS

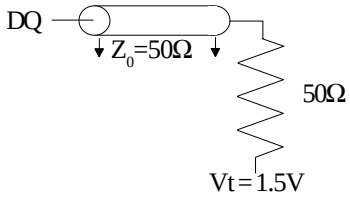


Fig. 1 3.3V I/O OUTPUT LOAD EQUIVALENT

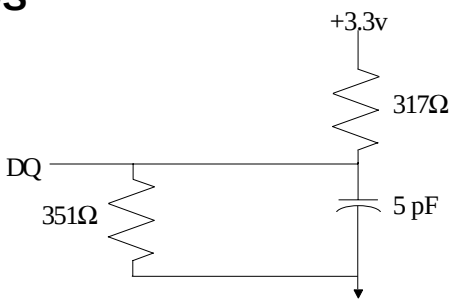


Fig. 2 3.3V I/O OUTPUT LOAD EQUIVALENT

NOTE: SRAM timing is dependent upon the capacitive loading on the outputs.

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

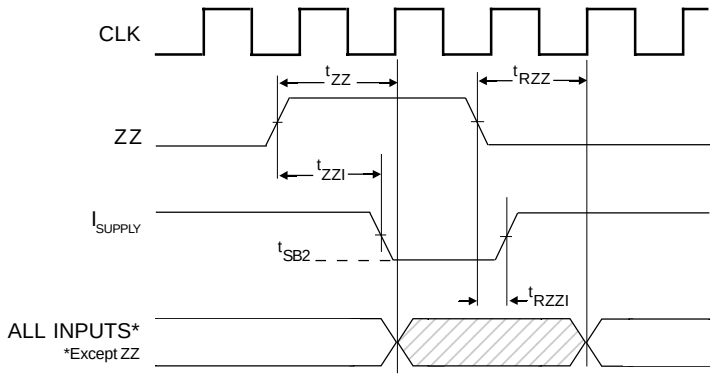
ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time t_{ZZ} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{SB2Z}		10	mA	
ZZ active to input ignored		t_{ZZ}		t_{KC}	ns	1
ZZ inactive to input sampled		t_{RZZ}	t_{KC}		ns	1
ZZ active to snooze current		t_{ZZI}		t_{KC}	ns	1
ZZ inactive to exit snooze current		t_{RZZI}	0		ns	1

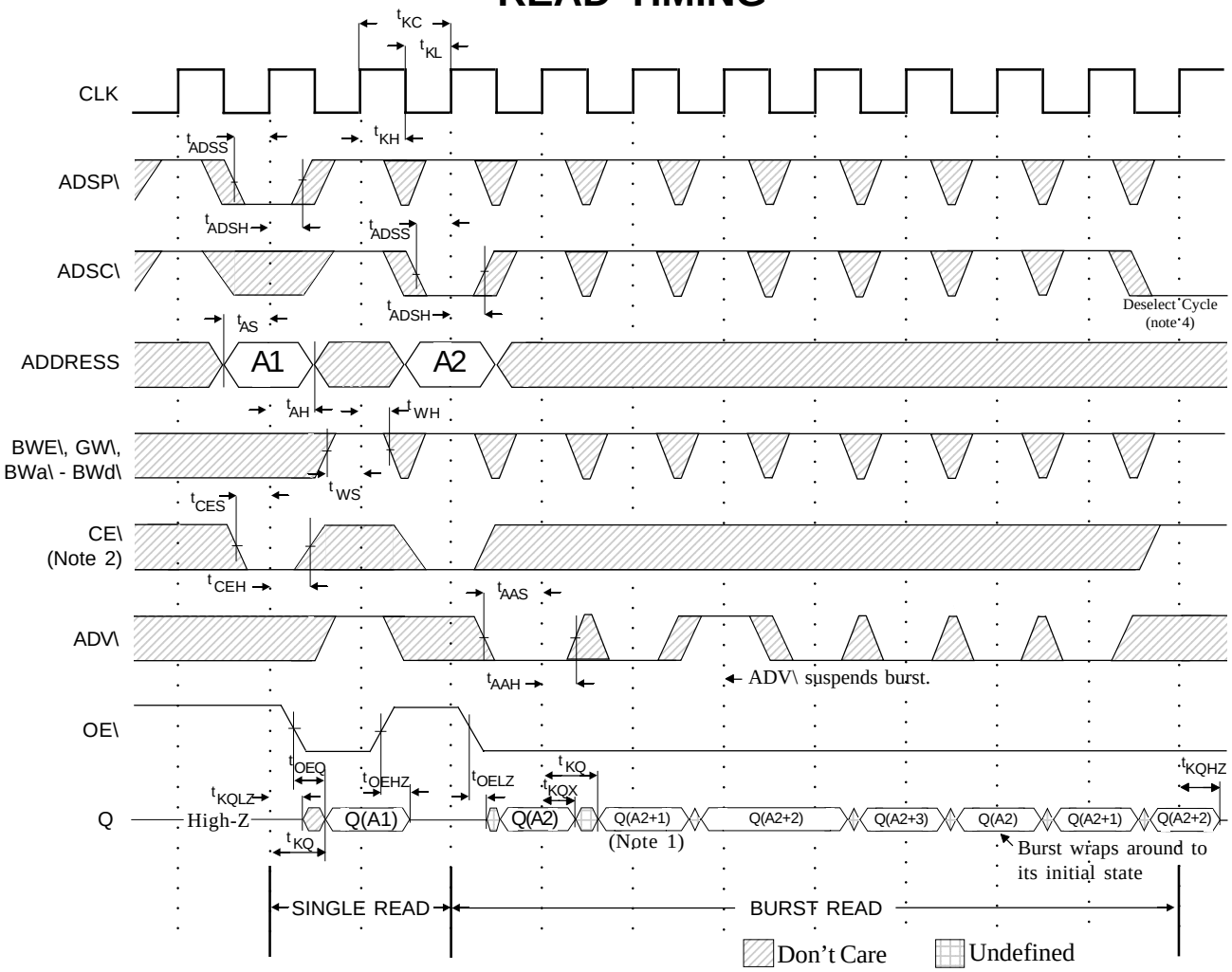
NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM



Don't Care

READ TIMING[3]



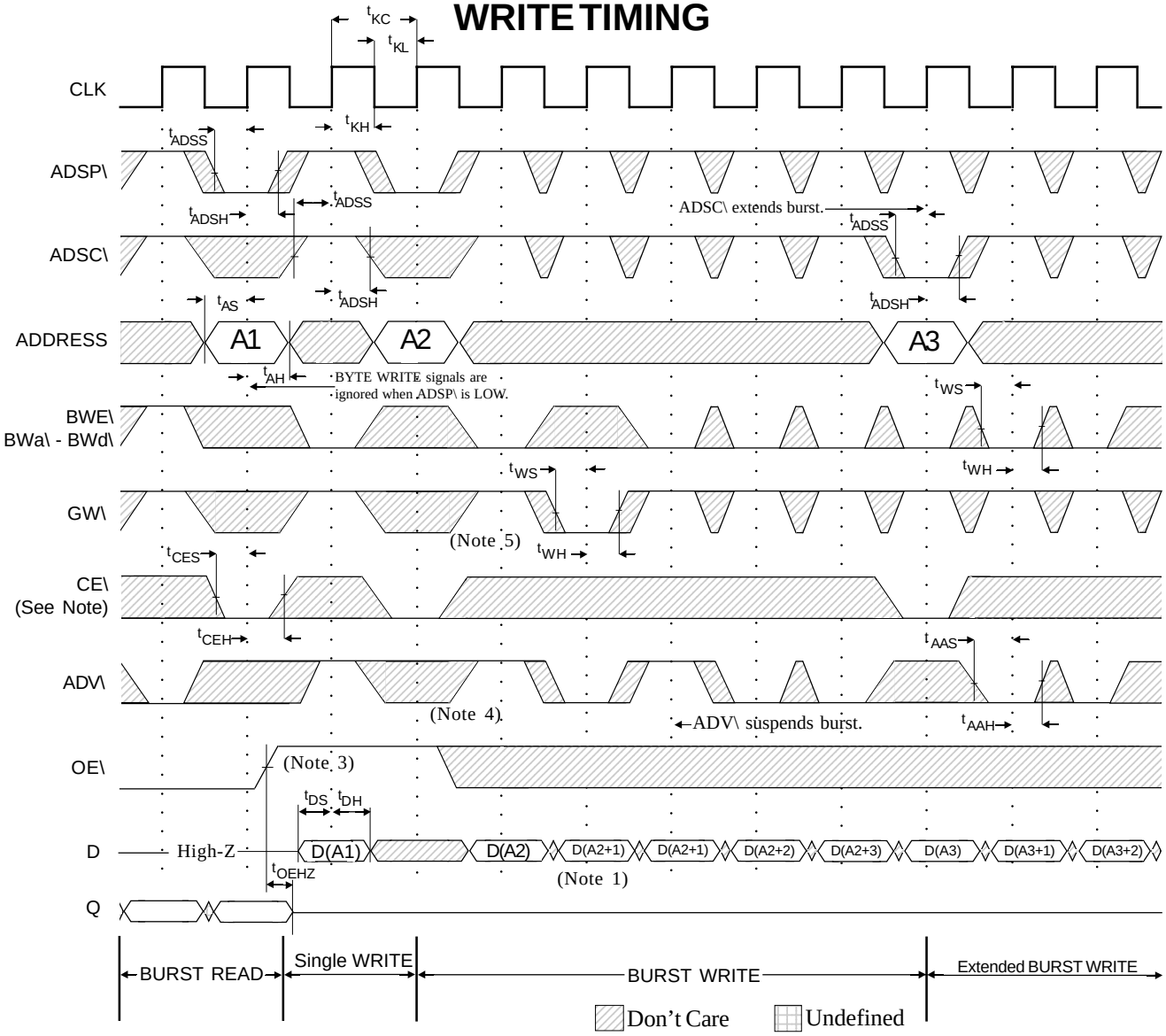
READ/WRITE TIMING PARAMETERS

	-8.5		-10		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
t_{KC}	10.0		15		ns
t_{KF}		100		66	MHz
t_{KH}	3.0		4.0		ns
t_{KL}	3.0		4.0		ns
t_{KQ}		8.5		10.0	ns
t_{KQX}	3.0		3.0		ns
t_{KQLZ}	3.0		3.0		ns
t_{KQHZ}		5.0		5.0	ns
t_{OEQ}		5.0		5.0	ns
t_{OELZ}	0		0		ns
t_{OEHZ}		5.0		5.0	ns

	-8.5		-10		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
t_{AS}	1.8		2.0		ns
t_{ADSS}	1.8		2.0		ns
t_{AAS}	1.8		2.0		ns
t_{WS}	1.8		2.0		ns
t_{CES}	1.8		2.0		ns
t_{AH}	0.5		0.5		ns
t_{ADSH}	0.5		0.5		ns
t_{AAH}	0.5		0.5		ns
t_{WH}	0.5		0.5		ns
t_{CEH}	0.5		0.5		ns

NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. CE2\ and CE2 have timing identical to CE\. On this diagram, when CE\ is LOW, CE2\ is LOW and CE2 is HIGH. When CE\ is HIGH, CE2\ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence.
4. Outputs are disabled t_{KQHZ} after deselect.

WRITE TIMING



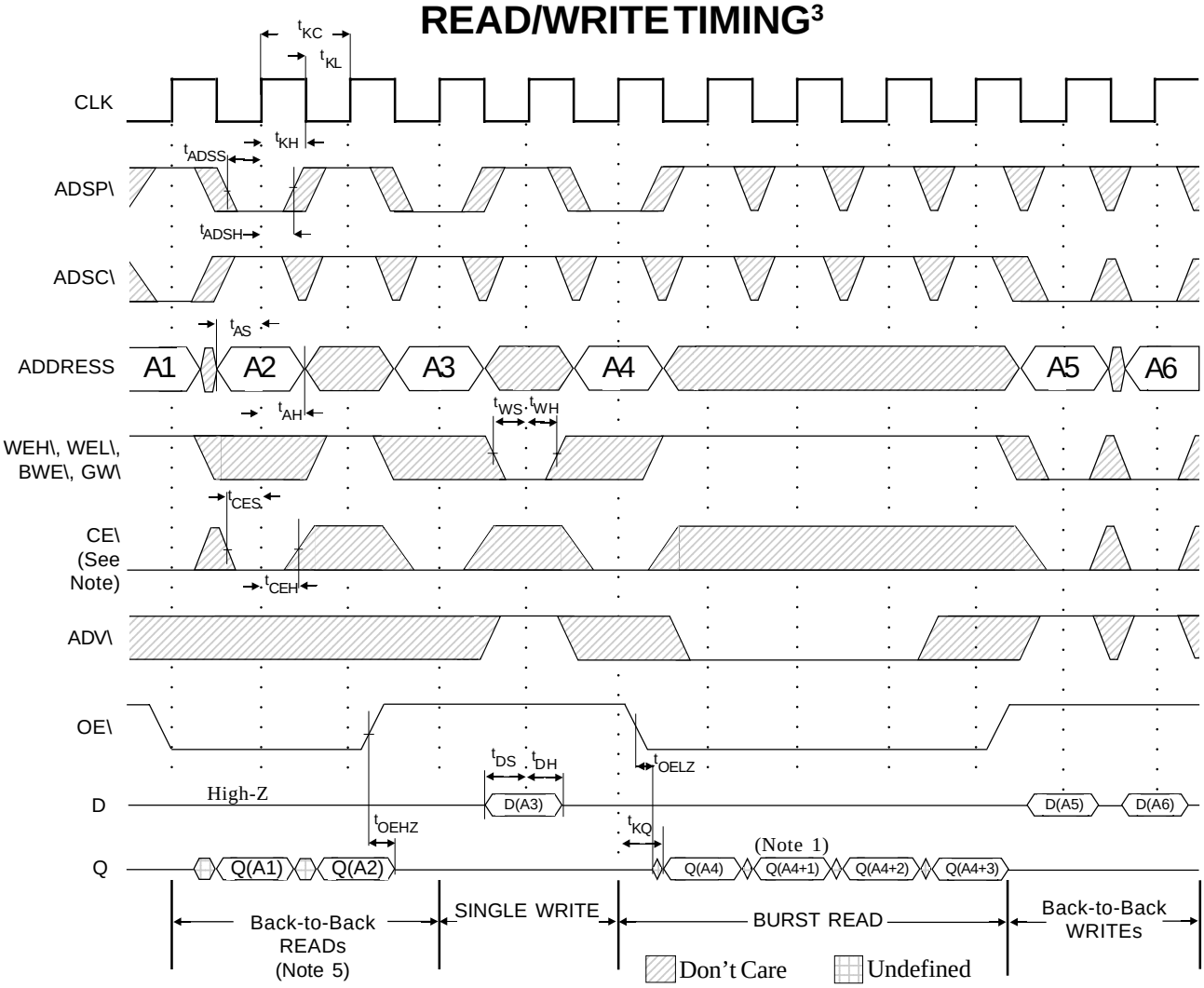
WRITE TIMING PARAMETERS

	-8.5		-10		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
t_{KC}	10.0		15		ns
t_{KF}		100		66	MHz
t_{KH}	3.0		4.0		ns
t_{KL}	3.0		4.0		ns
t_{OEHZ}		5.0		5.0	ns
t_{AS}	1.8		2.0		ns
t_{ADSS}	1.8		2.0		ns
t_{AAS}	1.8		2.0		ns
t_{WS}	1.8		2.0		ns

	-8.5		-10		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
t_{DS}	1.8		2.0		ns
t_{CES}	1.8		2.0		ns
t_{AH}	0.5		0.5		ns
t_{ADSH}	0.5		0.5		ns
t_{AAH}	0.5		0.5		ns
t_{WH}	0.5		0.5		ns
t_{DH}	0.5		0.5		ns
t_{CEH}	0.5		0.5		ns

NOTE:
1. D(A2) refers to output from address A2. D(A2+1) refers to output from the next internal burst address following A2.
2. CE2\ and CE2 have timing identical to CE\. On this diagram, when CE\ is LOW, CE2\ is LOW and CE2 is HIGH. When CE\ is HIGH, CE2\ is HIGH and CE2 is LOW.
3. OE\ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. ADV\ must be HIGH to permit a WRITE to the loaded address.
5. Full-width WRITE can be initiated by GW\ LOW; or GW\ HIGH and BEW\, BWa\ - BWd\ LOW.

READ/WRITE TIMING[3]



WRITE TIMING PARAMETERS

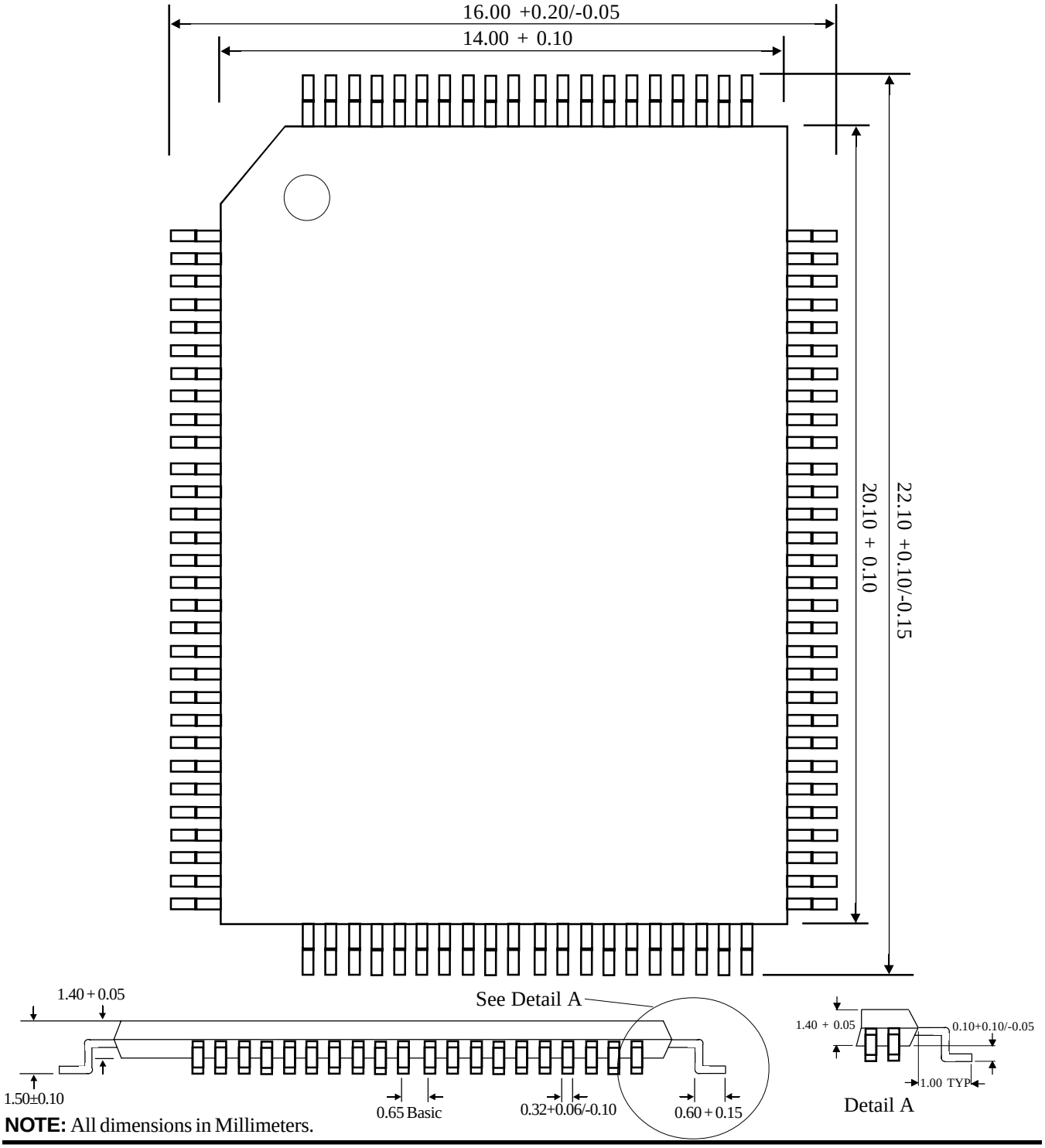
	-8.5		-10		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
t_{KC}	10.0		15		ns
t_{KF}		100		66	MHz
t_{KH}	3.0		4.0		ns
t_{KL}	3.0		4.0		ns
t_{KQ}		8.5		10.0	ns
t_{OELZ}	0		0		ns
t_{OEHZ}		5.0		5.0	ns
t_{AS}	1.8		2.0		ns
t_{ADSS}	1.8		2.0		ns

	-8.5		-10		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
t_{WS}	1.8		2.0		ns
t_{DS}	1.8		2.0		ns
t_{CES}	1.8		2.0		ns
t_{AH}	0.5		0.5		ns
t_{ADSH}	0.5		0.5		ns
t_{WH}	0.5		0.5		ns
t_{DH}	0.5		0.5		ns
t_{CEH}	0.5		0.5		ns

NOTE:
1. Q(A4) refers to output from address A. Q(A4+1) refers to output from the next internal burst address following A4.
2. CE2\ and CE2 have timing identical to CE\. On this diagram, when CE\ is LOW, CE2\ is LOW and CE2 is HIGH. When CE\ is HIGH, CE2\ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-A following a WRITE cycle unless an ADSP\, ADSC\ or ADV\ cycle is performed.
4. GW\ is HIGH.
5. Back-to-back READs may be controlled by either ADSP\ or ADSC\.

MECHANICAL DEFINITIONS

ASI Case #1001 (Package Designator DQ)



NOTE: All dimensions in Millimeters.

ORDERING INFORMATION

EXAMPLE: AS5SS256K36ADQ-8.5/IT

Device Number	Options**	Package Type	Speed ns	Process
AS5SS256K36	A	DQ	-8.5	/*
AS5SS256K36	A	DQ	-10	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range	-40°C to +85°C[1]
XT = Extended Temperature Range	-55°C to +125°C
883C = Full Military Processing	-55°C to +125°C

****DEFINITION OF OPTIONS**

2-Chip Enable Pinout	A
3-Chip Enable Pinout	no indicator

NOTES: *1. -8.5/XT combination not available.*