CY2SSTV16857

14-Bit Registered Buffer PC2700-/PC3200-Compliant

Features

- **Differential Clock Inputs up to 280 MHz**
- **Supports LVTTL switching levels on the $\overline{\text{RESET}}$ pin**
- **Output drivers have controlled edge rates, so no external resistors are required**
- **Two KV ESD protection**
- **Latch-up performance exceeds 100 mA: JESD78, Class II**
- **Conforms to JEDEC STD (JESD82-3) for buffered DDR DIMMs**
- **48-pin TSSOP**

Description

This 14-bit registered buffer is designed specifically for 2.3V to 2.7V V_{DD} operation and is characterized for operation from 0°C to + 85°C.

All inputs are compatible with the JEDEC Standard for SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II-compatible.

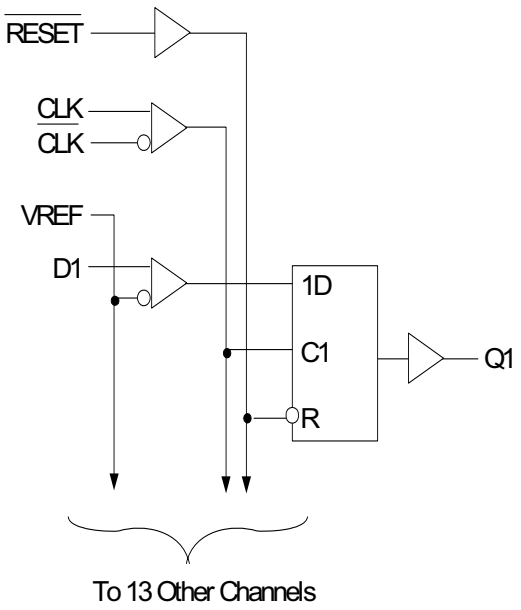
The SSTV16857 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data is measured at the crossing of CLK going HIGH, and $\overline{\text{CLK}}$ going LOW.

When $\overline{\text{RESET}}$ is LOW, the differential input receivers are disabled, and undriven (floating) data, clock, and REF voltage inputs are allowed. In addition, when $\overline{\text{RESET}}$ is LOW, all registers are reset and all outputs force to the LOW state. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic HIGH or LOW level.

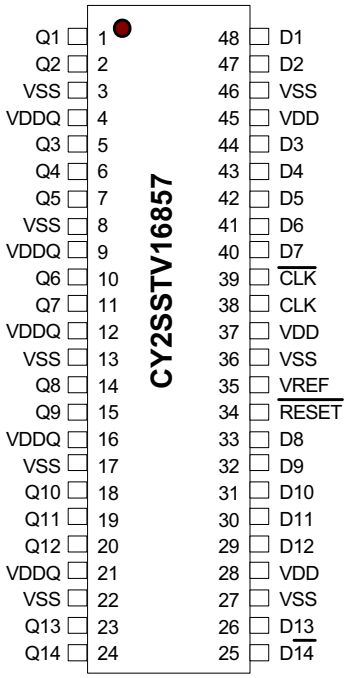
To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the LOW state during power-up.

In the DDR registered DIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CLK and $\overline{\text{CLK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven LOW quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the LOW-to-HIGH transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design must ensure that the outputs will remain LOW.

Block Diagram



Pin Configuration



2200 Laurelwood Road, Santa Clara, CA 95054 Tel:(408) 855-0555 Fax:(408) 855-0550 www.SpectraLinear.com

Pin Description

Pin	Name	I/O	Type	Description
34	RESET	I		
3,8,13,17,22,27,36,46	VSS	Ground		**Ground**.
28, 37, 45	VDD	Power		**2.5V nominal supply voltage**.
1, 2, 5, 6, 7, 10, 11, 14, 15, 18, 19, 20, 23, 24	Q(1:14)	O		**Data outputs, SSTL_2, Class II output**.
25, 26, 29, 30, 31, 32, 33, 40, 41, 42, 43, 44, 47, 48	D(1:14)	I		**Data input clocked on the crossing of the rising edge of CLK, and the falling edge of CLK**.
39, 38	$\overline{CLK}$, CLK	I/I		**Differential clock input**.
4, 8, 12, 16, 21	VDDQ	Power		**Power supply voltage quiet, 2.5V nominal**.
35	VREF	I		**Input reference voltage, 1.25V nominal**.

Absolute Maximum Conditions[1, 2, 3]

This device contains circuitry designed to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage[4]	Non-functional	2.3	2.7	VDC
V_{DD}	Operating Voltage[4]	Functional	2.3	2.7	VDC
V_{in}	Input Voltage	Relative to V_{SS}	0	V_{DD}	VDC
V_{out}	Output Voltage	Relative to V_{SS}		V_{DDQ}	VDC
I_{OUT}	DC Output Current			±50	mA
I_{IK}	Continuous Clamp Current	$V_I < 0$ or $V_I > V_{SS}$		±50	mA
I_{OK}	Continuous Clamp Current	$V_O < 0$		–50	mA
I_{DD}/I_{SS}	Continuous current through each V_{DD} or V_{SS}			±100	mA
LU_I	Latch Up Immunity	Exceeds spec of	100		mA
R_{PS}	Power Supply Ripple	Ripple Frequency < 100 kHz		150	mVp-p
T_s	Temperature, Storage	Non-functional	–65	+150	°C
T_a	Temperature, Operating Ambient	Functional	0	+70	°C
T_j	Temperature, Junction	Functional		165	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	22.23		°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	74.52		°C/W
UL_{FL}	Flammability	By design and verification	V – 0		Grade
MSL	Moisture Sensitivity	By design and verification	MSL – 1		Grade
ESD_h	ESD Protection (Human Body Model)		2000		V

Table 1. DC Electrical Specifications (V_{DD} = Temperature = 0°C to +85 °C)

Parameter	Description		Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	PC1600,2100,2700 PC3200		2.5	2.6	2.7	V
V_{DDQ}	Output Supply Voltage	PC1600,2100,2700 PC3200		2.5	2.6	2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)	PC1600,2100,2700 PC3200		1.25	1.3	1.35	V
V_{TT}	Termination voltage			V_{REF} – 40 mV	V_{REF}	V_{REF}+4 0 mV	V
V_{IH}	Input Voltage, High		$\overline{\text{RESET}}$	1.7			V
V_{IL}	Input Voltage, Low		$\overline{\text{RESET}}$			0.7	V
V_{OL}	Output Voltage, Low		V_{DD}/V_{DDQ} = 2.3V to 2.7V, I_{OL} = 100 µA, V_{DD} = 2.3 to 2.7V			0.2	V
			V_{DD}/V_{DDQ} = 2.3V, I_{OL} = 16 mA, V_{DD} = 2.3V			0.35	

Notes:
1. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
2. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
3. All terminals except V_{DD}.
4. V_{DD}/V_{DDQ} terminals.

Table 1. DC Electrical Specifications (V_{DD} = Temperature = 0°C to +85 °C) (continued)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{OH}	Output Voltage, High	V_{DD}/V_{DDQ} = 2.3V to 2.7V, I_{OH} = –100 µA, V_{DD}=2.3 to 2.7V	V_{DD} – 0.2			V
		V_{DD}/V_{DDQ} = 2.3V, I_{OH} = –16 mA	1.95			
I_{IL}	Input Current					
	Data Inputs	V_I = 1.7V or 0.8V, V_{REF} = 1.15V or 1.35V, V_{DD} = 2.7V			±5	µA
		V_I = 2.7V or 0,V_{REF} = 1.15V or 1.35V, V_{DD} = 2.7V			± 5	µA
		V_I = 1.7V or 0.8V, V_{REF} = 1.15V or 1.35V, V_{DD} = 3.6V			± 5	µA
		V_I = 2.7V or 0			± 5	µA
	CLK, $\overline{CLK}$	V_I = 1.7V or 0.8V, V_{REF} = 1.15V or 1.35V			±1	µA
		V_I = 2.7V or 0, V_{REF} = 1.15V or 1.35V, V_{dd} = 2.7V			± 1	µA
	RESET	V_I = V_{DD} or V_{SS}, V_{DD} = 2.7V			± 5	µA
	VREF	V_I = 1.5V or 1.35V, V_{DD} = 2.7			±5	µA
I_{IH}	Input Current, High	Data inputs only				mA.
I_{DD}	Dynamic Supply Current	V_I = 1.7V or 0.8V, I_O = 0, V_{DD} = 2.7V			90	mA
		V_I = 2.7V or 0, I_O = 0, V_{DD} = 2.7V			90	mA
C_{in}	Input pin capacitance					
	RESET	V_I = 1.7V or 0.8V, I_O = 0, V_{DD} = 2.7V		3		pF
	Clock and Data Inputs		2.5	2.7	3.5	pF
L_{pin}	Pin Inductance	All	2.1		4.5	nH

Table 2. AC Input Electrical Specifications (V_{DD} = 2.5 VDC ± 5%, Temperature = 0°C to +85°C)

Parameter	Description	Condition	V_{DD} = 2.5V ± 0.2V		Unit
			Min.	Max.	
F_{IN}	Input Clock Frequency	CLK, $\overline{CLK}$		200	MHz
P_W	Pulse Duration	CLK, $\overline{CLK}$ HIGH or LOW	3.3		ns
T_{ACT}	Differential Inputs Active Time	Data inputs must be LOW after $\overline{RESET}$ HIGH	22		ns
T_{INACT}	Differential Inputs Inactive Time	Data and clock inputs must be held at valid levels (not floating) after $\overline{RESET}$ LOW	22		ns
T_{SET}	Set-up Time	Fast slew rate, (see notes 5 and 7), Data before CLK, $\overline{CLK}$	0.75		ns
		Slow slew rate, (see notes 6 and 7), Data before CLK, $\overline{CLK}$	0.9		ns
T_{HOLD}	Hold Time	Fast slew rate, (see notes 5 and 7), Data after CLK, $\overline{CLK}$	0.75		ns
		Slow slew rate (see notes 6 and 7), Data after CLK, $\overline{CLK}$	0.9		ns
I_{Vpp}	Input Voltage, Pk–Pk		360		mV

Notes:
5. For data signal input slew rate > 1 V/ns.
6. For data signal input slew rate > 0.5 V/ns and < 1 V/ns.
7. CLK, $\overline{CLK}$ signals input slew rates are > 1 V/ns.

Table 3. AC Output Electrical Specifications (V_{DD} = 2.5V VDC ± 5%, Temperature = 0°C to +85°C)

Parameter	Description	Condition	V_{DD} = 2.5V ± 0.2V		Unit
			Min.	Max.	
F_{MAX}				280	
T_{DEL}	Propagation Delay from CLK/$\overline{CLK}$ to Q	Q	1.1	2.8	ns
T_{PHL}	RESET	Q		4.3	ns
T_R	Rise Time	Any Q	0.85	4	V/ns
T_F	Fall time	Any Q	1.0	4	V/ns

Output Buffer Characteristics

Table 4. Output Buffer Voltage vs. Current (V/I) Characteristics

Voltage (V)	Pull-Down		Pull-Up	
	Min I (mA)	Max I (mA)	Min I (mA)	Max I (mA)
0	0	0	0	0
0.1	6	13	–5	–15
0.2	10	25	–10	–27
0.3	15	38	–15	–38
0.4	19	49	–19	–49
0.5	23	60	–23	–60
0.6	27	71	–28	–72
0.7	30	81	–31	–83
0.8	34	91	–35	–96
0.9	36	100	–38	–104
1.0	38	108	–40	–112
1.1	40	115	–44	–120
1.2	42	123	–46	–125
1.3	43	130	–48	–130
1.4	44	137	–50	–134
1.5	44	144	–51	–137
1.6	45	150	–52	–140
1.7	45	158	–52	–143
1.8	45	165	–52	–146
1.9	45	172	–53	–149
2.0	45	179	–53	–152
2.1	46	185	–53	–154
2.2	46	191	–54	–156
2.3	46	196	–54	–157
2.4	46	201	–54	–159
2.5	46	206	–54	–160
2.6	46	211	–55	–161
2.7	46	216	–55	–162

Slew Rate

The following table describes output-buffer slew-rate characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these rates is not mandatory if it can be adequately demonstrated that alternate characteristics meet the requirements of the registered DDR DIMM application. This information does not necessarily have to appear in the device data sheet.

Obtain rise and fall time measurements by using the same procedure for obtaining "Ramp" data according to the current WIA IBIS specification. In particular it is very important to note that the following slew rates are specified at the output of the die, without package parasitics in the power, ground or output paths. The measurement points are at 20% and 80%. The slew-rate test load shall be a 50-ohm resistor to GND for Rise and a 50-ohm resistor to V_{DDQ} for fall. The dV/dt ratio is reduced to V/ns.

Table 5. Output Buffer Slew-Rate Characteristics

dV/dt	Min.	Max.
Rise	0.85 V/ns	4 V/ns
Fall	1.00 V/ns	4 V/ns

Test Configurations[9, 10]

V_{DD} = 2.5V ±0.2V

Timing Diagrams

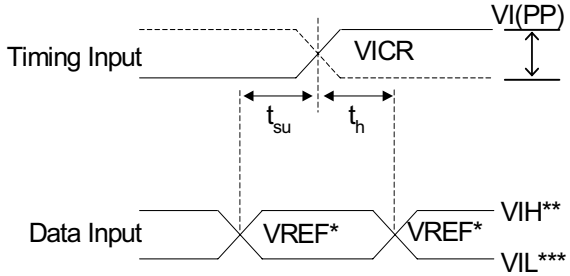


Figure 1. Voltage Waveforms Set-up and Hold Times[11, 13, 14]

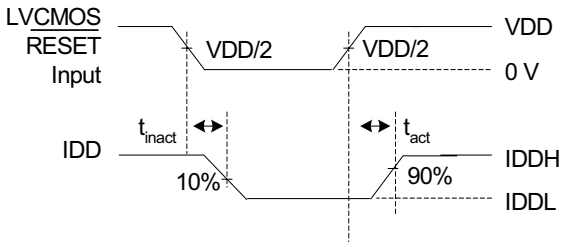


Figure 2. Voltage Waveforms Enable and Disable Times Low- and High-level Enabling[11]

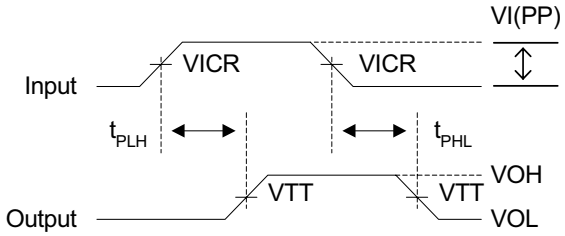


Figure 3. Voltage Waveforms Propagation Delay Times[12]

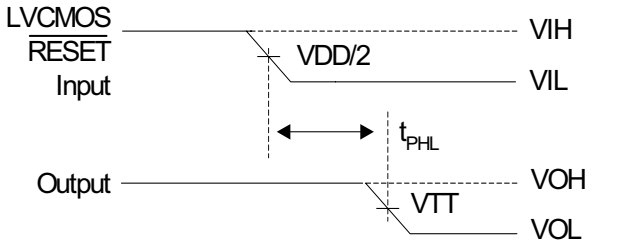


Figure 4. Voltage Waveforms Propagation Delay Times[11

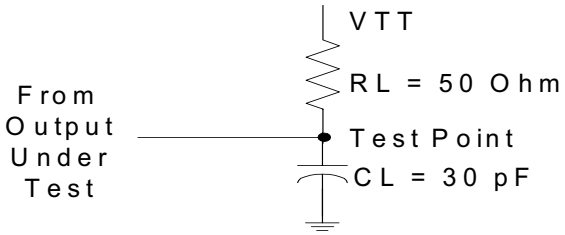


Figure 5. Load Circuit[8]

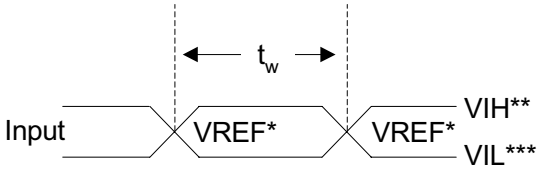


Figure 6. Voltage Waveforms Pulse Duration[13, 14]

Notes:
8. CL includes probe and jig capacitance.
9. IDD tested with clock and data inputs held at VDD or VSS, and IO = 0 mA.
10. All input pulses are supplied by generators having the following characteristics: PRR < 10 MHz, ZO = 50 ohm input slew rate = 1 V/ns ±20% (unless otherwise specified).
11. the outputs are measured one at a time with one transition per measurement.
12. *VTT = VREF = VDDQ/2.
13. **VIH = VREF + 350 mV (AC voltage levels).
14. ***VIL = VREF – 350 mV (AC voltage levels).

Ordering Information

Part Number	Package Type	Product Flow
CY2SSTV16857ZC	48-pin TSSOP	Commercial, 0° to 70°C
CY2SSTV16857ZCT	48-pin TSSOP –Tape and Reel	Commercial, 0° to 70°C
CY2SSTV16857ZI	48-pin TSSOP	Industrial, –40° to 85°C
CY2SSTV16857ZIT	48-pin TSSOP –Tape and Reel	Industrial, –40° to 85°C
Lead-Free		
CY2SSTV16857ZXC	48-pin TSSOP	Commercial, 0° to 70°C
CY2SSTV16857ZXCT	48-pin TSSOP –Tape and Reel	Commercial, 0° to 70°C
CY2SSTV16857ZXI	48-pin TSSOP	Industrial, –40° to 85°C
CY2SSTV16857ZXIT	48-pin TSSOP –Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensiona

48-lead (240-mil) TSSOP II Z4824