

MOS FIELD EFFECT TRANSISTOR

NP84N055ELE, NP84N055KLE
NP84N055CLE, NP84N055DLE, NP84N055MLE, NP84N055NLE

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

<R> ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP84N055ELE-E1-AY ^{Note1, 2}	Pure Sn (Tin)	Tape 800 p/reel	TO-263 (MP-25ZJ) typ. 1.4 g
NP84N055ELE-E2-AY ^{Note1, 2}			
NP84N055KLE-E1-AY ^{Note1}			TO-263 (MP-25ZK) typ. 1.5 g
NP84N055KLE-E2-AY ^{Note1}			
NP84N055CLE-S12-AZ ^{Note1, 2}	Sn-Ag-Cu	Tube 50 p/tube	TO-220 (MP-25) typ. 1.9 g
NP84N055DLE-S12-AY ^{Note1, 2}	Pure Sn (Tin)		TO-262 (MP-25 Fin Cut) typ. 1.8 g
NP84N055MLE-S18-AY ^{Note1}			TO-220 (MP-25K) typ. 1.9 g
NP84N055NLE-S18-AY ^{Note1}			TO-262 (MP-25SK) typ. 1.8 g

Notes 1. Pb-free (This product does not contain Pb in the external electrode.)

2. Not for new design

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance

$R_{DS(on)1} = 7.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 42 \text{ A)}$

$R_{DS(on)2} = 8.7 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5 \text{ V, } I_D = 42 \text{ A)}$

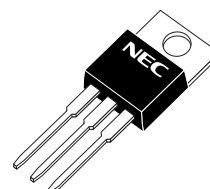
$R_{DS(on)3} = 9.4 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 42 \text{ A)}$

- Low input capacitance

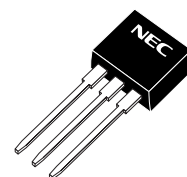
$C_{iss} = 6130 \text{ pF TYP.}$

- Built-in gate protection diode

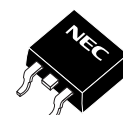
(TO-220)



(TO-262)



(TO-263)



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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	55	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C) ^{Note1}	I _{D(DC)}	±84	A
Drain Current (pulse) ^{Note2}	I _{D(pulse)}	±336	A
Total Power Dissipation (T _A = 25°C)	P _T	1.8	W
Total Power Dissipation (T _C = 25°C)	P _T	200	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	–55 to +175	°C
Single Avalanche Current ^{Note3}	I _{AS}	84/55/20	A
Single Avalanche Energy ^{Note3}	E _{AS}	70/302/400	mJ

Notes 1. Calculated constant current according to MAX. allowable channel temperature.

2. PW ≤ 10 μs, Duty cycle ≤ 1%

3. Starting T_{ch} = 25°C, V_{DD} = 28 V, R_G = 25 Ω, V_{GS} = 20 → 0 V (See **Figure 4.**)

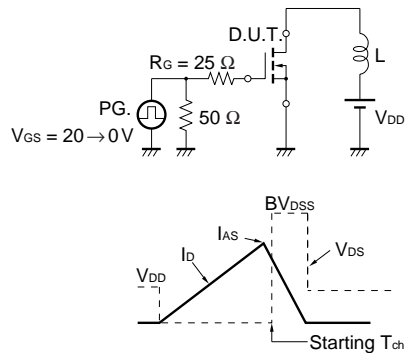
THERMAL RESISTANCE

Channel to Case Thermal Resistance	R _{th(ch-C)}	0.75	°C/W
Channel to Ambient Thermal Resistance	R _{th(ch-A)}	83.3	°C/W

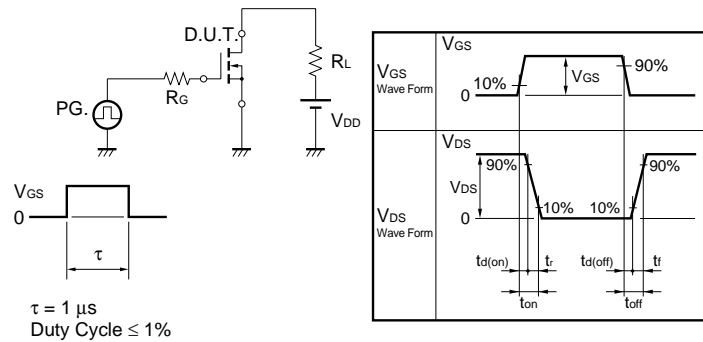
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 42 A	27	58		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 42 A		5.6	7.0	mΩ
	R _{DS(on)2}	V _{GS} = 5 V, I _D = 42 A		6.5	8.7	mΩ
	R _{DS(on)3}	V _{GS} = 4.5 V, I _D = 42 A		7.0	9.4	mΩ
Input Capacitance	C _{iss}	V _{DS} = 25 V,		6130	9200	pF
Output Capacitance	C _{oss}	V _{GS} = 0 V,		710	1070	pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		350	630	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 28 V, I _D = 42 A,		29	64	ns
Rise Time	t _r	V _{GS} = 10 V,		19	47	ns
Turn-off Delay Time	t _{d(off)}	R _G = 1 Ω		120	230	ns
Fall Time	t _f			21	53	ns
Total Gate Charge	Q _{G1}	V _{DD} = 44 V, V _{GS} = 10 V, I _D = 84 A		120	180	nC
	Q _{G2}	V _{DD} = 44 V,		65	98	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 5 V,		18		nC
Gate to Drain Charge	Q _{GD}	I _D = 84 A		33		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 84 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 84 A, V _{GS} = 0 V,		49		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		78		nC

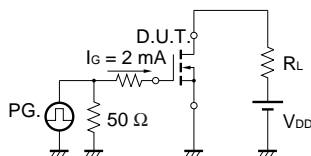
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

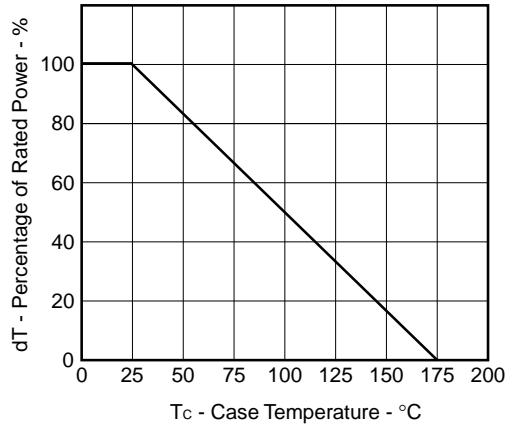


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

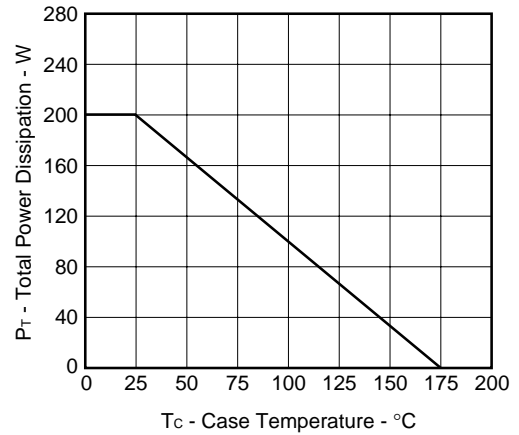


Figure3. FORWARD BIAS SAFE OPERATING AREA

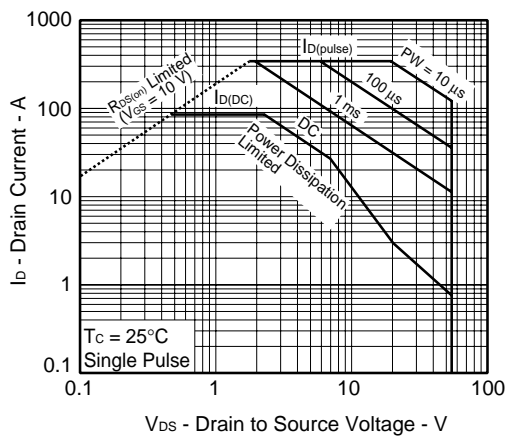


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

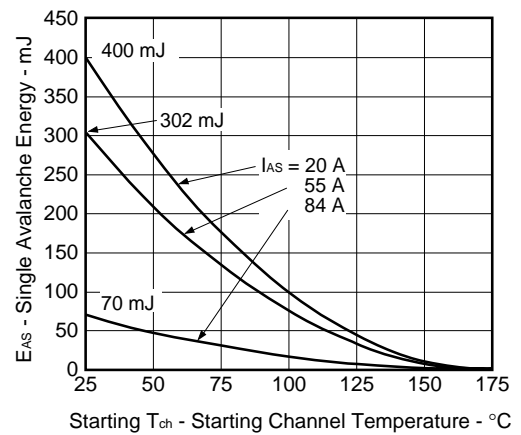


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

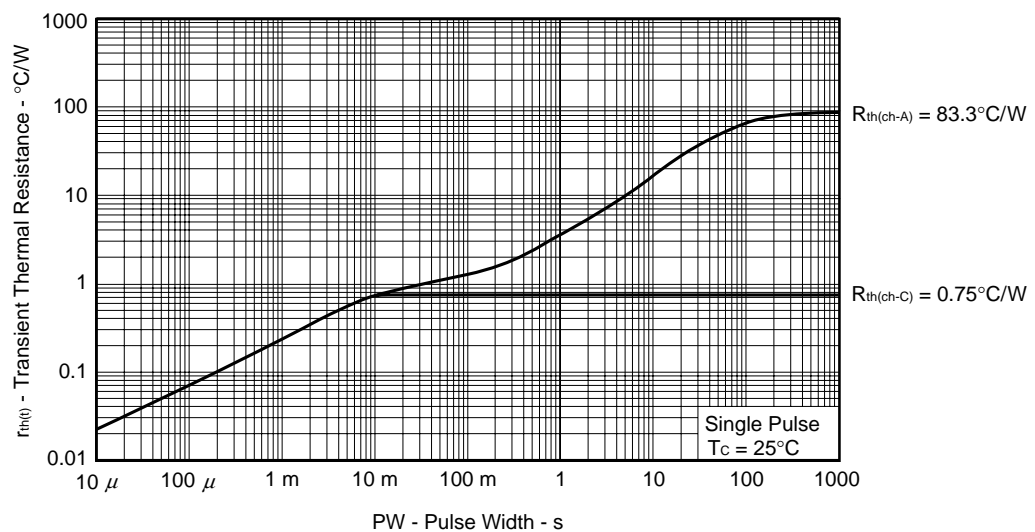


Figure6. FORWARD TRANSFER CHARACTERISTICS

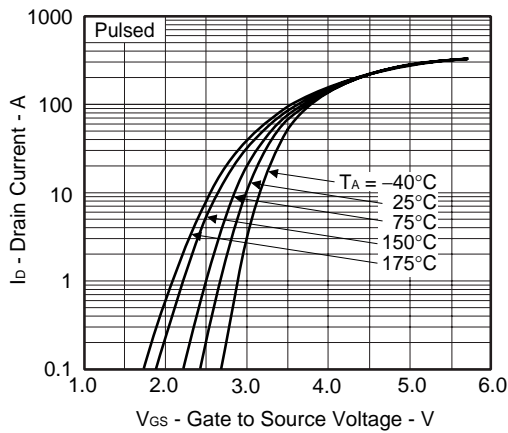


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

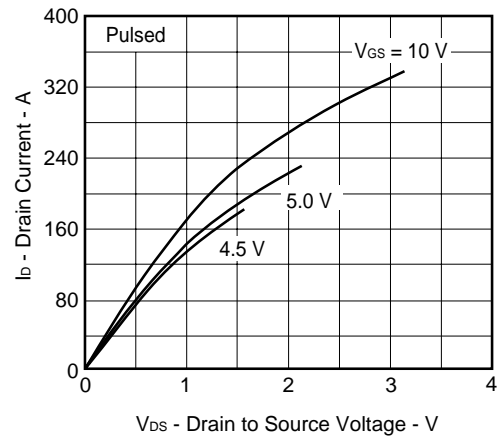


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

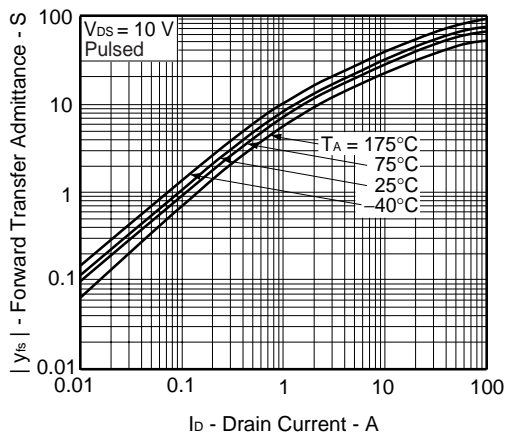


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

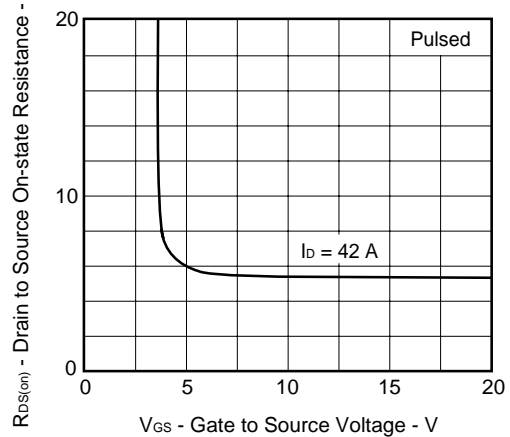


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

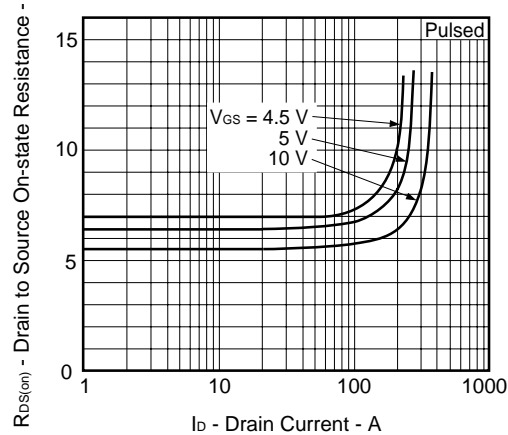


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

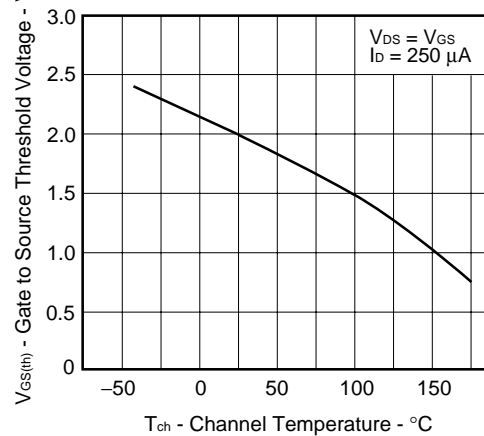


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

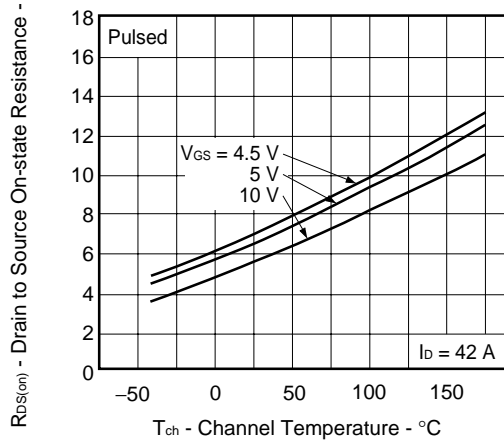


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

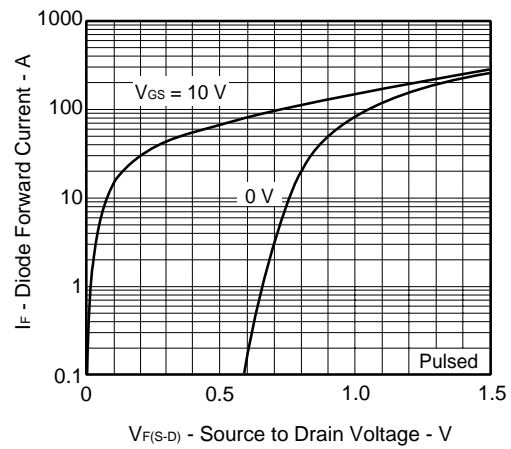


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

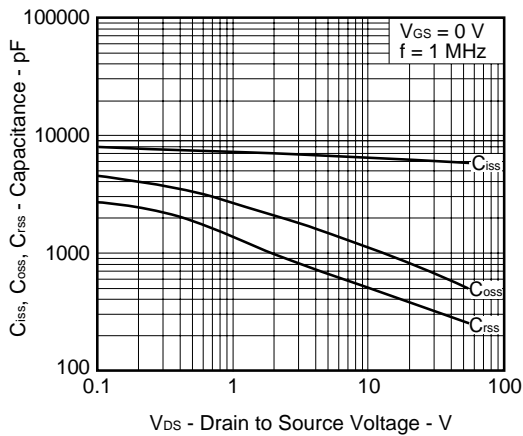


Figure15. SWITCHING CHARACTERISTICS

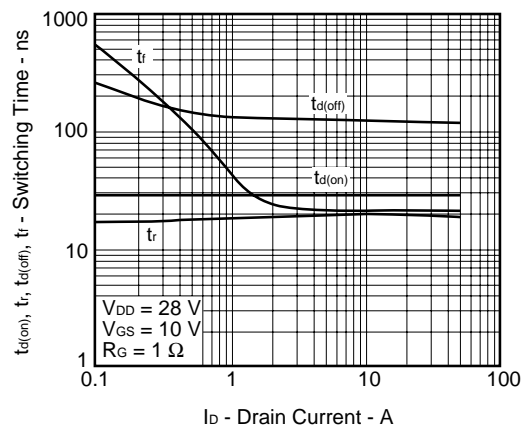


Figure16. REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

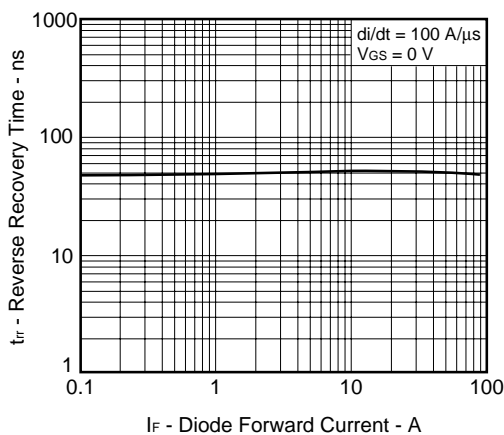
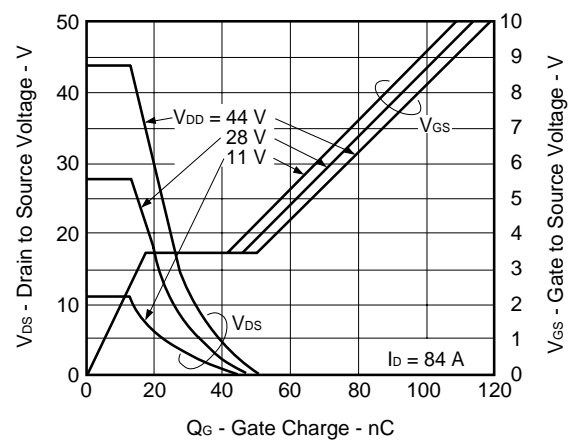
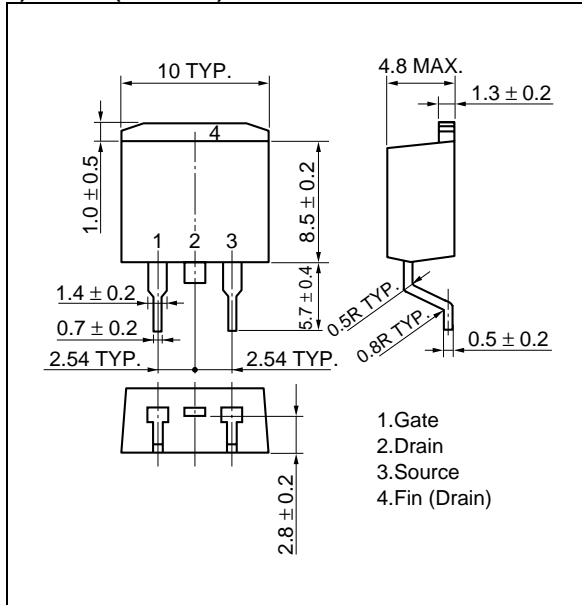


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

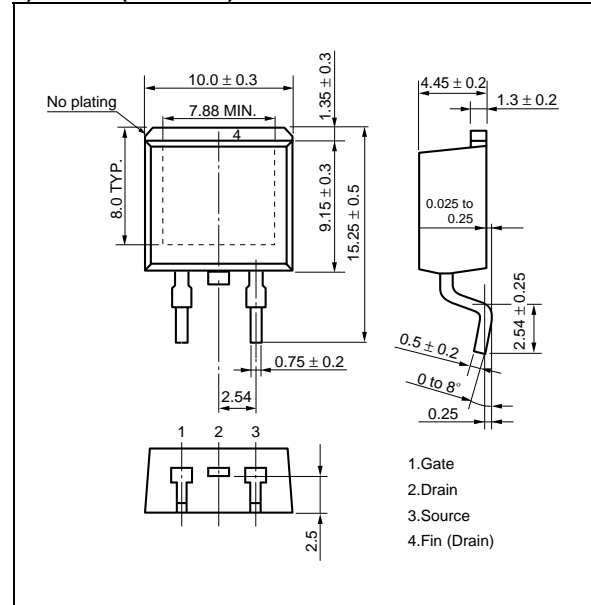


<R> PACKAGE DRAWINGS (Unit: mm)

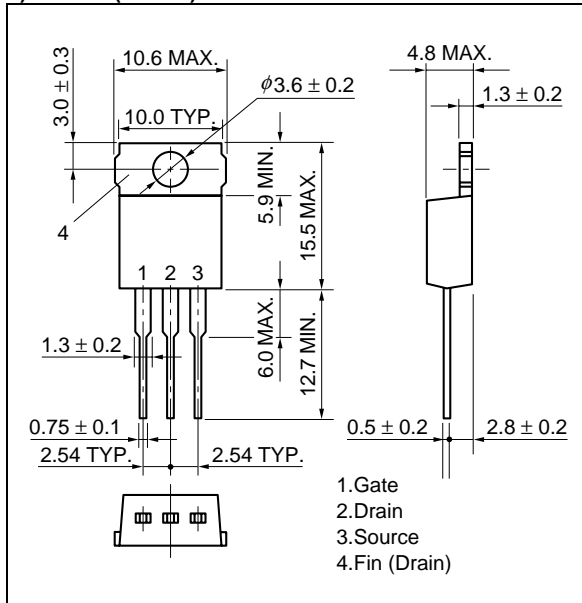
1) TO-263 (MP-25ZJ) ^{Note}



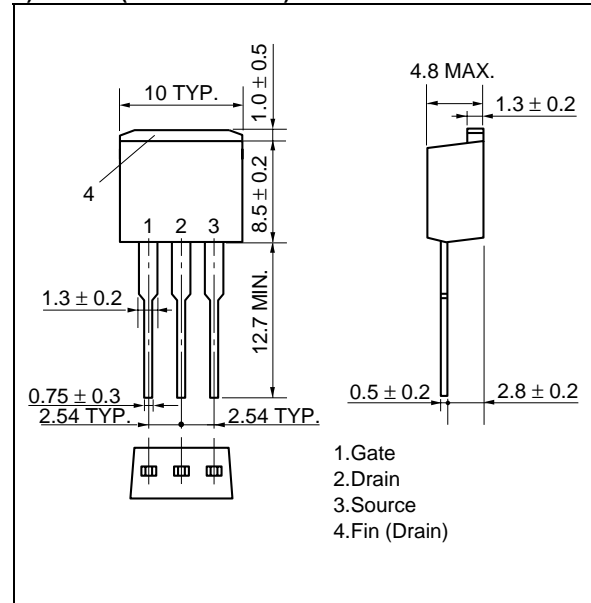
2) TO-263 (MP-25ZK)



3) TO-220 (MP-25) ^{Note}

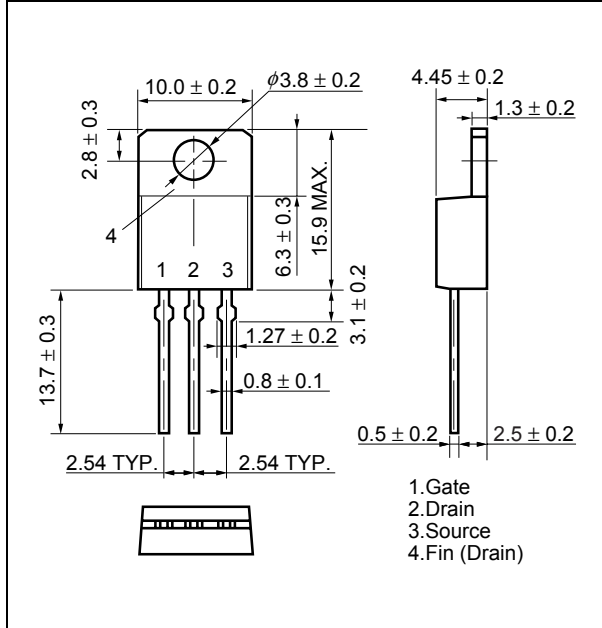


4) TO-262 (MP-25 Fin Cut) ^{Note}

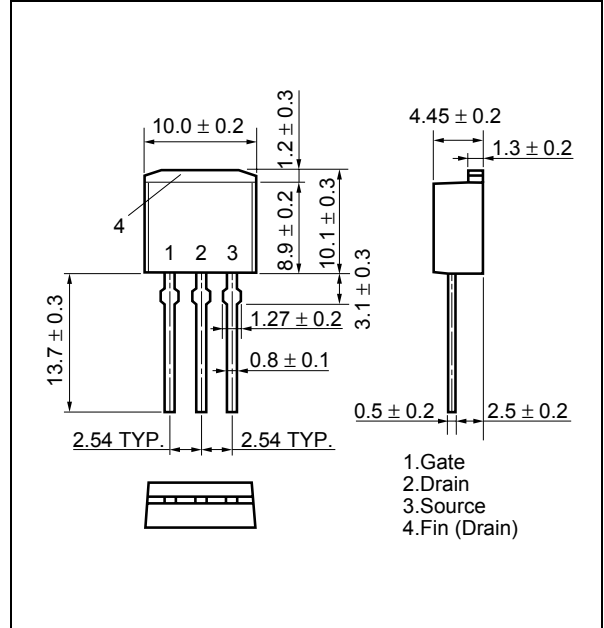


Note Not for new design

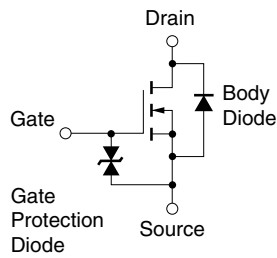
5)TO-220 (MP-25K)



6)TO-262 (MP-25SK)



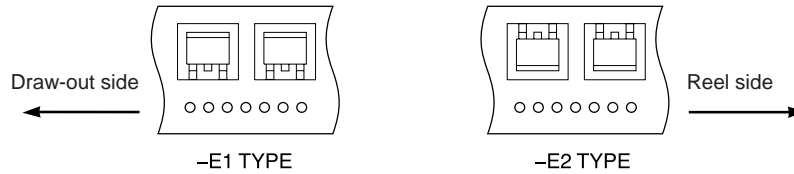
EQUIVALENT CIRCUIT



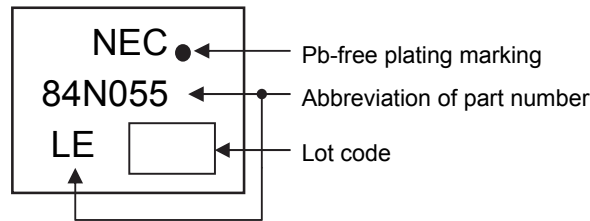
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

<R> TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



<R> MARKING INFORMATION



<R> RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow MP-25ZJ, MP-25ZK	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Wave soldering MP-25, MP-25K, MP-25SK, MP-25 Fin Cut	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating MP-25ZJ, MP-25ZK, MP-25K, MP-25SK	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350
Partial heating MP-25, MP-25 Fin Cut	Maximum temperature (Pin temperature): 300°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P300

Caution Do not use different soldering methods together (except for partial heating).

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