

SILICON MMIC UPCONVERTER WITH AGC + IQ MODULATOR

UPC8125GR

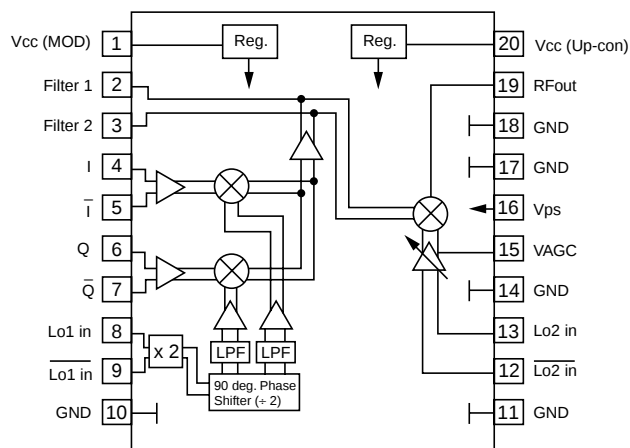
FEATURES

- **WIDE SUPPLY VOLTAGE RANGE:** 2.7 to 5.5 V
- **OUTPUT FREQUENCY RANGE:** 1.8 to 2.0 GHz
- **INTERNAL LPF TO REJECT LO & SPURIOUS LEAKAGE**
- **PORTS FOR EXTERNAL IF FILTER**
- **AGC FUNCTION:** 40 dB RANGE
- **POWER SAVE FUNCTION**
- **SMALL 20 PIN SSOP PACKAGE**
- **TAPE AND REEL PACKAGING AVAILABLE**

DESCRIPTION

The UPC8125GR is a Silicon MMIC manufactured with the NESAT™ III silicon bipolar process. The IC consists of a 1.8 - 2.0 GHz upconverter with AGC function and a 220 - 270 MHz IQ modulator. The device operates over a wide 2.7 - 5.5 V supply voltage range and features a power save function. The device

INTERNAL BLOCK DIAGRAM



was specifically designed for digital mobile communication applications such as 1900 MHz PCS and PHS handsets.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (TA = 25°C, VCC = VPS = 3.0 V, unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPC8125GR S20 (SSOP 20)		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Icc	Total Circuit Current (no input signal)	mA	30	36	48
Icc(PS)	Total Circuit Current at Sleep Mode VPS ≤ 0.5 V (Low)	μA		0.3	10
PRFout 1	Total Output Power 1 VAGC = 3.0 V	dBm	-13	-9	-5
PRFout 2	Total Output Power 2 VAGC = 0.5 V	dBm		-50	
LoL	Lo Carrier Leak ¹ fLo1 + fLo2	dBc		-37	-30
ImR	Image Rejection (Side Band leak) ¹	dBc		-35	-30
IM3 I/Q	I/Q 3rd Order Intermodulation Distortion ¹	dBc		-50	-30
GCR	AGC Amp. Gain control range VAGC = 2.5 V to 0 V	dB	28	40	
TPS(RISE)	Power Save Rise Time VPS (OFF) → VPS (ON)	μS		2	5
TPS (FALL)	Power Save Fall Time VPS (ON) → VPS (OFF)	μS		5	10
ZI/Q	Input Impedance I and Q Ports fI/Q = 24 kHz, I → I-bar, Q → Q-bar	kΩ		200	
II/Q	I/Q Bias Current I → I-bar, Q → Q-bar	μA		5	
ZLo1	Lo1 Input VSWR fLo1= 220 MHz to 270 MHz			1.2:1	
EVM	Error Vector Magnitude MOD Pattern : PN9	%rms		2.5	4.5
Padj	Adjacent Channel Power Δf = 600 KHz MOD Pattern : PN9	dBc		-68	-60

Notes:

1. VI/Q = 1.5 V (DC) +0.5 Vp-p (AC)

ABSOLUTE MAXIMUM RATINGS¹ ($T_A = 25^\circ\text{C}$)

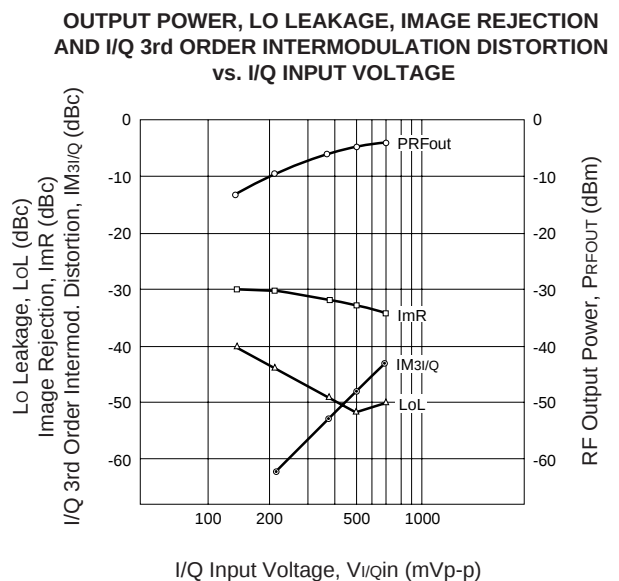
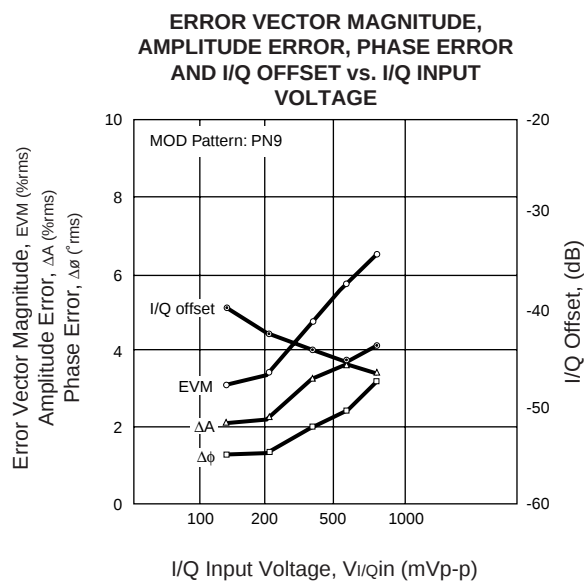
SYMBOLS	PARAMETERS	UNITS	RATINGS
V _{CC}	Supply Voltage	V	6.0
V _{PS}	Power Save Control Voltage	V	6.0
V _{AGC}	AGC Control Voltage	V	6.0
P _D	Power Dissipation ²	mW	430
T _{OP}	Operating Temperature	°C	-40 to +85
T _{STG}	Storage Temperature	°C	-55 to +150

Notes:

- Operation in excess of any one of these conditions may result in permanent damage.
- $T_A = 85^\circ\text{C}$ Mounted on a 50x50x1.6 mm double copper clad epoxy glass board.

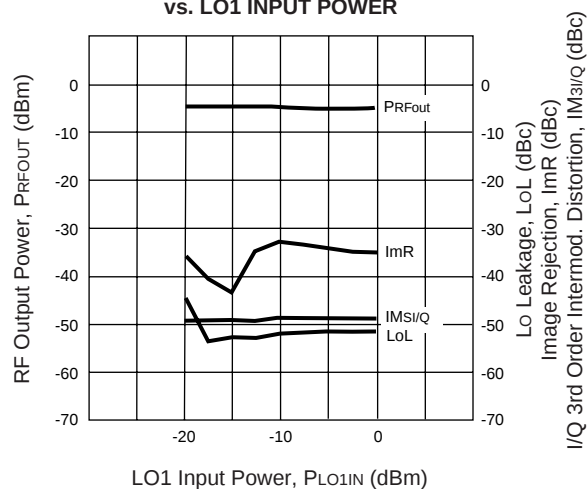
RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V _{CC}	Supply Voltage	V	2.7	3.0	5.5
T _{OP}	Operating Temperature	°C	-40	+25	+85
f _{RFout}	Up Converter RF Frequency	GHz	1.8		2.0
f _{UPCONin}	Up Converter Input Freq.	MHz	220		270
f _{MODout}	Modulator Output Frequency				
f _{LO1in}	Lo1 Input Frequency, P _{LO1in} = -10 dBm				
f _{LO2in}	Lo2 Input Frequency, P _{LO2in} = -10 dBm	MHz	1500		1800
f _{I/Qin}	I/Q Input Frequency, V _{I/Qin} = 500 mVp-p MAX (Single ended)	MHz	DC		10
P _{LO1in}	Lo1 Input Level	dBm	-11.5	-10	-5
P _{LO2in}	Lo2 Input Level	dBm	-15	-10	-5
V _{I/Qin}	I/Q Input Amplitude, Single ended Input	mVp-p			500
	Differential Input				250

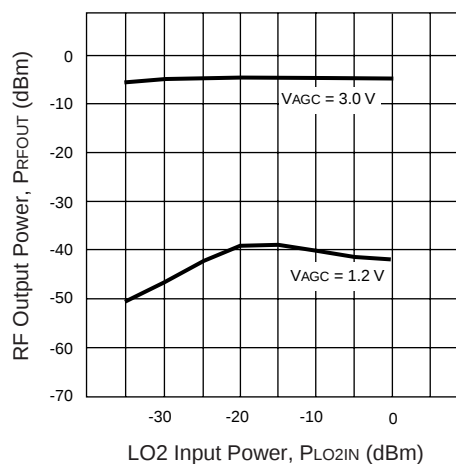
TYPICAL PERFORMANCE CURVES ($T_A = 25^\circ\text{C}$, $V_{CC} = V_{PS} = V_{AGC} = 3.0\text{ V}$, I/Q DC Offset = $\bar{I}/\bar{Q}$ DC Offset = 1.5 V, I/Q Input Signal = 500 mVp-p (Single-ended), LO1 = 250 MHz, P_{LO1} = -10 dBm, LO2 = 1650 MHz, P_{LO2} = -10 dBm, R_{FOUT} = 1900 MHz + f_{I/Q} unless otherwise specified)


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

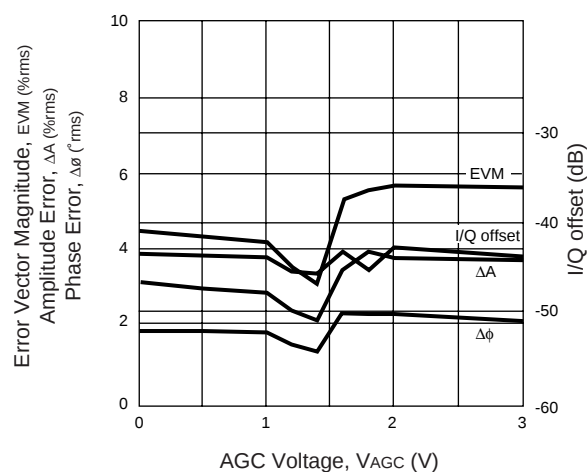
**OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION
AND I/Q 3rd ORDER INTERMODULATION DISTORTION
vs. LO1 INPUT POWER**



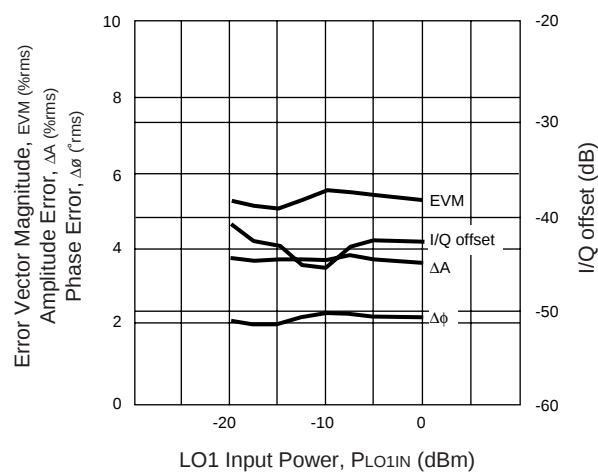
**OUTPUT POWER vs.
LO2 INPUT POWER AND VAGC**



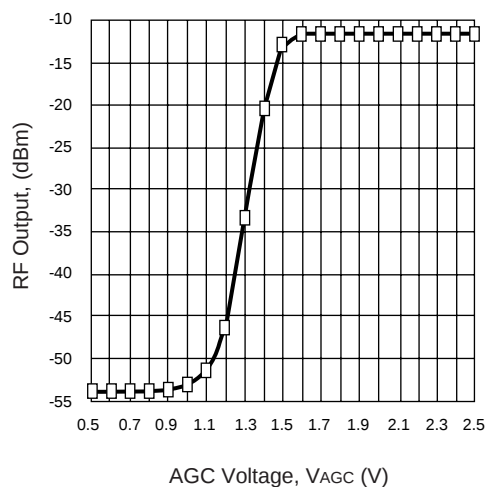
**ERROR VECTOR MAGNITUDE,
AMPLITUDE ERROR, PHASE ERROR,
AND I/Q OFFSET vs. AGC VOLTAGE**



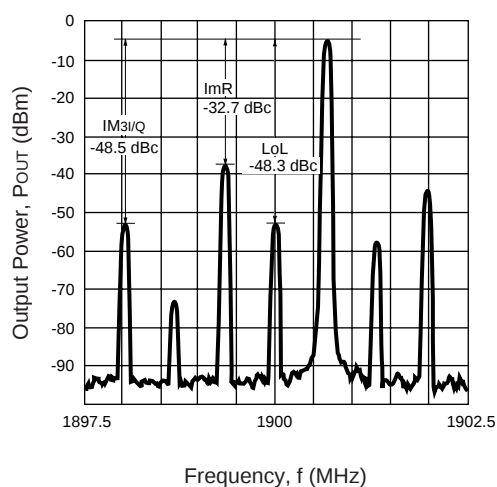
**ERROR VECTOR MAGNITUDE,
AMPLITUDE ERROR, PHASE ERROR,
AND I/Q OFFSET vs. LO1 INPUT POWER**



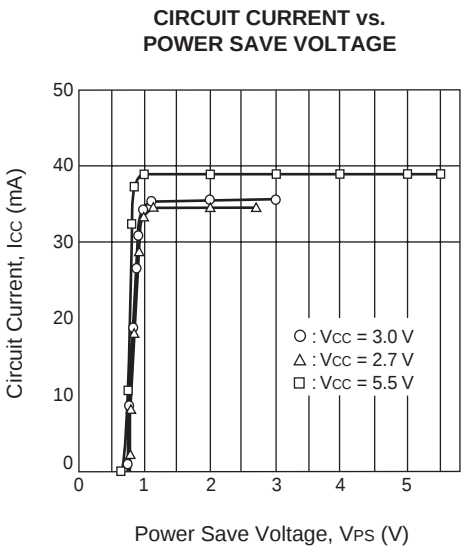
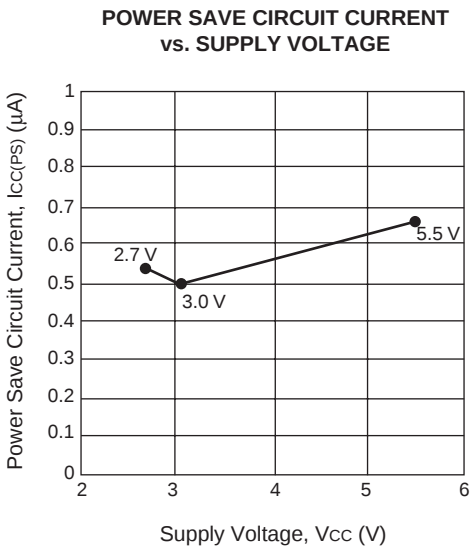
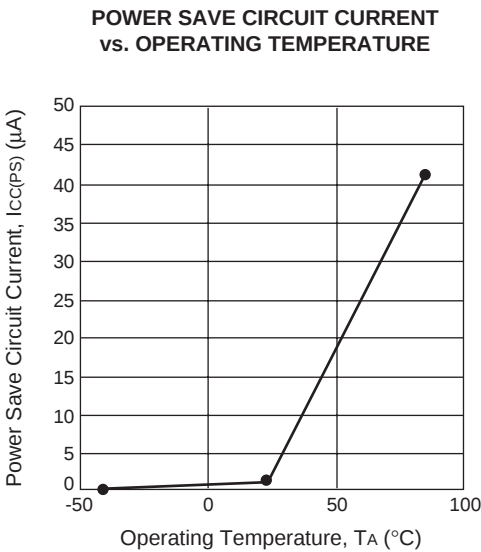
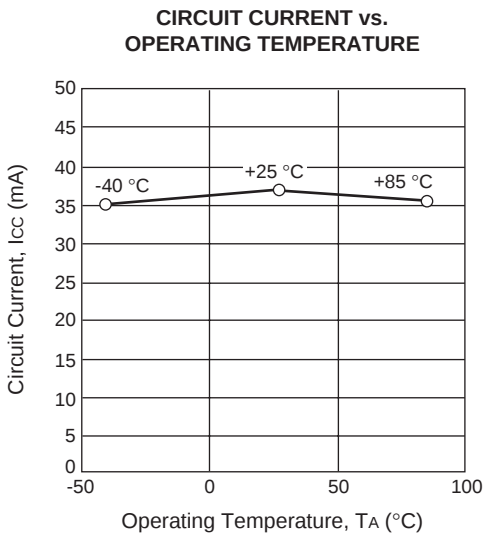
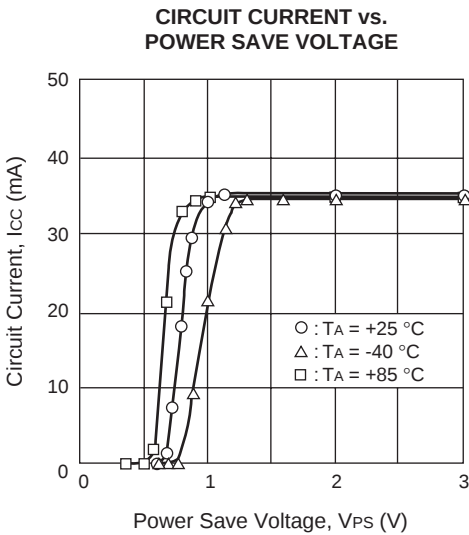
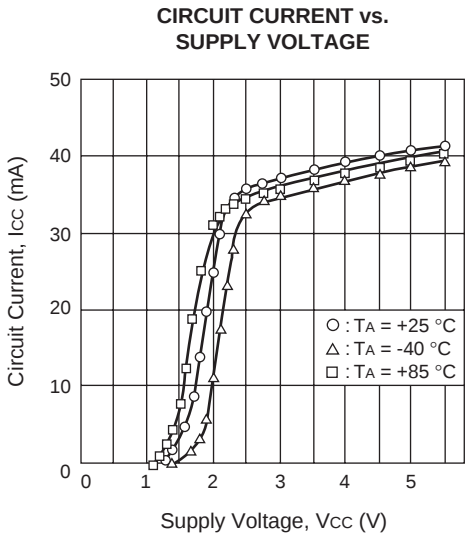
RF OUTPUT vs. AGC VOLTAGE



TYPICAL OUTPUT SPECTRUM

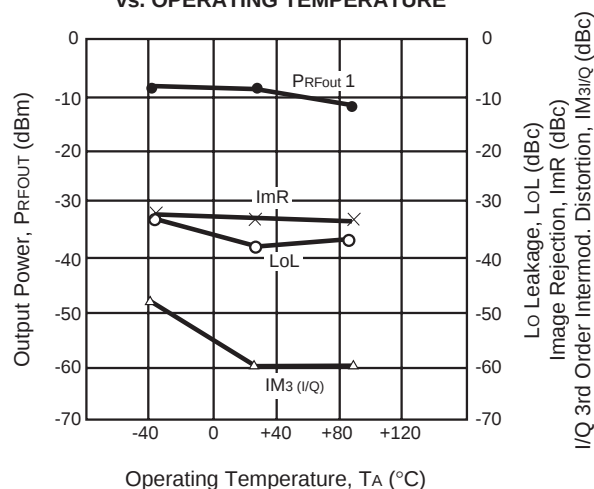


TYPICAL PERFORMANCE CURVES (TA = 25°C)

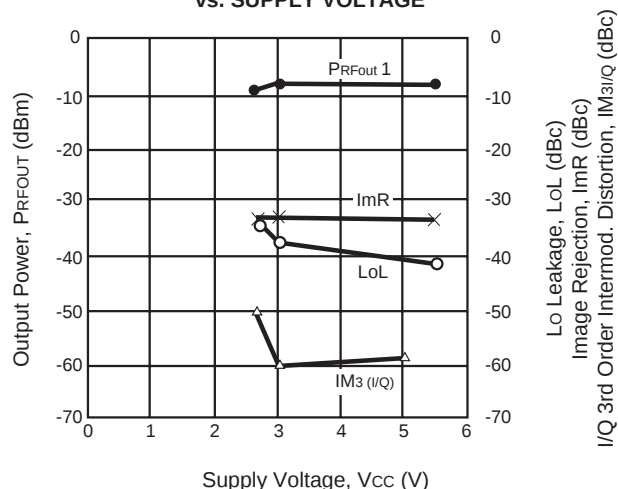


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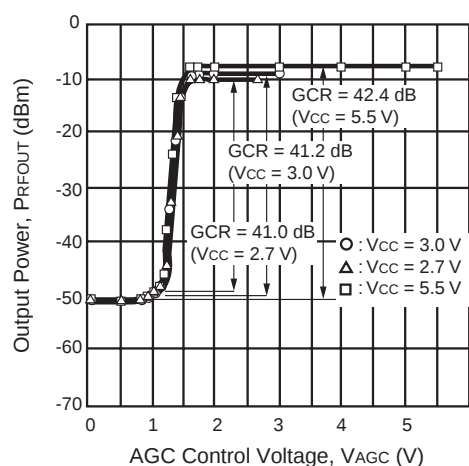
OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION
AND I/Q 3rd ORDER INTERMODULATION DISTORTION
vs. OPERATING TEMPERATURE



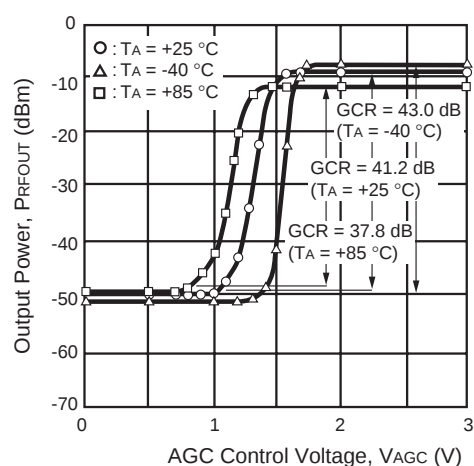
OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION AND I/Q
3rd ORDER INTERMODULATION DISTORTION
vs. SUPPLY VOLTAGE



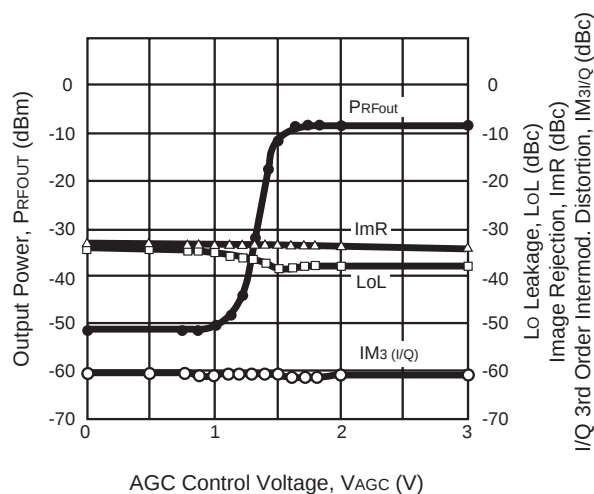
OUTPUT POWER vs.
AGC CONTROL VOLTAGE



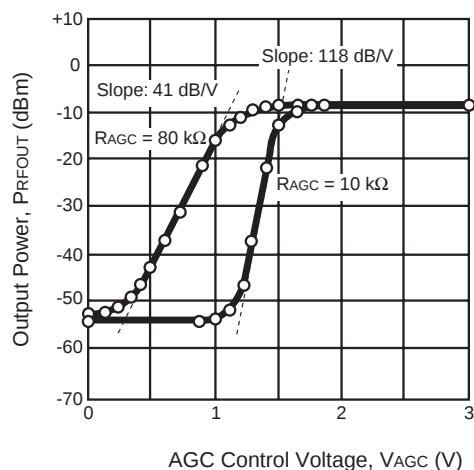
OUTPUT POWER vs.
AGC CONTROL VOLTAGE



OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION
AND I/Q 3rd ORDER INTERMODULATION DISTORTION
vs. AGC CONTROL VOLTAGE

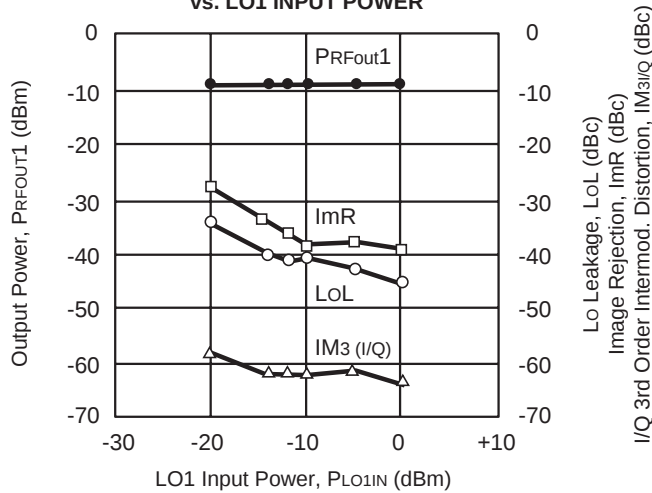


OUTPUT POWER vs.
AGC CONTROL VOLTAGE

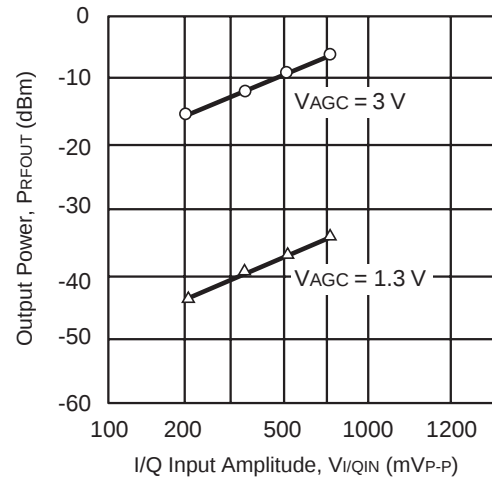


TYPICAL PERFORMANCE CURVES ($T_A = 25^\circ\text{C}$)

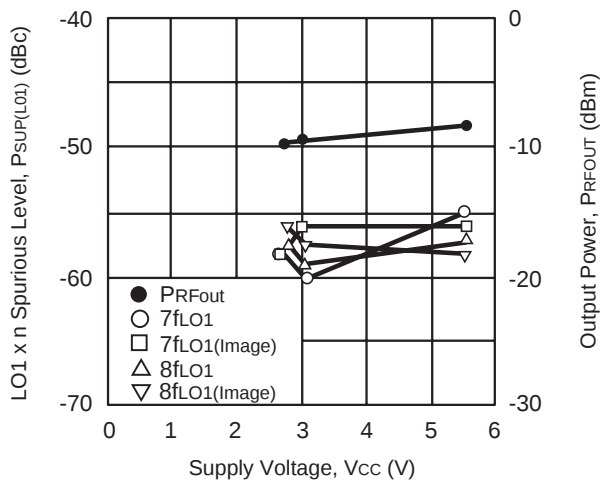
OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION
AND I/Q 3rd ORDER INTERMODULATION DISTORTION
vs. LO1 INPUT POWER



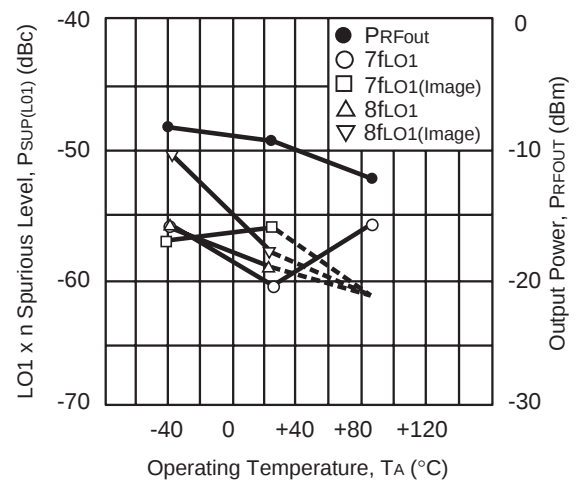
OUTPUT POWER vs.
I/Q INPUT AMPLITUDE



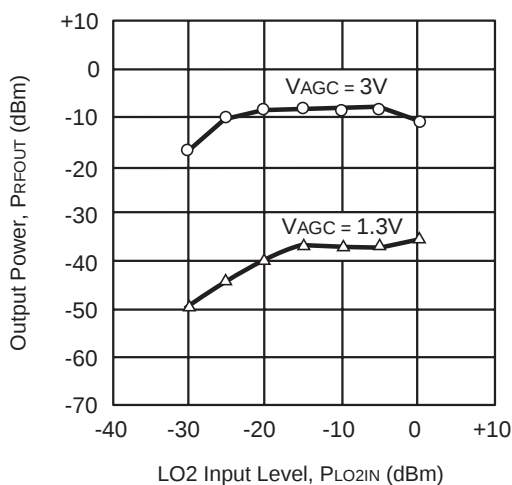
LO1 x n SPURIOUS LEVEL,
OUTPUT POWER
vs. SUPPLY VOLTAGE



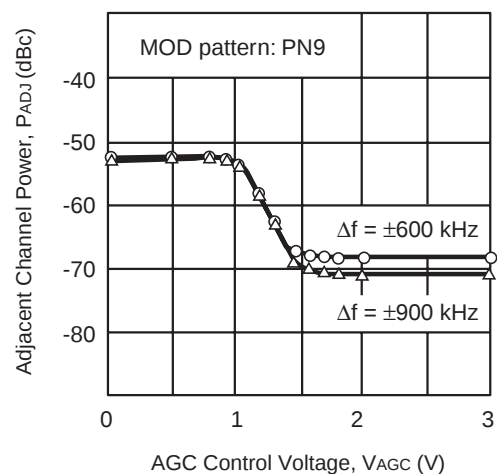
LO1 x n SPURIOUS LEVEL,
OUTPUT POWER
vs. OPERATING TEMPERATURE



OUTPUT POWER vs.
LO2 INPUT LEVEL

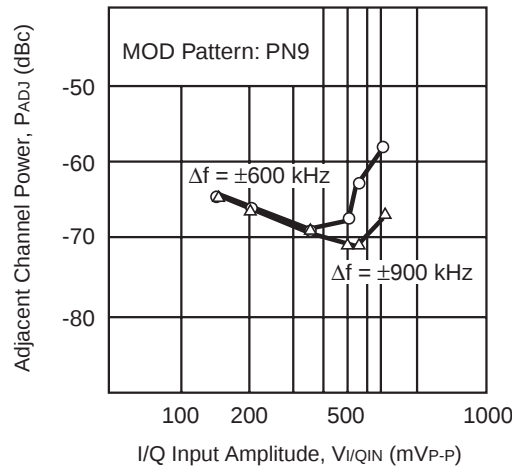


ADJACENT CHANNEL POWER vs.
AGC CONTROL VOLTAGE

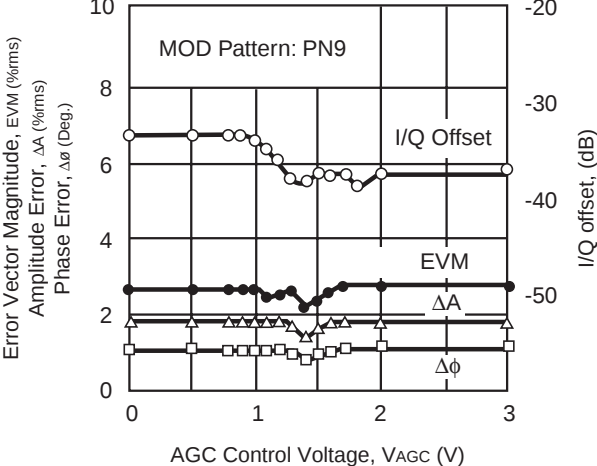


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

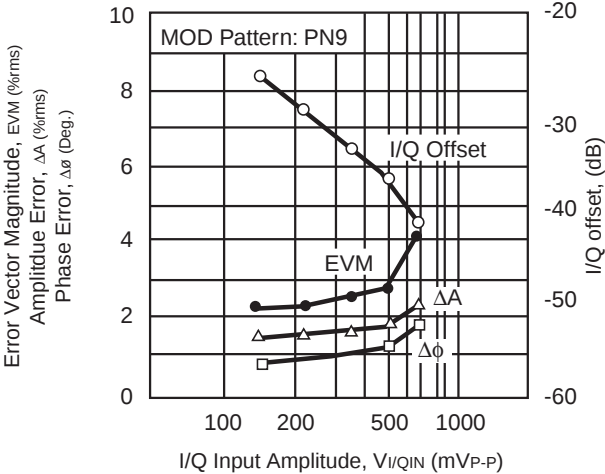
ADJACENT CHANNEL POWER
vs. I/Q INPUT AMPLITUDE



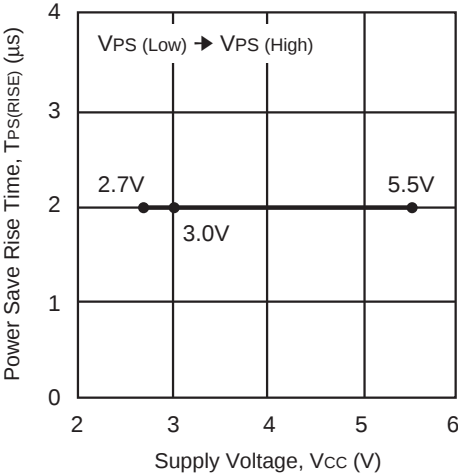
ERROR VECTOR MAGNITUDE, AMPLITUDE
ERROR, PHASE ERROR, AND I/Q OFFSET
vs. AGC CONTROL VOLTAGE



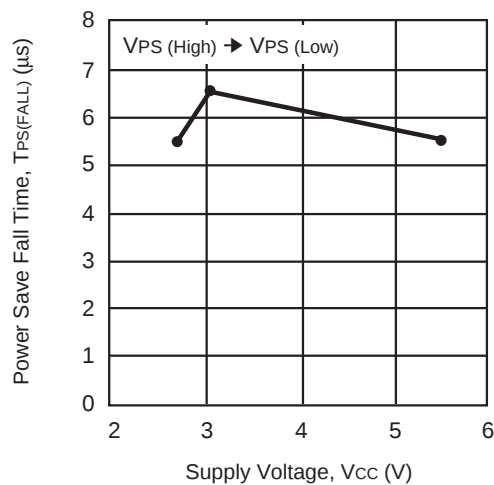
ERROR VECTOR MAGNITUDE,
AMPLITUDE ERROR, PHASE ERROR,
AND I/Q OFFSET vs. I/Q INPUT AMPLITUDE



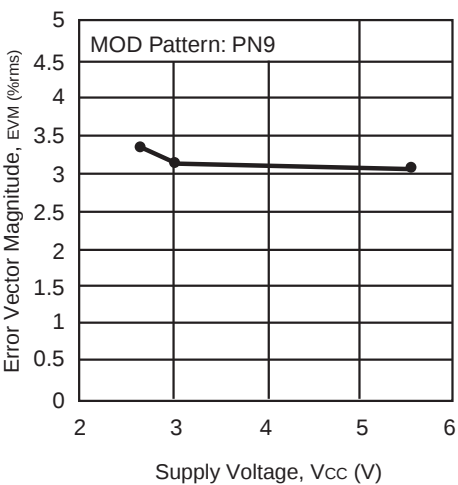
POWER SAVE RISE TIME
vs. SUPPLY VOLTAGE



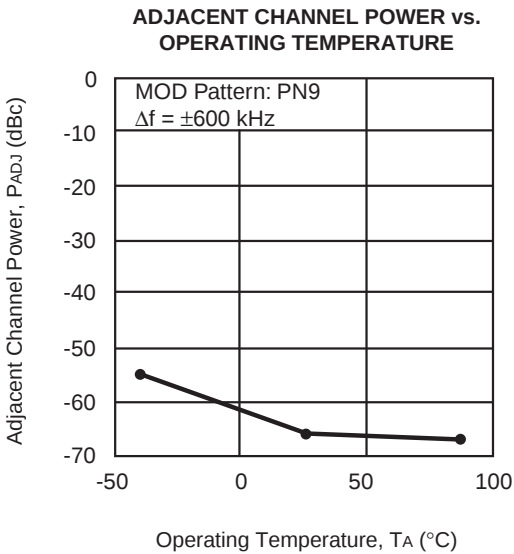
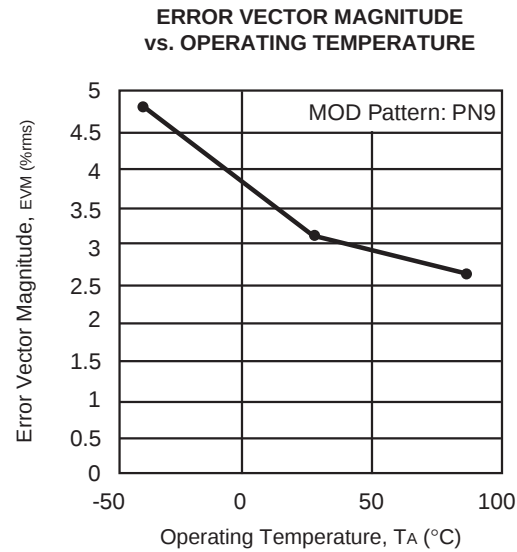
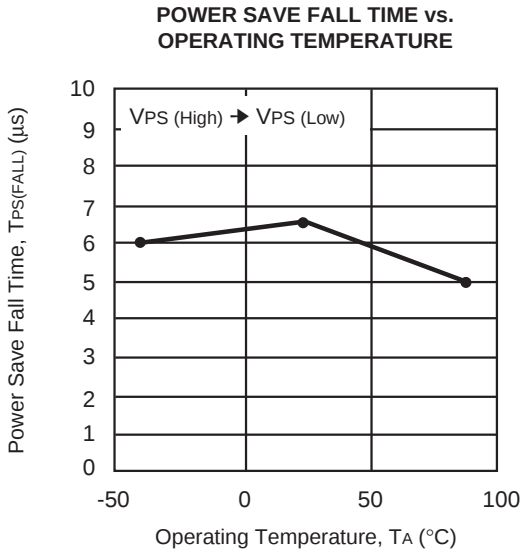
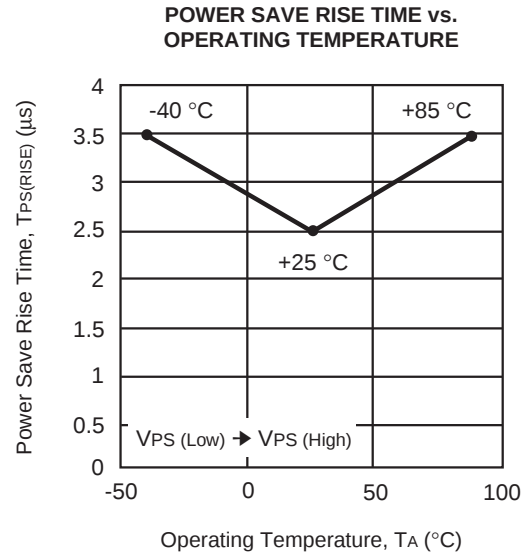
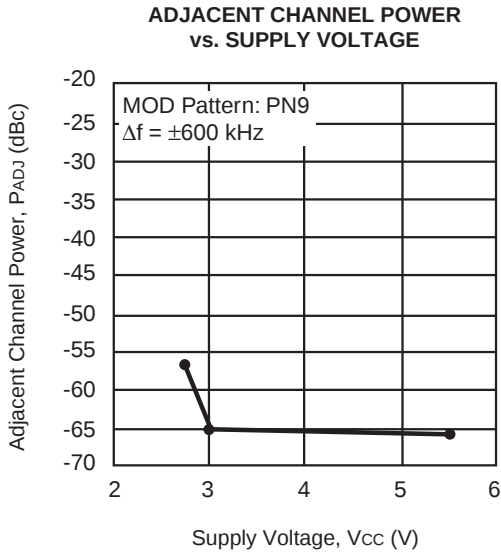
POWER SAVE FALL TIME
vs. SUPPLY VOLTAGE



ERROR VECTOR MAGNITUDE
vs. SUPPLY VOLTAGE

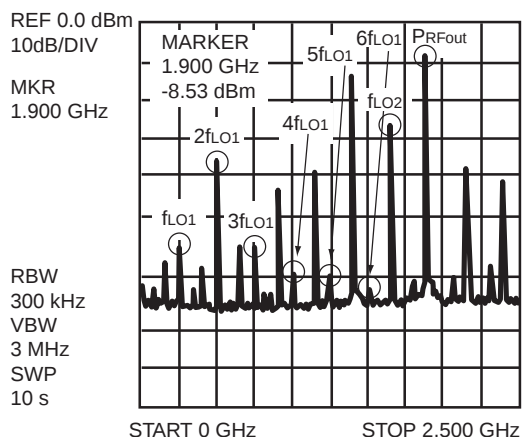


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

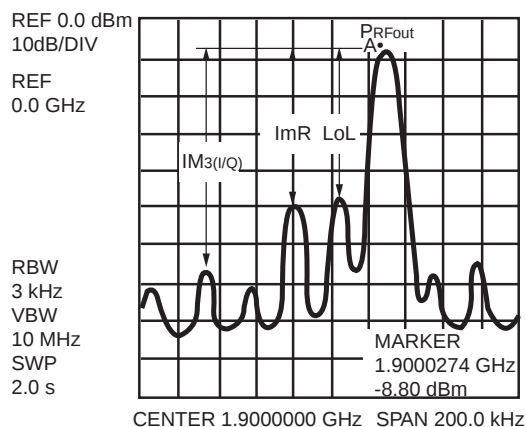


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

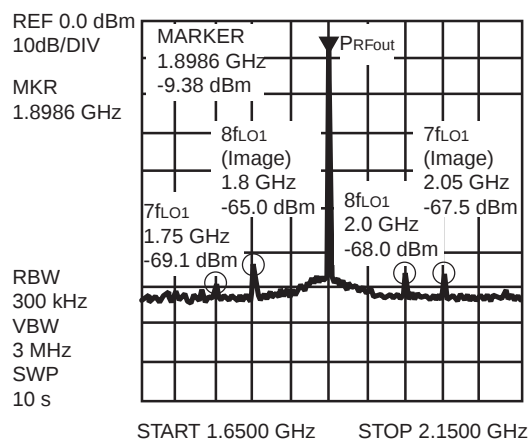
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



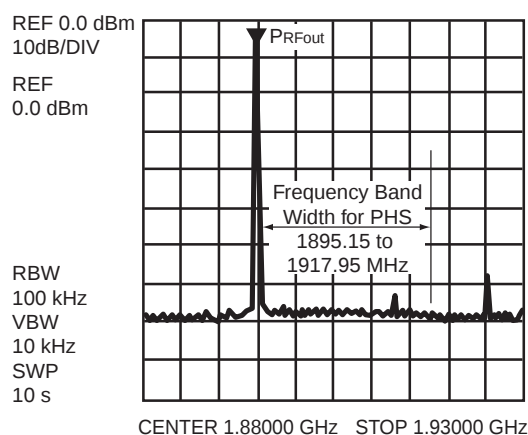
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



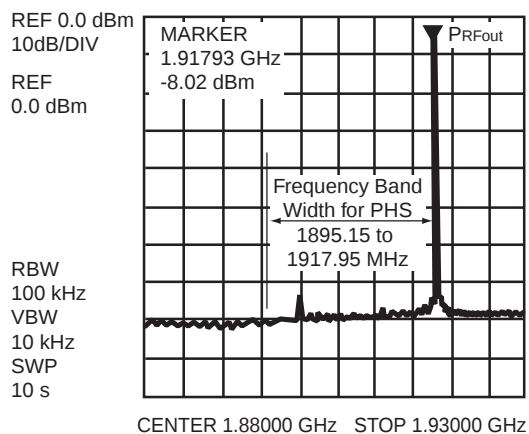
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND) (1)



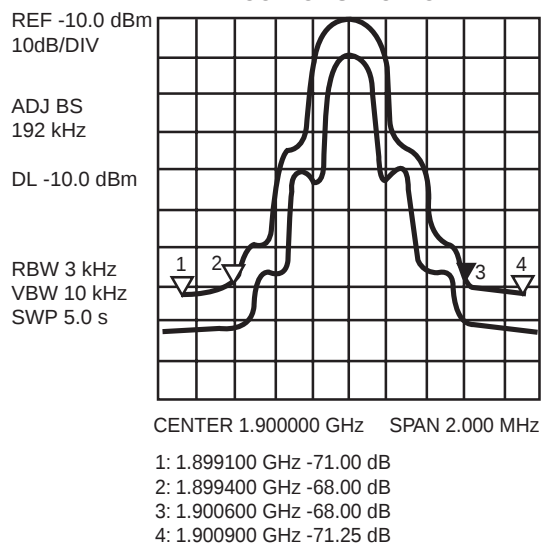
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND) (2) (f_{LO1} = 233.15 MHz, f_{LO2} = 1662 MHz)



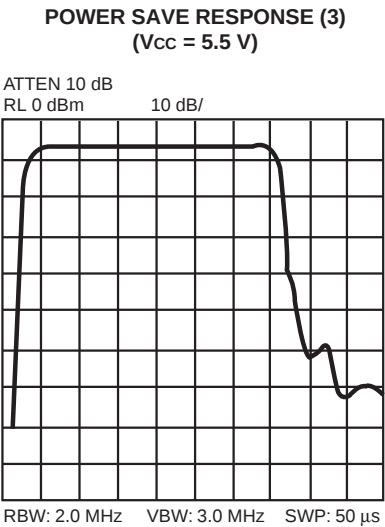
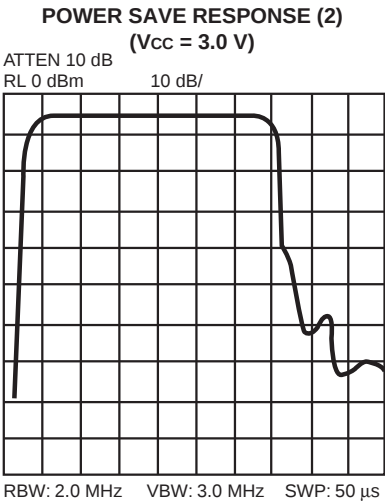
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND) (3) (f_{LO1} = 233.15 MHz, f_{LO2} = 1684.8 MHz)



TYPICAL $\pi/4$ DQPSK MODULATION OUTPUT SPECTRUM



TYPICAL PERFORMANCE CURVES (T_A = 25°C)

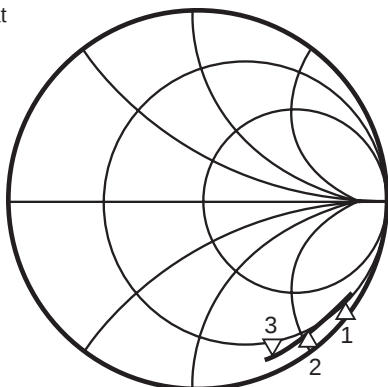


TYPICAL PERFORMANCE CURVES ($T_A = 25^\circ\text{C}$, $V_{CC} = V_{PS} = 3.0\text{ V}$)

RF OUTPUT IMPEDANCE (PIN 19)

Impedance at
Marker 3:
9.145-j84.36

Marker:
1: 900 MHz
2: 1.5 GHz
3: 1.9 GHz

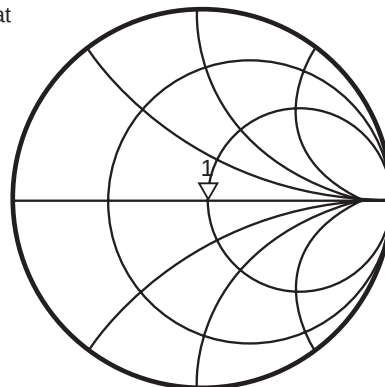


Start: 800 MHz
Stop: 2000 MHz

LO1 INPUT IMPEDANCE (PIN 8)

Impedance at
Marker 1:
50.00+j0.0

Marker:
1: 250 MHz

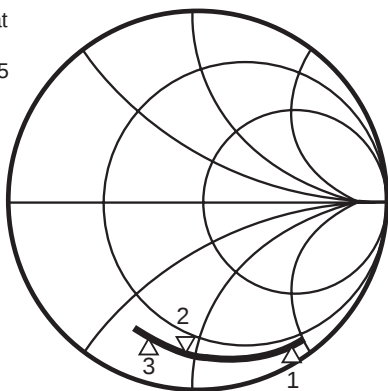


Start: 50 MHz
Stop: 500 MHz

LO2 INPUT IMPEDANCE (PIN 13)

Impedance at
Marker 2:
10.053-j44.05

Marker:
1: 900 MHz
2: 1.65 GHz
3: 1.9 GHz



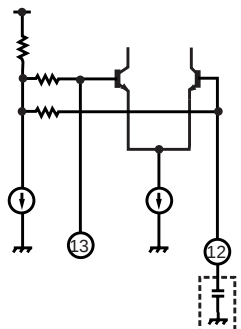
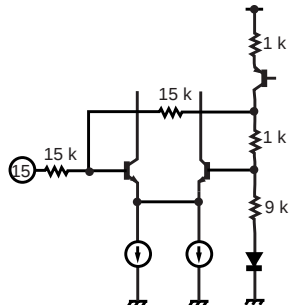
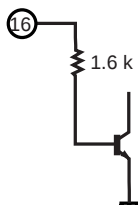
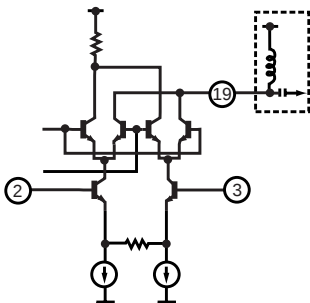
Start: 800 MHz
Stop: 2000 MHz

PIN FUNCTIONS

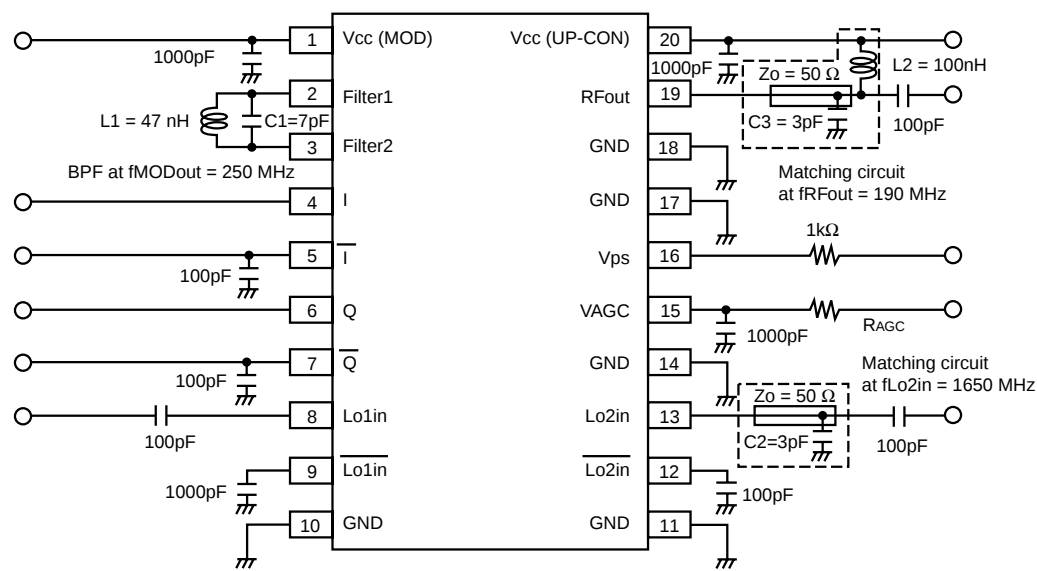
Pin No.	Symbol	Supply Voltage (V)	Pin Voltage (V) @ 3 V	Description	Equivalent Circuit
1	Vcc(MOD.)	2.7 to 5.5	—	Supply Voltage pin for the modulator. An internal regulator helps keep the device stable against temperature or Vcc variation. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.	
2	Filter 1	—	1.9	An external BPF installed between these pins can control the LO1 harmonics.	
3	Filter 2	—	1.9		
4	I	Vcc/2 NOTE	—	Input for I signal. This input impedance is 200 kΩ. When used as a single-ended input, the maximum amplitude should be 500 mV _{P-P} . When used as a differential input, the maximum amplitude should be 250 mV _{P-P} .	
5	$\bar{I}$	Vcc/2 NOTE	—	Input for I signal. This input impedance is 200 kΩ. When used as a single-ended input, a Vcc/2 biased DC signal should be input. When used as a differential input, the maximum amplitude is 250 mV _{P-P} .	
6	Q	Vcc/2 NOTE	—	Input for Q signal. This input impedance is 200 kΩ. When used as a single-ended input, the maximum amplitude should be 500 mV _{P-P} . When used as a differential input, the maximum amplitude should be 250 mV _{P-P} .	
7	$\bar{Q}$	Vcc/2 NOTE	—	Input for Q signal. This input impedance is 200 kΩ. When used as a single-ended input, a Vcc/2 biased DC signal should be input. When used as a differential input, the maximum amplitude is 250 mV _{P-P} .	
8	LO1IN	—	0	LO input for the phase shifter. This input impedance is internally matched to 50 Ω.	
9	$\overline{LO IN}$	—	2.4	Bypass of the LO1 input. This pin should be externally grounded through a capacitor.	
10	GND	—	0	Ground pins for modulator block. These pins should be connected to system ground with minimum inductance. Track length should be kept as short as possible.	
11	(MOD.)	—	0		

Note: Vcc/2 DC bias must be supplied to I, $\bar{I}$, Q, $\bar{Q}$.

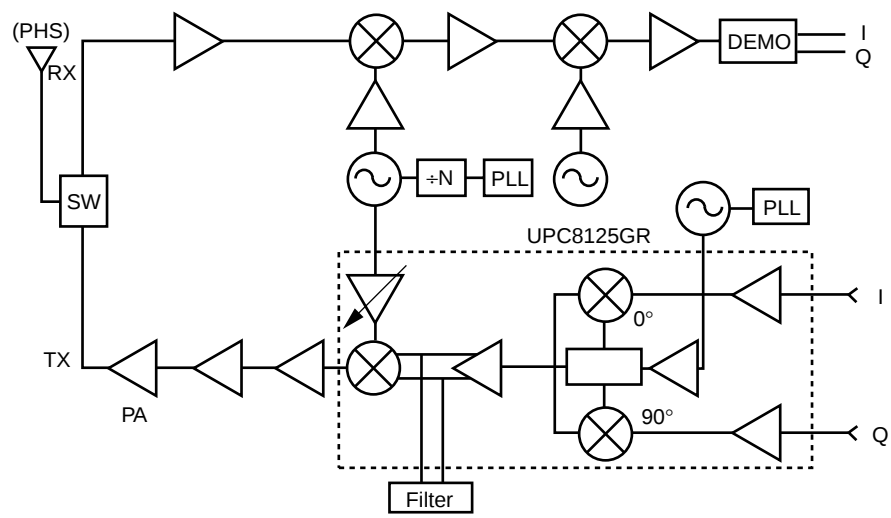
PIN FUNCTIONS

Pin No.	Symbol	Supply Voltage (V)	Pin Voltage (V) @ 3 V	Description	Equivalent Circuit						
12	LO2IN	—	1.9	Bypass of the LO2 input. This pin should be externally grounded through a capacitor.							
13	LO2IN	—	1.9	LO input for the up-converter. This pin is high impedance input and should be used with an external matching circuit.							
14 17 18	GND (Up-conv.)	—	0	Ground pins for the upconverter block. These pins should be connected to sytem ground with minimum inductance. Track length should be kept as short as possible.							
15	VAGC	0 to VCC	—	Gain Control pin. VAGC Up = Gain Up. Adjust value of RAGC to set gain slope.							
16	VPS	0 to VCC	—	Power save control pin can control the On/ Sleep state with bias as follows: <table border="1" data-bbox="634 1125 963 1228"><thead><tr><th>VPS (V)</th><th>STATE</th></tr></thead><tbody><tr><td>≥2.0</td><td>ON</td></tr><tr><td>0 to 0.5</td><td>SLEEP</td></tr></tbody></table>	VPS (V)	STATE	≥2.0	ON	0 to 0.5	SLEEP	
VPS (V)	STATE										
≥2.0	ON										
0 to 0.5	SLEEP										
19	RFOUT	VCC	—	RF output from up-converter. This pin is an open collector and requires an external LC matching circuit.							
20	VCC (Up-con.)	2.7 to 5.5	—	Supply voltage pin for the up-converter. An internal regulator helps keep the device stable against temperature or Vcc variation. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.							

APPLICATION CIRCUIT

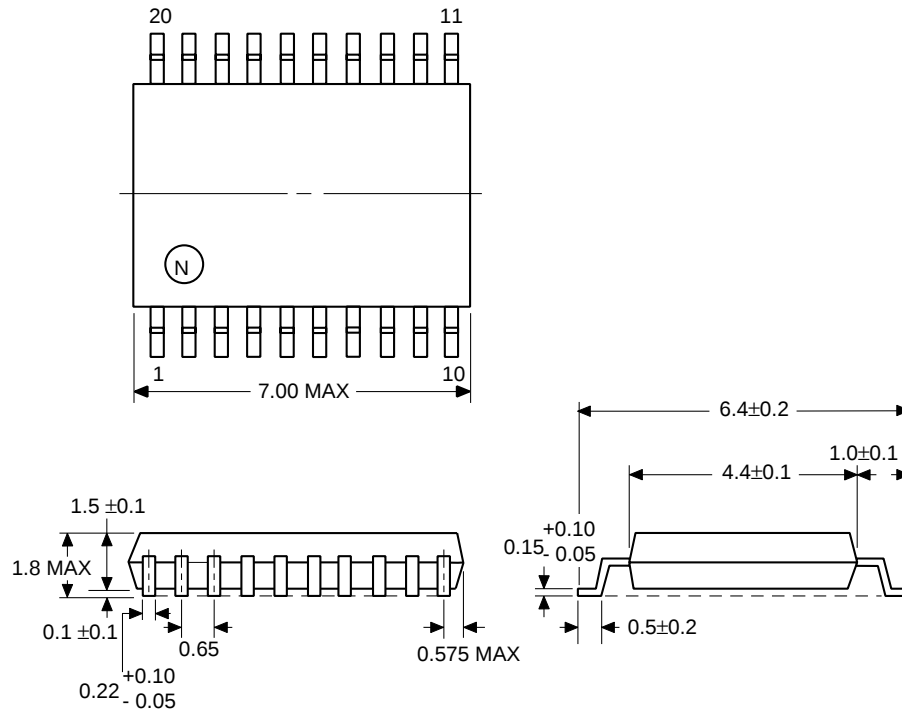


APPLICATION CIRCUIT



PACKAGE DIMENSIONS (Units in mm)

PACKAGE OUTLINE SSOP 20



ORDERING INFORMATION

PART NUMBER	QUANTITY
UPC8125GR-E1	2500/Reel

Notes:

1. Embossed tape, 12 mm wide.

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