National Semiconductor

PRELIMINARY
November 2006

LMH6555
Low Distortion 1.2 GHz Differential Driver

General Description

The LMH6555 is an ultra high speed differential line driver with 50 dB SFDR at 750 MHz. The LMH6555 features a fixed gain of 13.6 dB. An input to the device allows the output common mode voltage to be set independent of the input common mode voltage in order to simplify the interface to high speed differential input ADC's . A unique architecture allows the device to operate as a fully differential driver or as a single-ended to differential converter.

The outstanding linearity and drive capability (100Ω differential load) of this device is a perfect match for driving high speed analog-to-digital converters. When combined with the ADC081000/ ADC08D1500, the LMH6555 forms an excellent 8-bit data acquisition system with analog bandwidths exceeding 1 GHz.

The LMH6555 is offered in a space saving 16-pin LLP package.

Features

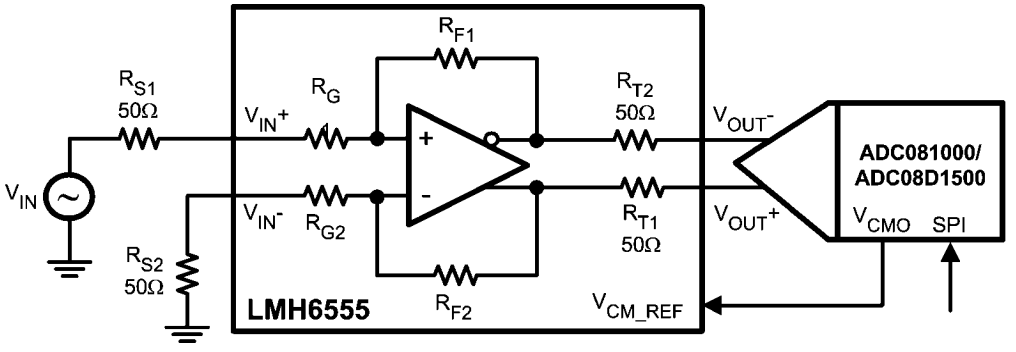
Typical Unless Otherwise Specified:

- –3 dB bandwidth (V_{OUT} = 0.80$_{PP}$) 1.2 GHz
- ±0.5 dB gain flatness (V_{OUT} = 0.80 V_{PP}) 500 MHz
- Slew rate 3000 V/µs
- 2nd/3rd Harmonics (750 MHz) –53/–54 dBc
- Fixed gain 13.6 dB
- Supply current 120 mA
- Single supply operation 3.3V ±10%
- Adjustable common-mode output voltage

Applications

- Differential ADC driver
- National Semiconductor ADC081000/ ADC08D1500 driver
- Single ended to differential converter
- Differential driver
- Intermediate frequency (IF) amplifier
- Communication receivers
- Oscilloscope front end

Block Diagram



Single Ended to Differential Conversion

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 5)	
Human Body Model	2000V
Machine Model	200V
V_S	TBD
Output Short Circuit Duration (one pin to ground)	Infinite
Common Mode Input Voltage	−1V to TBD
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings (Note 1)

Temperature Range (Note 4)	−40°C to +85°C
Supply Voltage Range	+3.3V ±10%
Package Thermal Resistance (θ_{JA})(Note 4)	
16-Pin LLP	65°C/W

3.3V Electrical Characteristics (Note 2)

Unless otherwise specified, all limits are guaranteed for T_A= 25°C, V_{CM_REF} = 1.2V, both inputs tied to 0.3V through 50Ω (R_{S1} & R_{S2}) each (Note 11), V_S = 3.3V, R_L = 100Ω differential, V_{OUT} = 0.8 V_{PP}; See Notes section for definition of terms used throughout the datasheet. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Differential AC Performance						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		1200		MHz
LSBW		V_{OUT} = 0.8 V_{PP}		1200		
GF_0.5	±0.5 dB Gain Flatness	V_{OUT} = 0.8 V_{PP}		500		MHz
Ph_Delta	Phase Delta	Output Differential Phase Difference, f = 400 MHz		TBD		deg
TRS/TRL	Rise/ Fall Time	V_{OUT} = 0.4 V_{PP}		320		pS
OS	Overshoot	V_{OUT} = 0.4 V_{PP}		14		%
SR	Slew Rate	0.8V Step, 10% to 90%,(Note 6)		3000		V/µs
t_s	Settling Time	0.8V Step, V_{OUT} within ±0.1%		TBD		ns
A_{V_DIFF}	Insertion Gain ($\lvert S_{21} \rvert$)	$DC, \frac{\Delta V_{OUT}}{\Delta V_{IN}}$ ΔV_{IN} = 50 mV	TBD **TBD**	13.6	TBD **TBD**	dB
A_{V_VAR}	Insertion Gain Variation	V_{CM_REF} Input Varied from 0.95V to 1.45V, V_{OUT} = 0.8 V_{PP}		±TBD	±TBD	dB
Distortion And Noise Response						
HD2_L	2nd Harmonic Distortion	250 MHz (Note 12)		−60		dBc
HD2_M		500 MHz (Note 12)		−62		
HD2_H		750 MHz (Note 12)		−53		
HD3_L	3rd Harmonic Distortion	250 MHz (Note 12)		−67		dBc
HD3_M		500 MHz (Note 12)		−61		
HD3_H		750 MHz (Note 12)		−54		
OIP3_L	Output 3rd Order Intercept	70 MHz (Note 12)		TBD		dBm
OIP3_H		250 MHz (Note 12)		TBD		
OIM3	Third Order Intermodulation Distortion	f_1 = 70 MHz, f_2 = 70 MHz + 10 kHz, P_{IN} = TBD (Note 12)		TBD		dBc
e_{no}	Output Referred Voltage Noise	>1 MHz		24		$nV/\sqrt{Hz}$
NF	Noise Figure	Relative to Differential Inputs		TBD		dB
Input Characteristics						
R_{IN}	Input Resistance	Single Ended Input Drive	TBD	50	TBD	Ω
R_{IN_DIFF}	Differential Input Resistance	Differential Input Drive	TBD	80	TBD	Ω
C_{IN}	Input Capacitance	Each Input to GND		0.3		pF

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Output Characteristics						
CMVR	Input Common Mode Voltage Range	$A_{V\_DIFF} - A_{V\_CM} \geq 30$ dB	0		TBD	V
V_{OOS}	Output Offset Voltage	Differential Mode		TBD	±100 **TBD**	mV
TCV_{OOS}	Output Offset Voltage Average Drift	(Note 9)		±200	TBD	µV/°C
R_O	Output Resistance	R_{T1} and R_{T2}	TBD	50	TBD	Ω
V_{OUT}	Differential Output Voltage Swing	$\Delta A_{V\_DIFF} \leq 1$ dB	TBD **TBD**	800		mV
V_{O_CM}	Output Common Mode Voltage Range	V_{CM_REF} Input Varied, V_{OUT} = 0.80 V_{PP}	0.95 **TBD**		1.45 **TBD**	V
BAL_Error_DC	Output Balance Error	DC, $\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$		TBD	TBD	dB
BAL_Error_AC		f = 500 MHz, $\frac{v_{O\_CM}}{v_{OUT}}$		TBD		
A_{V_CM}	Common Mode Gain	DC, $\Delta V_{O\_CM}/\Delta V_{I\_CM}$	TBD **TBD**	TBD	TBD **TBD**	dB
V_{CM_REF} Characteristics						
V_{OS_CM}	Output CM Offset Voltage	$V_{OS\_CM} = V_{O\_CM} - V_{CM\_REF}$		TBD	±50	mV
I_{B_CM}	V_{CM_REF} Bias Current	$0.95V \leq V_{CM\_REF} \leq 1.45V$ (Note 10)		−100	TBD	µA
R_{IN_CM}	V_{CM_REF} Input Resistance			TBD		kΩ
Gain_V_{CM_REF}	V_{CM_REF} Input Gain to Output	$\Delta V_{O\_CM}/\Delta V_{CM\_REF}$	TBD	0.99	TBD	V/V
Power Supply						
I_S	Supply Current	R_{S1} & R_{S2} Open (Note 3)	TBD **TBD**	120	TBD **TBD**	mA
PSRR	Differential Power Supply Rejection Ratio	DC, $\Delta V_S = \pm 0.3V$, $\Delta V_{OUT}/\Delta V_S$	TBD **TBD**	76		dB
PSRR_CM	Common Mode PSRR	DC, $\Delta V_S = \pm 0.3V$, $\Delta V_{O\_CM}/\Delta V_S$	TBD **TBD**	TBD		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 3: Total supply current is affected by the input voltages connected through R_{S1} and R_{S2}. Supply current tested with input removed.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow.

Note 5: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 6: Slew Rate is the average of the rising and falling edges.

Note 7: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 8: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 9: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Note 10: Positive current is current flowing into the device.

Note 11: Quiescent device common mode input voltage is 0.3V.

Note 12: Distortion data taken under single ended input condition.

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
16-Pin LLP	LMH6555SQ	L6555SQ	1k Units Tape and Reel	SQA16A
	LMH6555SQX		4.5k Units Tape and Reel	

Definition of Terms and Specifications (Alphabetical order)

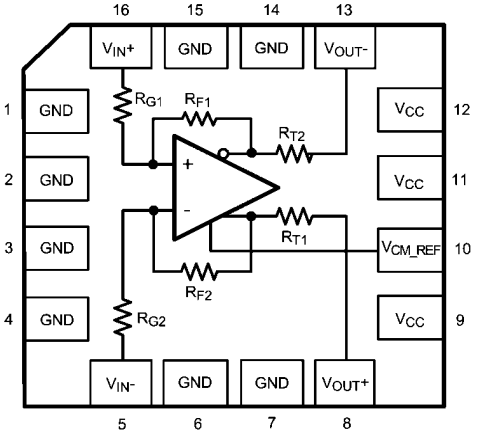
Unless otherwise specified, V_{CM_REF} = 1.2V

1.	1. A_{V_CM} (dB)	Change in the output common mode voltage (ΔV_{O_CM}) with respect to the change in input common mode voltage (ΔV_{I_CM})
2.	A_{V_DIFF} (dB)	Insertion gain from a single ended 50Ω (or 100Ω differential) source to the differential output (ΔV_{OUT})
3.	ΔA_{V_DIFF} (dB)	Variation in insertion gain (A_{V_DIFF}) with input signal change (ΔV_{IN})
4.	A_{V_VAR} (dB)	Variation of insertion gain (A_{V_DIFF}) with V_{CM_REF} input change (ΔV_{CM_REF}). Calculated as the change in A_{V_DIFF} (dB) at various V_{CM_REF}
5.	CMVR (V)	Range of input common mode voltage (V_{I_CM}) where the insertion gain (A_{V_DIFF}) is 30 dB larger than common mode gain (A_{V_CM}) and hence the amplifier's output is dominated by its differential output
6.	Gain_VCM_REF (V/V)	Variation in output common mode voltage (ΔV_{O_CM}) with respect to change in V_{CM_REF} input (ΔV_{CM_REF}) with maximum differential output
7.	Pin (dBm referenced to 50Ω)	Input power associated with each of the tones for OIM3 testing
8.	PSRR (dB)	Differential output change (ΔV_{OUT}) with respect to the power supply voltage change (ΔV_S) with nominal differential output
9.	PSRR_CM (dB)	Output common mode voltage change (ΔV_{O_CM}) with respect to the change in the power supply voltage (ΔV_S)
10.	R_{IN} (Ω)	Single ended input impedance to ground
11.	R_{IN_DIFF} (Ω)	Differential input impedance
12.	R_L (Ω)	Differential output load
13.	R_O (Ω)	Equivalent to R_{T1} & R_{T2}
14.	R_{S1}, R_{S2} (Ω)	Source impedance to V_{IN+} and V_{IN-} respectively
15.	R_{T1}, R_{T2} (Ω)	Output impedance looking into each output
16.	V_{CM_REF} (V)	Device input pin voltage which controls output common mode
17.	ΔV_{CM_REF} (V)	Change in the V_{CM_REF} input voltage
18.	V_{I_CM} (V)	DC average of the inputs (V_{IN+}, V_{IN-})
19.	ΔV_{I_CM} (V)	Variation in input common mode voltage (V_{I_CM})
20.	V_{IN+}, V_{IN-} (V)	Device input pin voltages
21.	ΔV_{IN} (V)	Terminated (50Ω for single ended and 100Ω for differential) generator voltage
22.	V_{O_CM} (V)	Output common mode voltage (DC average of V_{OUT+} and V_{OUT-})
23.	ΔV_{O_CM} (V)	Variation in output common mode voltage (V_{O_CM})
24.	$\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$ (dB)	Balance Error. Measure of the output swing balance of V_{OUT+} and V_{OUT-}, as reflected on the output common mode voltage (V_{O_CM}), relative to the differential output swing (V_{OUT}). Calculated as output common mode voltage change (ΔV_{O_CM}) divided into the output differential voltage change (ΔV_{OUT})
25.	$\frac{V_{O\_CM}}{V_{OUT}}$ (dB)	AC version of the DC balance error $\left(\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}\right)$ test
26.	V_{OOS} (V)	DC Offset Voltage. Differential output voltage measured with both inputs grounded through 50Ω

27.	V_{OS_CM} (V)	Difference between the output common mode voltage (V_{O_CM}) and the voltage on the V_{CM_REF} input, for the allowable V_{CM_REF} range
28.	V_{OUT} (V)	Differential Output Voltage (V_{OUT+} - V_{OUT-}) (Corrected for DC offset (V_{OOS}))
29.	ΔV_{OUT} (V)	Change in the differential output voltage (Corrected for DC offset (V_{OOS}))
30.	V_{OUT+}, V_{OUT-} (V)	Device output pin voltages
31.	V_S (V)	Supply Voltage (V^+ - V^-)
32.	ΔV_S (V)	Change in V_{CC} supply voltage

Connection Diagram

16-Pin LLP



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Application Information

The LMH6555 consists of three individual amplifiers: The V_{OUT+} driver, V_{OUT-} driver, and the common mode amplifier. Being a differential amplifier, the LMH6555 will not respond to the input common mode input (as long as it is within its input common mode range) and instead the output common mode is forced by the built-in common mode amplifier with V_{CM_REF} as its input. As shown in *Figure 1* below, the VCMO of most differential high speed ADC's will be tied to the V_{CM_REF} input of the LMH6555 for direct output common mode control. In some cases, the output drive capability of the ADC VCMO output may need an external buffer (not shown) to increase its current capability in order to drive the V_{CM_REF} pin. The LMH6555 Electrical Characteristics table shows the gain (A_{V_CM}) and the offset (V_{OS_CM}) from the V_{CM_REF} to the device output common mode.

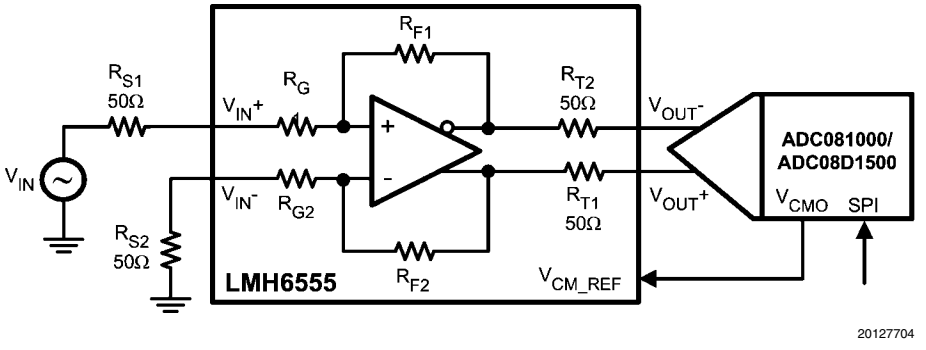

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FIGURE 1. Single Ended to Differential Conversion

The single ended AC input and output impedance of the LMH6555 I/O pins are close to 50Ω and are also specified in the Electrical Characteristics table (R_{IN} and R_O). With differential input drive, the differential input impedance (R_{IN_DIFF}) will be close to 80Ω.

The device nominal input common mode voltage is close to 0.3V at V_{IN+} and V_{IN-} with a weak relationship to the V_{CM_REF} voltage. Thus, the input source will experience a DC current which is dependant on its DC voltage. Because of this, the differential output offset voltage is influenced by the matching between R_{S1} and R_{S2} under DC and AC conditions. So, for example, in a single ended input condition, if the signal source is AC coupled to one input, the undriven input needs to also be AC coupled.

In applications where very low output offset is required, adjusting the value of R_{S2} (the input which is not driven) can be an effective method of trimming the output offset voltage of the LMH6555 in a single ended input configuration. The nominal value of R_{S1} and R_{S2} on the other hand will affect the insertion gain. The LMH6555 can also be used with the input signal AC coupled. In this case, the coupling capacitors need to be large enough to not block the frequency content below $(1/2\pi R_{IN}C)$Hz.

The single ended output impedance of the LMH6555 is 50Ω. The LMH6555 Electrical Characteristics shows the device performance with 100Ω differential output load, as would be the case if a device such as the ADC081000 were being driven. As shown in *Figure 2* below, some applications can benefit from using the LMH6555 to interface a Class A type differential output device (U1) to a high speed ADC. In this application, the LMH6555 performs the task of buffering and amplifying the signal to properly drive the 100Ω differential input impedance of the ADC.

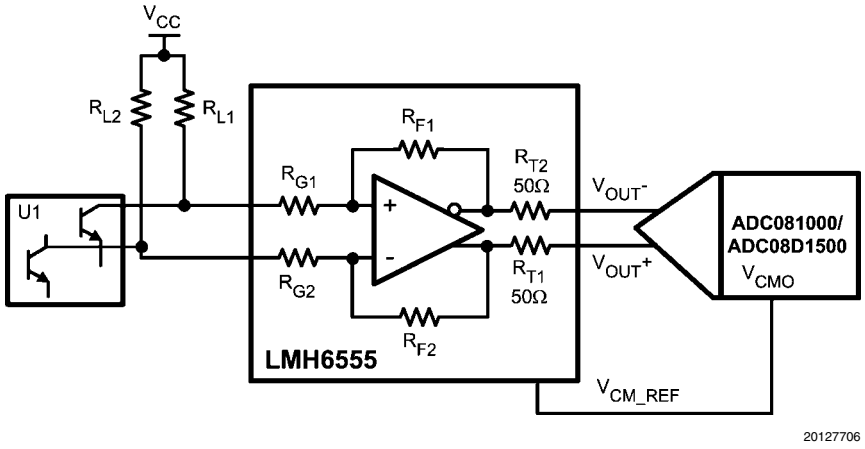


FIGURE 2. Differential Buffering and Amplification

In this application, U1's DC common mode output will be affected by the LMH6555 input common mode voltage through R_G and R_L. The equivalent load to the driver Collector within U1 would be the combination of R_L and R_{IN_DIFF} (≅80Ω). Series isolation resistors (not shown) between U1 outputs and LMH6555 input pins would offer additional isolation at the expense of more signal loss. Alternatively, input AC coupling could have been used to alleviate the common mode concerns.

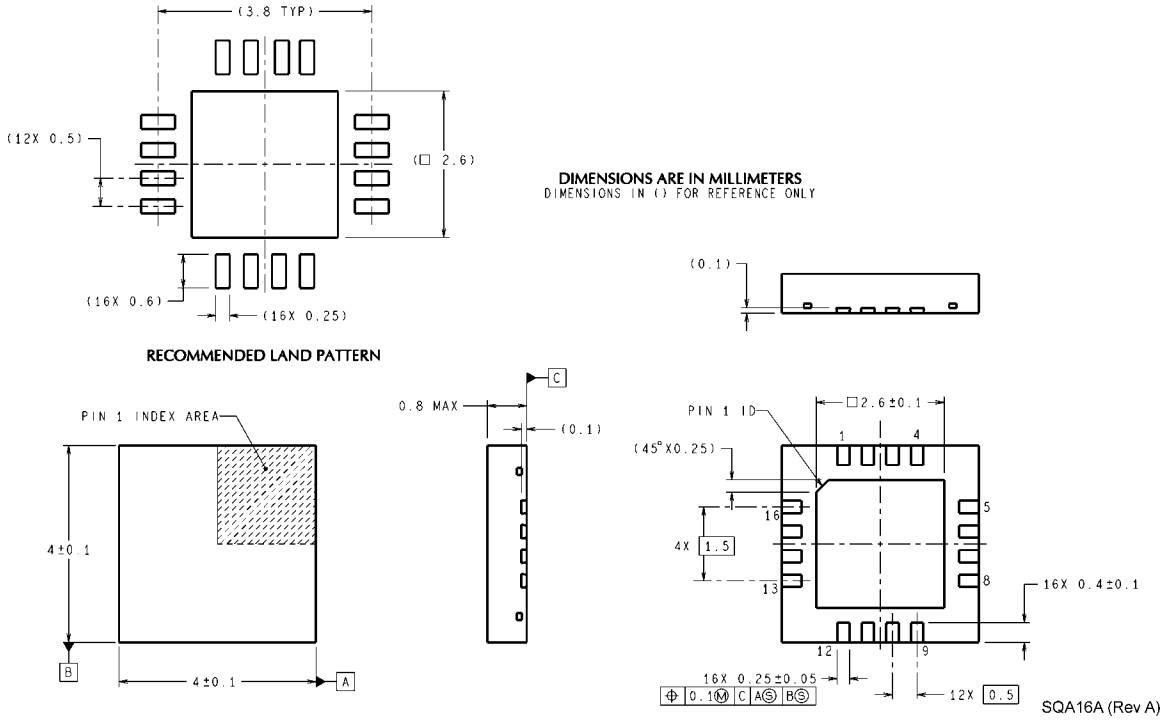
EXPOSED PAD LLP PACKAGE

The LMH6555 is packaged in a thermally enhanced package. The exposed pad (device bottom) is connected to the GND pins. It is recommended, but not necessary, that the exposed pad be connected to the supply ground plane. The thermal dissipation of the device is largely dependent on the connection of this pad. The exposed pad should be attached to as much copper on the circuit board as possible, preferably external copper. However, it is very important to maintain good high speed layout practices when designing a system board.

Here is a link to more information on the National 16 pin LLP package:

http://www.national.com/packaging/folders/sqa16a.html

Physical Dimensions inches (millimeters) unless otherwise noted



16-Pin LLP
NS Package Number SQA16A

Notes

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