

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT CMOS STATIC RAM

DESCRIPTION

The TC55VZM216AJJN/AFTN is a 4,194,304-bit high-speed static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable ($\overline{CE}$) can be used to place the device in a low-power mode, and output enable ($\overline{OE}$) provides fast memory access. Data byte control signals ($\overline{LB}$, $\overline{UB}$) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55VZM216AJJN/AFTN is available in plastic 44-pin SOJ and TSOP with 400mil width for high density surface assembly.

FEATURES

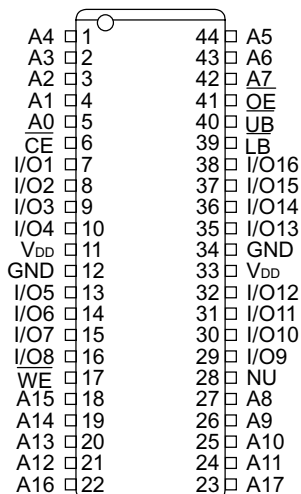
- Fast access time (the following are maximum values)
 - TC55VZM216AJJN/AFTN08:8 ns
 - TC55VZM216AJJN/AFTN10:10 ns
 - TC55VZM216AJJN/AFTN12:12 ns
- Low-power dissipation (I_{DD02}) (the following are maximum values)

Cycle Time	8	10	12	ns
Operation (max)	140	130	120	mA
- Single power supply voltage of 3.3 V $\pm$ 0.3 V
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Output buffer control using $\overline{OE}$
- Data byte control using $\overline{LB}$ (I/O1 to I/O8) and $\overline{UB}$ (I/O9 to I/O16)
- Package:
 - SOJ44-P-400-1.27 (AJJN) (Weight: 1.64 g typ)
 - TSOP II44-P-400-0.80 (AFTN) (Weight: 0.45 g typ)

Standby:4 mA (both devices)

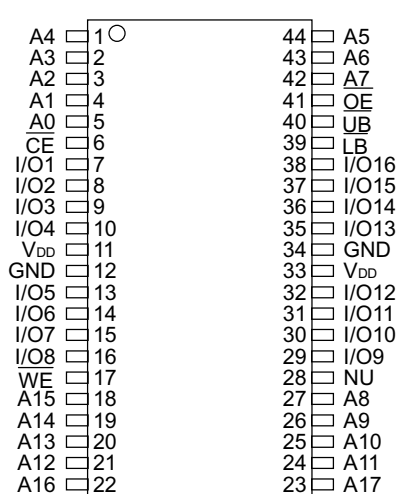
PIN ASSIGNMENT (TOP VIEW)

44 PIN SOJ



(TC55VZM216AJJN)

44 PIN TSOP

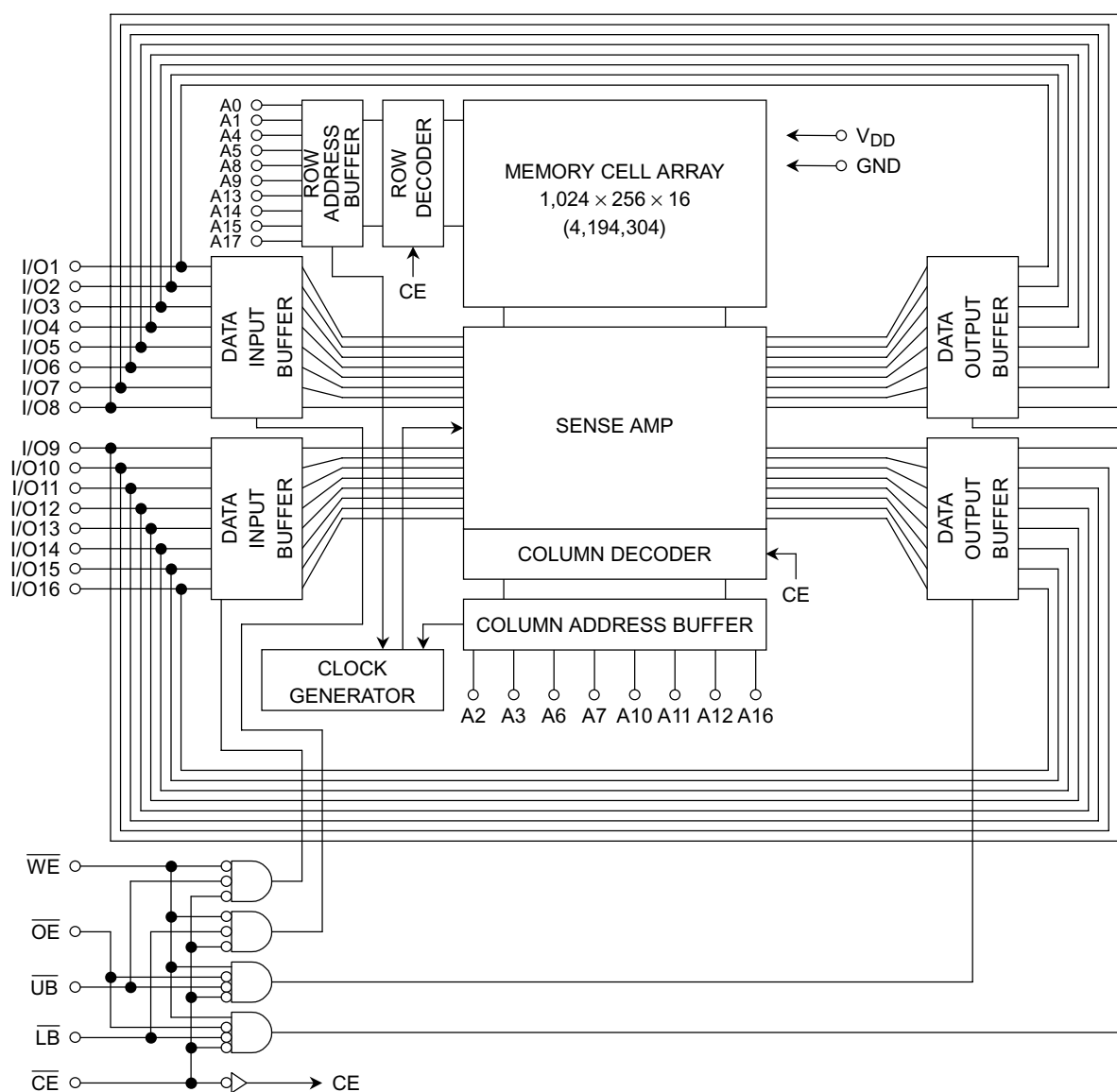


(TC55VZM216AFTN)

PIN NAMES

A0 to A17	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power (+3.3 V)
GND	Ground
NU	Not Usable (Input)

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	−0.5 to 4.6	V
V _{IN}	Input Terminal Voltage	−0.5* to 4.6	V
V _{I/O}	Input/Output Terminal Voltage	−0.5* to V _{DD} + 0.5**	V
P _D	Power Dissipation	1.4	W
T _{solder}	Soldering Temperature (10s)	260	°C
T _{stg}	Storage Temperature	−65 to 150	°C
T _{opr}	Operating Temperature	−10 to 85	°C

*: -1.5 V with a pulse width of 20% of t_{RC} min (4 ns max)

** $V_{DD} + 1.5\text{ V}$ with a pulse width of 20% of $t_{RC}\text{ min}$ (4 ns max)

DC RECOMMENDED OPERATING CONDITIONS ($T_a = 0^\circ \text{ to } 70^\circ \text{C}$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	—	$V_{DD} + 0.3^{**}$	V
V_{IL}	Input Low Voltage	-0.3*	—	0.8	V

*: -1.0 V with a pulse width of 20% of t_{RC} min (4 ns max)**: $V_{DD} + 1.0$ V with a pulse width of 20% of t_{RC} min (4 ns max)**DC CHARACTERISTICS** ($T_a = 0^\circ \text{ to } 70^\circ \text{C}$, $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current (Except NU pin)	V _{IN} = 0 to V _{DD}		−1	—	1	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, V _{OUT} = 0 to V _{DD}		−1	—	1	μA
I _I (NU)	Input Leakage Current (NU pin)	V _{IN} = 0 V		−1	—	1	μA
V _{OH}	Output High Voltage	I _{OH} = −2 mA		2.4	—	—	V
		I _{OH} = −100 μA		V _{DD} − 0.2	—	—	
V _{OL}	Output Low Voltage	I _{OL} = 2 mA		—	—	0.4	
		I _{OL} = 100 μA		—	—	0.2	
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$, I _{OUT} = 0 mA, $\overline{OE} = V_{IH}$, Other Input = V _{IH} /V _{IL}	t _{cycle} = 8 ns	—	—	170	mA
			t _{cycle} = 10 ns	—	—	160	
			t _{cycle} = 12 ns	—	—	150	
I _{DDO2}		$\overline{CE} = 0.2$ V, I _{OUT} = 0 mA, $\overline{OE} = V_{DD} - 0.2$ V, Other Input = V _{DD} − 0.2 V/0.2 V	t _{cycle} = 8 ns	—	—	140	
			t _{cycle} = 10 ns	—	—	130	
			t _{cycle} = 12 ns	—	—	120	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Input = V _{IH} or V _{IL}		—	—	55	mA
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2$ V, Other Input = V _{DD} − 0.2 V or 0.2 V		—	—	4	

CAPACITANCE ($T_a = 25^\circ \text{C}$, $f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Outputs Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDs}

* : Don't care

Note: The NU pin must be left unconnected or tied to GND.
You must not apply a voltage of more than 0.8 V to the NU.

AC CHARACTERISTICS (Ta = 0° to 70°C (See Note 1), VDD = 3.3 V ± 0.3 V)

READ CYCLE

SYMBOL	PARAMETER	TC55VZM216AJJN/AFTN						UNIT
		08		10		12		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t _{ACC}	Address Access Time	—	8	—	10	—	12	
t _{CO}	Chip Enable Access Time	—	8	—	10	—	12	
t _{OE}	Output Enable Access Time	—	4	—	5	—	6	
t _{BA}	Upper Byte, Lower Byte Access Time	—	4	—	5	—	6	
t _{OH}	Output Data Hold Time from Address Change	3	—	3	—	3	—	
t _{COE}	Output Enable Time from Chip Enable	3	—	3	—	3	—	
t _{OEE}	Output Enable Time from Output Enable	0	—	0	—	0	—	
t _{BE}	Output Enable Time from Upper Byte, Lower Byte	0	—	0	—	0	—	
t _{COD}	Output Disable Time from Chip Enable	—	4	—	5	—	6	
t _{ODO}	Output Disable Time from Output Enable	—	4	—	5	—	6	
t _{BD}	Output Disable Time from Upper Byte, Lower Byte	—	4	—	5	—	6	

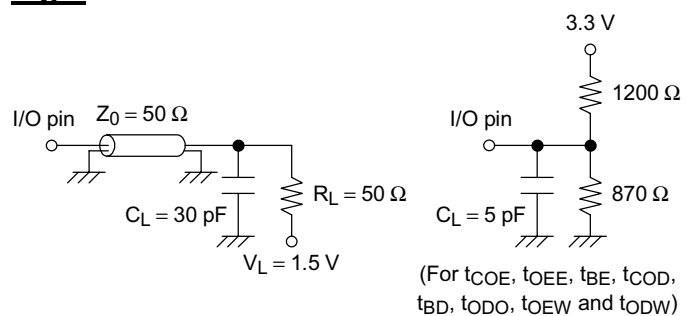
WRITE CYCLE

SYMBOL	PARAMETER	TC55VZM216AJJN/AFTN						UNIT
		08		10		12		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t _{WP}	Write Pulse Width	6	—	7	—	8	—	
t _{CW}	Chip Enable to End of Write	6	—	7	—	8	—	
t _{BW}	Upper Byte, Lower Byte Enable to End of Write	6	—	7	—	8	—	
t _{AW}	Address Valid to End of Write	6	—	7	—	8	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{DS}	Data Setup Time	4	—	5	—	6	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	
t _{OE_W}	Output Enable Time from Write Enable	3	—	3	—	3	—	
t _{OD_W}	Output Disable Time from Write Enable	—	4	—	5	—	6	

AC TEST CONDITIONS

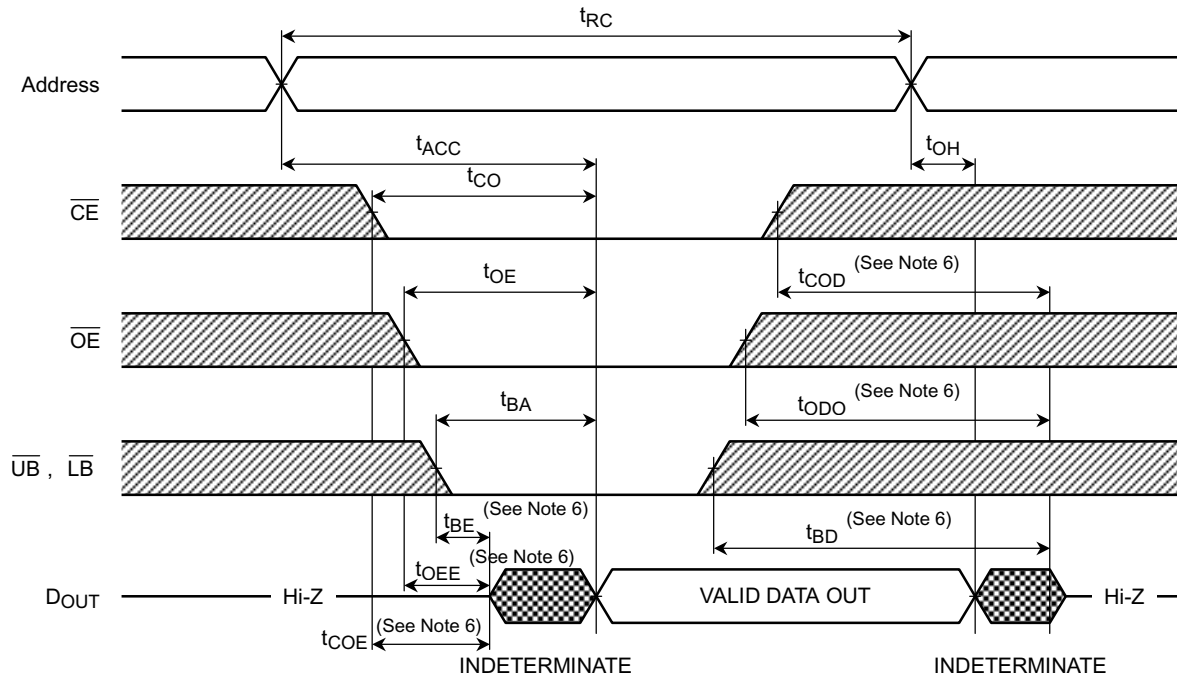
PARAMETER	TEST CONDITION
Input Pulse Level	3.0 V/ 0.0 V
Input Pulse Rise and Fall Time	2 ns
Input Timing Measurement Reference Level	1.5 V
Output Timing Measurement Reference Level	1.5 V
Output Load	Fig.1

Fig.1

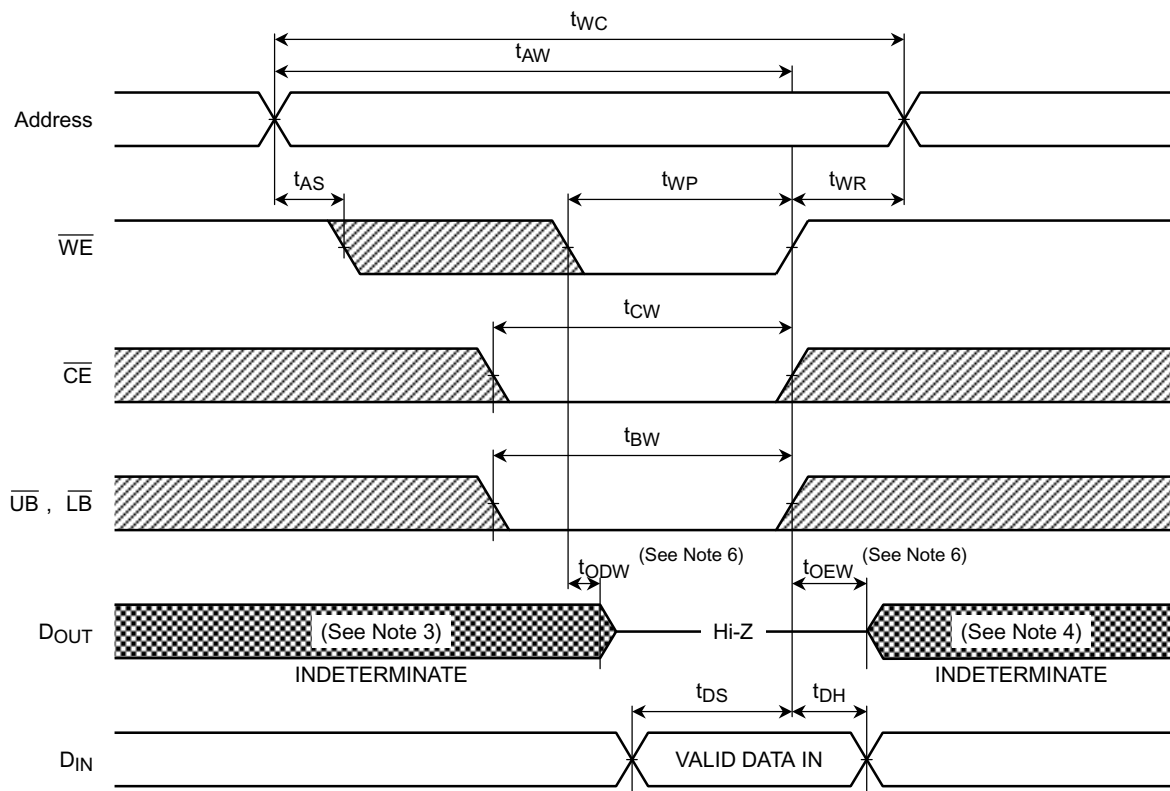


TIMING DIAGRAMS

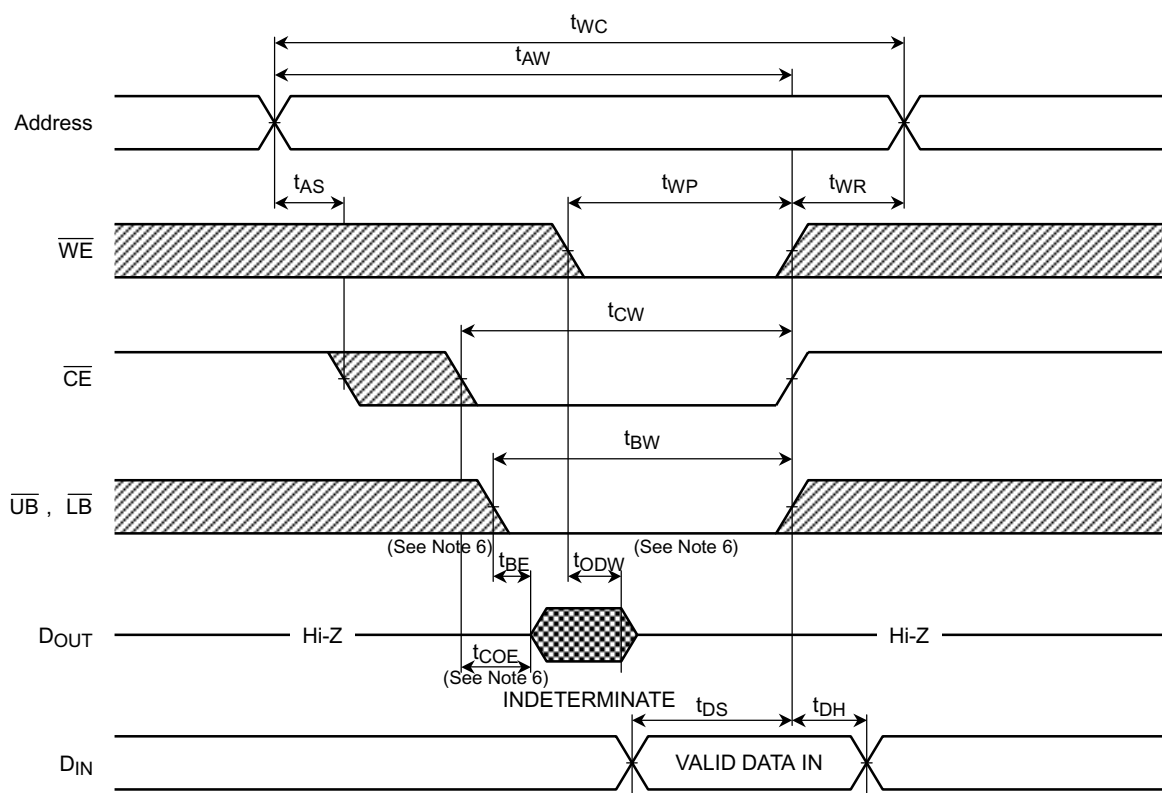
READ CYCLE (See Note 2)



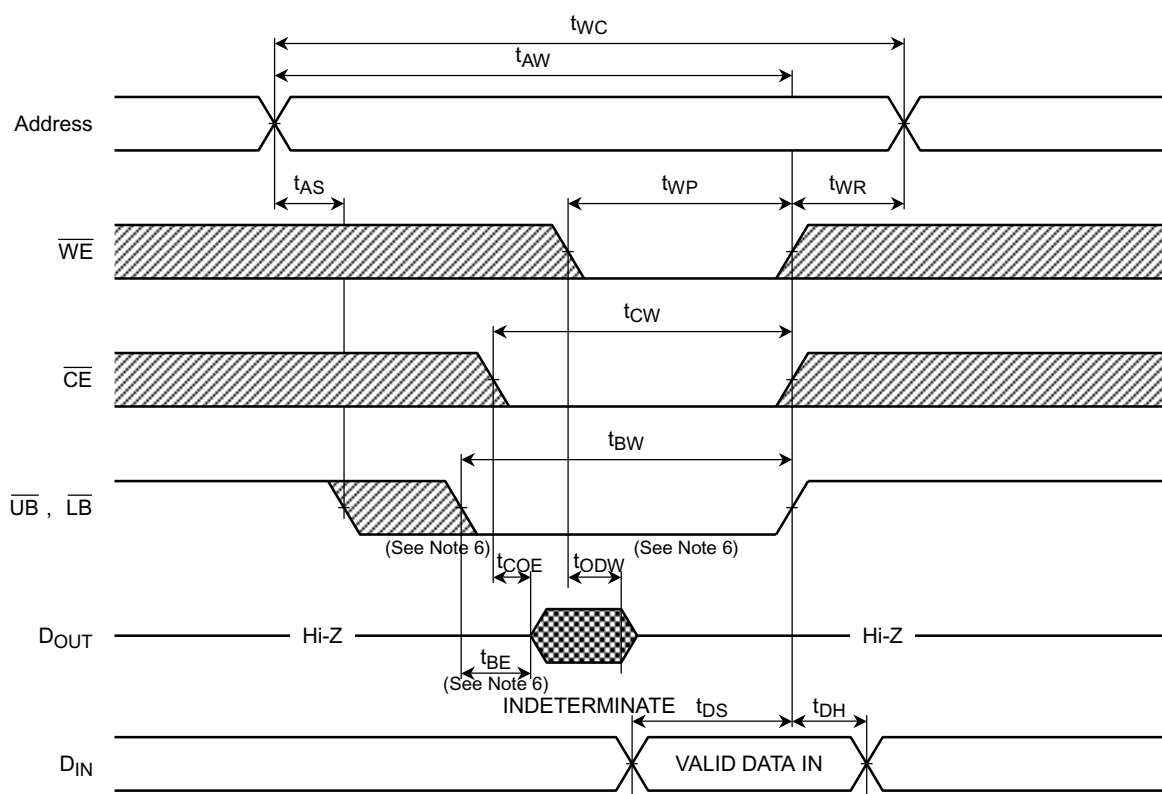
WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (See Note 5)



WRITE CYCLE 2 ($\overline{\text{CE}}$ CONTROLLED) (See Note 5)



WRITE CYCLE 2 ($\overline{\text{UB}}$, $\overline{\text{LB}}$ CONTROLLED) (See Note 5)

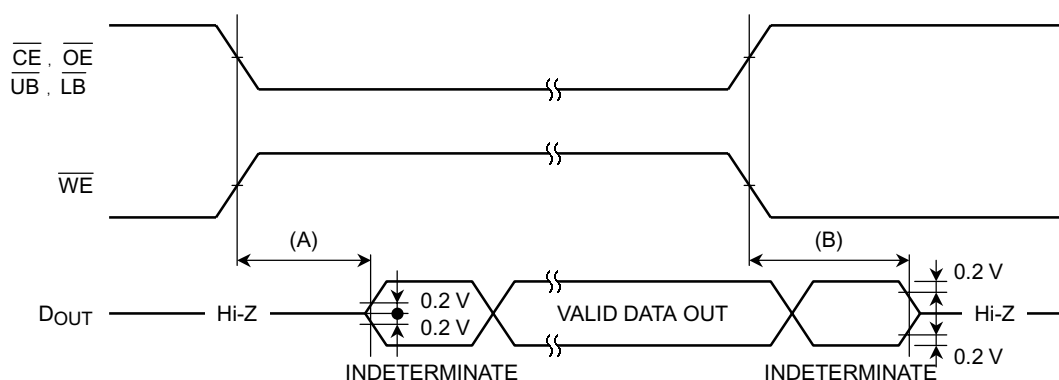


Note:

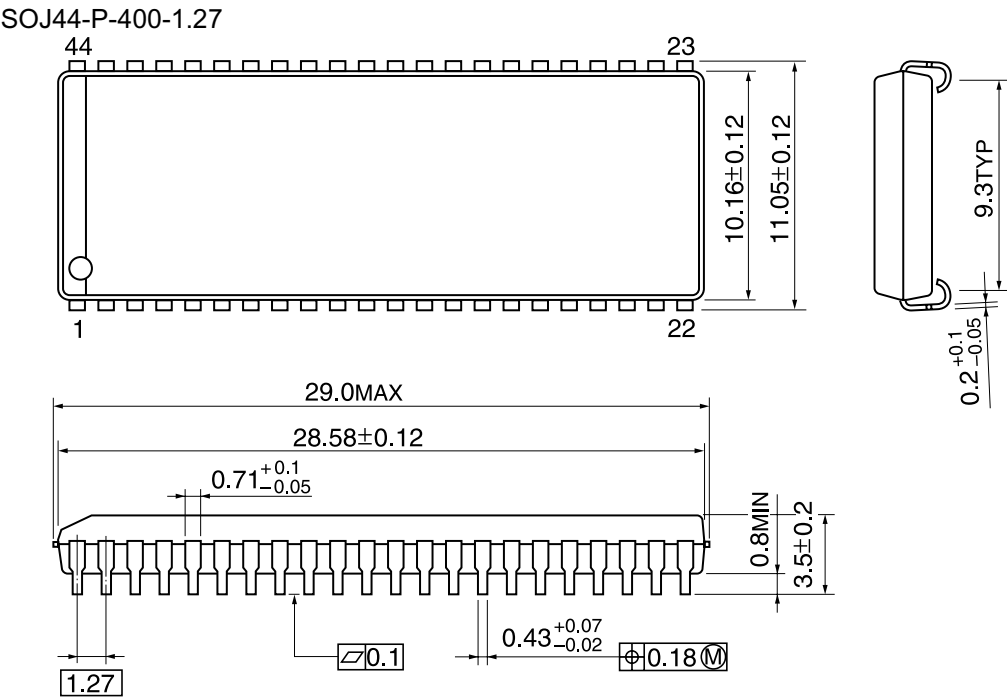
- (1) Operating temperature (Ta) is guaranteed for transverse air flow exceeding 400 linear feet per minute.
- (2) $\overline{\text{WE}}$ remains HIGH for the Read Cycle.
- (3) If $\overline{\text{CE}}$ goes LOW coincident with or after $\overline{\text{WE}}$ goes LOW, the outputs will remain at high impedance.
- (4) If $\overline{\text{CE}}$ goes HIGH coincident with or before $\overline{\text{WE}}$ goes HIGH, the outputs will remain at high impedance.
- (5) If $\overline{\text{OE}}$ is HIGH during the write cycle, the outputs will remain at high impedance.
- (6) The parameters specified below are measured using the load shown in Fig.1.

(A) tCOE, tOEE, tBE, tOEW Output Enable Time

(B) tCOD, tODO, tBD, tODW..... Output Disable Time



PACKAGE DIMENSIONS

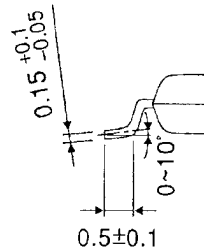
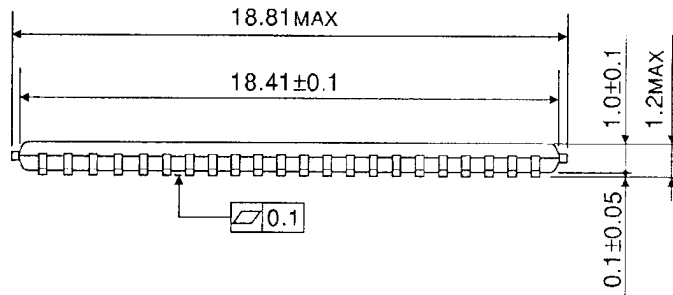
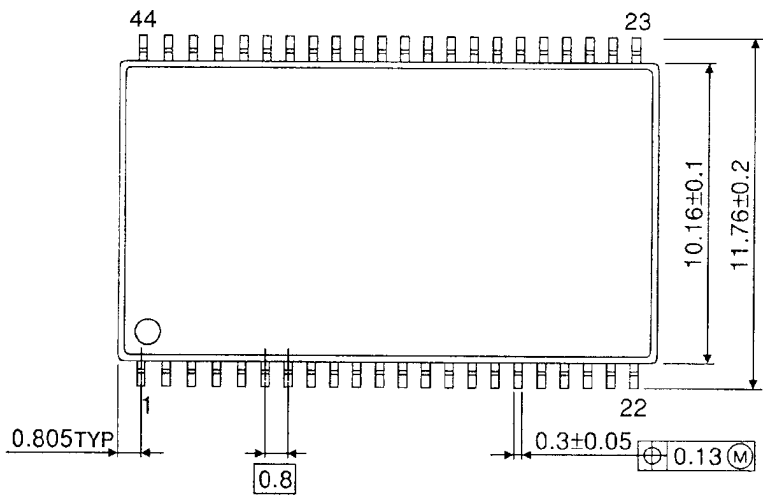


Weight: 1.64 g (typ)

PACKAGE DIMENSIONS

TSOPII 44-P-400-0.80

Unit : mm



Weight: 0.45 g (typ)

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