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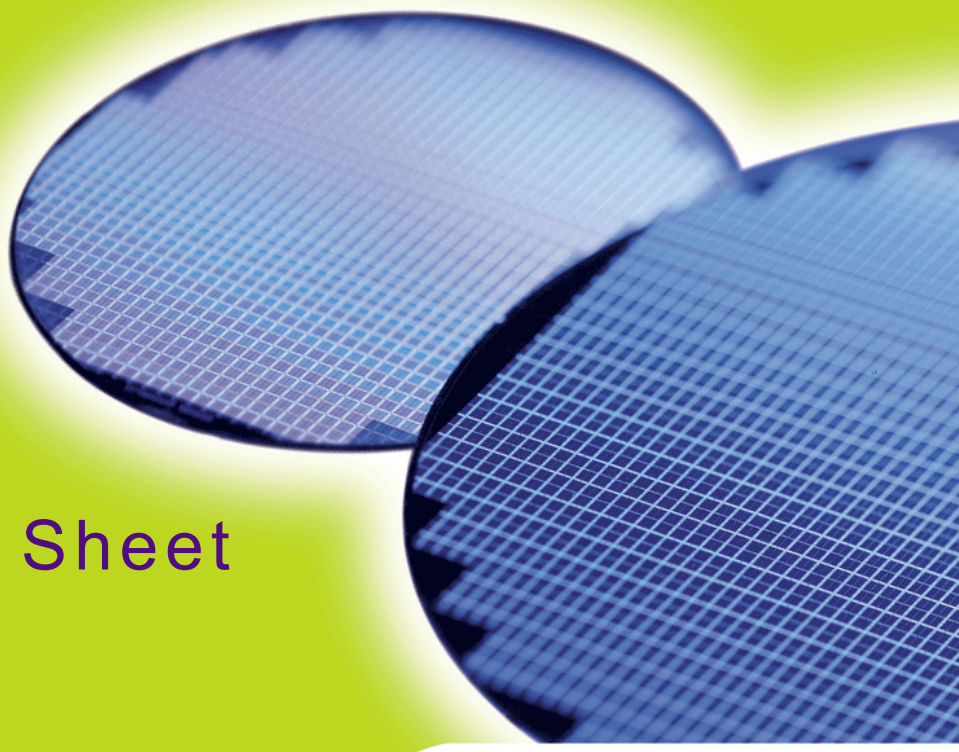
HYB18M256320CF–6/7.5
HYE18M256320CF–6/7.5
HYB18M256160CF–6/7.5
HYE18M256160CF–6/7.5

DRAMs for Mobile Applications

256-Mbit Mobile-RAM



Internet Data Sheet

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HYB18M256320CF–6/7.5, HYE18M256320CF–6/7.5, HYB18M256160CF–6/7.5 , HYE18M256160CF–6/7.5 Revision History: Rev.1.44, 2007-07	
Page	**Subjects (major changes since last revision)**
All	Adapted Internet Edition
55, 56	Editorial changes
Previous Revision:Rev.1.43, 2007-04	
24	Updated Figure 44 for 60-ball PG-VFBGA-60-4 (x16)
25	Updated Figure 45 for 90-ball PG-VFBGA-90-3 (x32)
Previous Revision:Rev.1.42, 2007-03	
All	New Qimonda Template.
All	see Change List Rev. 1.41
Previous Revision:Rev.1.40, 2006-06	

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1 Overview

1.1 Features

- Organization:
  - 4 banks × 4 Mbit × 16, 1 KB page size
  - 4 banks × 2 Mbit × 32, 2 KB page size
- Double-data-rate architecture: two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted / received with data; to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs and center-aligned with data for WRITEs
- Differential clock input (CK / $\overline{CK}$)
- Commands entered on positive CK edge; data and mask data are referenced to both edges of DQS
- Four internal banks for concurrent operation
- Programmable CAS latency: 2 and 3
- Programmable burst length: 2, 4, 8, 16 and full page
- Programmable drive strength: full, 1/2, 1/4 and 1/8
- Auto refresh and self refresh modes
- Refresh cycles:
  - 8192 refresh cycles / 64ms (x16)
  - 4096 refresh cycles / 64ms (x32)
- Auto precharge
- Commercial (-0°C to +70°C) and Extended (-25°C to +85°C) operating temperature ranges
- Package:
  - x16: 60–ball PG-VFBGA-60-4 10.0 × 10.5 × 1.0 mm
  - x32: 90–ball PG-VFBGA-60-3 10.0 × 12.5 × 1.0 mm
- RoHS Compliant Products[1)]

Power Saving Features

- Low supply voltages: V_{DD} = 1.70 V – 1.95 V, V_{DDQ} = 1.70 V – 1.95 V
- Optimized operating (I_{DD0}, I_{DD4}), self refresh (I_{DD6}) and standby currents (I_{DD2}, I_{DD3})
- DDR I/O scheme with no DLL
- Programmable Partial Array Self Refresh (PASR)
- Temperature Compensated Self-Refresh (TCSR), controlled by on-chip temperature sensor
- Clock Stop, Power-Down and Deep Power-Down modes

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

TABLE 1
Performance

Part Number Speed Code		– 6	– 7.5	Unit
Clock Frequency (f_{CKmax})	CL = 3	166	133	MHz
	CL = 2	83	83	MHz
Access Time (t_{ACmax})		5.5	6.0	ns

TABLE 2
Memory Addressing Scheme

Item	Addresses
Banks	BA0, BA1
Rows	A0 - A12 (x16) A0 - A11 (x32)
Columns	A0 - A8

green Product

TABLE 3
Ordering Information

Type[1)]	Package	Description
Standard Temperature Range		
HYB18M256320CF–6/7.5	90–ball PG-VFBGA-60-3	166/133 MHz 4 Banks × 2 Mbit × 32 Low Power DDR SDRAM
HYB18M256160CF–6/7.5	60–ball PG-VFBGA-60-4	166/133 MHz 4 Banks × 4 Mbit × 16 Low Power DDR SDRAM
Extended Temperature Range		
HYE18M256320CF–6/7.5	90–ball PG-VFBGA-60-3	166/133 MHz 4 Banks × 2 Mbit × 32 Low Power DDR SDRAM
HYE18M256160CF–6/7.5	60–ball PG-VFBGA-60-4	166/133 MHz 4 Banks × 4 Mbit × 16 Low Power DDR SDRAM

1) HY[B/E]: Designator for memory products (HYB: Standard temp. range, HYE: Extended temp. range)
18M: 1.8V DDR Mobile-RAM
256: 256 MBit density
16/32: 16 or 32 bit interface width
C: die revisionF: green product
-6 / -7.5: speed grades (min. clock cycle time)

1.2 Pin Configuration

FIGURE 1
Standard Ballout 256-MBit x16 DDR Mobile-RAM (Top View 60-ball)

1	2	3		7	8	9
V_{SS}	DQ15	V_{SSQ}	A	V_{DDQ}	DQ0	V_{DD}
V_{DDQ}	DQ13	DQ14	B	DQ1	DQ2	V_{SSQ}
V_{SSQ}	DQ11	DQ12	C	DQ3	DQ4	V_{DDQ}
V_{DDQ}	DQ9	DQ10	D	DQ5	DQ6	V_{SSQ}
V_{SSQ}	UDQS	DQ8	E	DQ7	LDQS	V_{DDQ}
V_{SS}	UDM	NC	F	NC	LDM	V_{DD}
CKE	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
A9	A11	A12	H	$\overline{CS}$	BA0	BA1
A6	A7	A8	J	A10/AP	A0	A1
V_{SS}	A4	A5	K	A2	A3	V_{DD}

FIGURE 2
Standard Ballout 256-MBit x32 DDR Mobile-RAM (Top View 90-ball)

1	2	3		7	8	9
V_{SS}	DQ31	V_{SSQ}	A	V_{DDQ}	DQ16	V_{DD}
V_{DDQ}	DQ29	DQ30	B	DQ17	DQ18	V_{SSQ}
V_{SSQ}	DQ27	DQ28	C	DQ19	DQ20	V_{DDQ}
V_{DDQ}	DQ25	DQ26	D	DQ21	DQ22	V_{SSQ}
V_{SSQ}	DQS3	DQ24	E	DQ23	DQS2	V_{DDQ}
V_{DD}	DM3	NC	F	NC	DM2	V_{SS}
CKE	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
A9	A11	NC	H	$\overline{CS}$	BA0	BA1
A6	A7	A8	J	A10/AP	A0	A1
A4	DM1	A5	K	A2	DM0	A3
V_{SSQ}	DQS1	DQ8	L	DQ7	DQS0	V_{DDQ}
V_{DDQ}	DQ9	DQ10	M	DQ5	DQ6	V_{SSQ}
V_{SSQ}	DQ11	DQ12	N	DQ3	DQ4	V_{DDQ}
V_{DDQ}	DQ13	DQ14	P	DQ1	DQ2	V_{SSQ}
V_{SS}	DQ15	V_{SSQ}	R	V_{DDQ}	DQ0	V_{DD}

1.3 Description

The HY[B/E]18M256[16/32]0CF is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

The HY[B/E]18M256[16/32]0CF uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2n pre fetch architecture, with an interface designed to transfer two or four data words per clock cycle at the I/O pins. A single READ or WRITE access for the HY[B/E]18M256[16/32]0CF consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

The HY[B/E]18M256[16/32]0CF is especially designed for mobile applications. It operates from a 1.8V power supply. Power consumption in self refresh mode is drastically reduced by an On-Chip Temperature Sensor (OCTS); it can further be reduced by using the programmable Partial Array Self Refresh (PASR).

A conventional data-retaining Power-Down (PD) mode is available as well as a non-data-retaining Deep Power-Down (DPD) mode. For further power-savings the clock may be stopped during idle periods.

The HY[B/E]18M256[16/32]0CF is housed in a BGA package. It is available in Standard (-0°C to +70°C) and Extended (-25°C to +85°C) temperature ranges.

1.4 Pin Definition and Description

TABLE 4
Pin Description

Ball	Type	Detailed Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control inputs are sampled on crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides precharge power-down and self refresh operation (all banks idle), or active power-down (row active in any bank). CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DQ0 - DQ15 (x16)DQ0 - DQ31 (x32)	I/O	**Data Inputs/Output:** Bi-directional data bus
LDQS, UDQS (x16)DQS0 - DQS3 (x32)	I/O	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. For x16 LDQS corresponds to the data on DQ0 - DQ7; UDQS to the data on DQ8 - DQ15. For x32 DQS0 corresponds to the data on DQ0 - DQ7, DQS1 to the data on DQ8 - DQ15, DQS2 to the data on DQ16 - DQ23, DQS3 to the data on DQ24 - DQ31.
LDM, UDM (x16)DM0 - DM3 (x32)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x16 LDM corresponds to the data on DQ0 - DQ7; UDM to the data on DQ8 - DQ15. For x32 DM0 corresponds to the data on DQ0 - DQ7, DM1 to the data on DQ8 - DQ15, DM2 to the data on DQ16 - DQ23, DM3 to the data on DQ24 - DQ31.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an ACTIVATE, READ, WRITE or PRECHARGE command is being applied. BA0, BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS or EMRS).
A0 - A12 (x16) A0 - A11 (x32)	Input	**Address Inputs:** Provide the row address for ACTIVE commands and the column address and Auto Precharge bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 (=AP) is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10=LOW) or all banks (A10=HIGH). If only one bank is to be precharged, the bank is selected by BA0 and BA1. The address inputs also provide the op-code during a MODE REGISTER SET command.
V_{DDQ}	Supply	**I/O Power Supply:** Isolated power for DQ output buffers for improved noise immunity: V_{DDQ} = 1.70 V – 1.95 V
V_{SSQ}	Supply	**I/O Ground**
V_{DD}	Supply	**Power Supply:** Power for the core logic and input buffers, V_{DD} = 1.70 V – 1.95 V
V_{SS}	Supply	**Ground**
N.C.	–	**No Connect**

2 Functional Description

The DDR Mobile-RAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

READ and WRITE accesses to the DDR Mobile-RAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the banks, A0 - A12 (x16)/A0 - A11 (x32), select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR Mobile-RAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

2.1 Register Definition

2.1.1 Mode Register

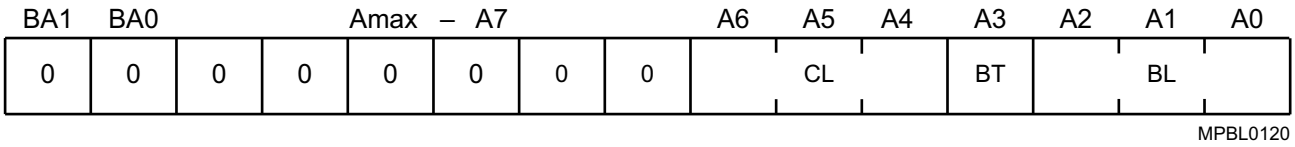
The Mode Register is used to define the specific mode of operation of the DDR Mobile-RAM. This definition includes the selection of a burst length (bits A0-A2), a burst type (bit A3) and a CAS latency (bits A4-A6). The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Full page bursts wrap within the page if the boundary is reached. Please note that full page bursts do not self-terminate; this implies that full-page read or write bursts with Auto Precharge are not legal commands. Full page burst has to start from an even column address.

Mode Register Definition (BA[1:0] = 00_B)



Field	Bits	Type	Description
CL	[6:4]	w	**CAS Latency** 010_B **CL** 2 011_B **CL** 3 *Note: All other bit combinations are RESERVED.*
BT	3	w	**Burst Type** 0_B **BT** Sequential 1_B **BT** Interleaved
BL	[2:0]	w	**Burst Length** 001_B **BL** 2 010_B **BL** 4 011_B **BL** 8 100_B **BL** 16 111_B **BL** Full page (Sequential burst type only) *Note: All other bit combinations are RESERVED.*
A	[Amax:7]	w	**Reserved address bits** *Note: Amax = A12 for x16, A11 for x32*

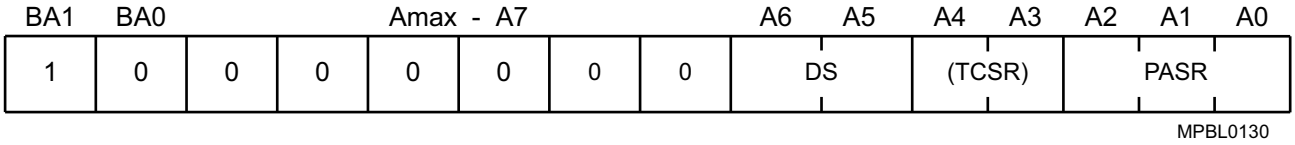
2.1.2 Extended Mode Register

The Extended Mode Register controls additional low power features of the device. These include the Partial Array Self Refresh (PASR), the Temperature Compensated Self Refresh (TCSR) and the drive strength selection for the DQs. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 1) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation. Address bits A0 - A2 specify the Partial Array Self Refresh (PASR) and bits A5 - A6 the Drive Strength, while bits A7 - Amax shall be written to zero. Bits A3 and A4 are “don’t care” (see below).

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Mode Register Definition (BA[1:0] = 00_B)



Field	Bits	Type	Description
DS	[6:5]	w	**Selectable Drive Strength** 00_B **DS** Full Drive Strength 01_B **DS** Half Drive Strength 10_B **DS** Quarter Drive Strength 11_B **DS** 1/8 Drive Strength
TCSR	[4:3]	w	**Temperature Compensated Self Refresh** XX_B **TCSR** Superseded by on-chip temperature sensor (see text)
PASR	[2:0]	w	**Partial Array Self Refresh** 000_B **PASR** all banks 001_B **PASR** half array (BA1 = 0) 010_B **PASR** quarter array (BA1 = BA0 = 0) *Note: All other bit combinations are RESERVED.*
A	[Amax:7]	w	**Reserved address bits** *Note: Amax = A12 for x16, A11 for x32*

2.2 Function Truth Tables

TABLE 5
Truth Table - CKE

CKEn-1	CKEn	Current State	Command	Action	Note
L	L	Power-Down	X	Maintain Power-Down	1)2)3)4)
		Self Refresh	X	Maintain Self Refresh	1)2)3)4)
		Deep Power-Down	X	Maintain Deep Power-Down	1)2)3)4)
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	1)2)3)4)5)
		Self Refresh	DESELECT or NOP	Exit Self Refresh	1)2)3)4)5)
		Deep Power-Down	X	Exit Deep Power-Down	1)2)3)4)6)
H	L	All Banks Idle	DESELECT or NOP	Enter Precharge Power-Down	1)2)3)4)
		Bank(s) Active	DESELECT or NOP	Enter Active Power-Down	1)2)3)4)
		All Banks Idle	AUTO REFRESH	Enter Self Refresh	1)2)3)4)
		All Banks Idle	BURST TERMINATE	Enter Deep Power-Down	1)2)3)4)
H	H	See **Table 6** and **Table 7**			1)2)3)4)

1) CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2) Current state is the state immediately prior to clock edge n.
3) COMMAND n is the command registered at clock edge n; ACTION n is a result of COMMAND n.
4) All states and sequences not shown are illegal or reserved.
5) DESELECT or NOP commands should be issued on any clock edges occurring during t_{XP} or t_{XSR} period.
6) Exit from DEEP POWER DOWN requires the same command sequence as for power-up initialization.

TABLE 6
Current State Bank n - Command to Bank n

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Note
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1)2)3)4)5)6)
Idle	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	L	L	H	AUTO REFRESH	1)2)3)4)5)6)7)
	L	L	L	L	MODE REGISTER SET	1)2)3)4)5)6)7)
Row Active	L	H	L	H	READ (select column and start Read burst)	1)2)3)4)5)6)8)
	L	H	L	L	WRITE (select column and start Write burst)	1)2)3)4)5)6)8)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1)2)3)4)5)6)9)
Read (Auto-Precharge Disabled)	L	H	L	H	READ (truncate Read and start new Read burst)	1)2)3)4)5)6)8)
	L	H	L	L	WRITE (truncate Read and start new Write burst)	1)2)3)4)5)6)8)10)
	L	L	H	L	PRECHARGE (truncate Read and start Precharge)	1)2)3)4)5)6)9)
	L	H	H	L	BURST TERMINATE	1)2)3)4)5)6)11)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Note
Write (Auto-Precharge Disabled)	L	H	L	H	READ (truncate Write and start Read burst)	1)2)3)4)5)6)8)12)
	L	H	L	L	WRITE (truncate Write and start Write burst)	1)2)3)4)5)6)8)
	L	L	H	L	PRECHARGE (truncate Write burst, start Precharge)	1)2)3)4)5)6)9)12)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH (see **Table 7**) and after t_{XP} or t_{XSR} has been met (if the previous state was POWER-DOWN or SELF REFRESH).
2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3) Current state definitions:Idle: The bank has been precharged, and t_{RP} has been met.Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.Read: A read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.Write: A write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4) The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to **Table 7**.Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the “idle” state.Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the “row active” state.Read with AP enabled: Starts with registration of a READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.Write with AP enabled: Starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
5) The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.Refreshing: Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the DDR Mobile-RAM is in the “all banks idle” state.Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR Mobile-RAM is in the “all banks idle” state.Precharging All: Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks are in the idle state.
6) All states and sequences not shown are illegal or reserved.
7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
8) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
9) May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
10) A WRITE command may be applied after the completion of the Read burst; otherwise, a BURST TERMINATE command must be used to end the Read burst prior to issuing a WRITE command.
11) Not bank-specific; BURST TERMINATE affects the most recent Read burst, regardless of bank.
12) Requires appropriate DM masking.

TABLE 7

Current State Bank n - Command to Bank m (different bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Note
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1)2)3)4)5)6)
Idle	X	X	X	X	Any command otherwise allowed to bank m	1)2)3)4)5)6)
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (select column and start Read burst)	1)2)3)4)5)6)7)
	L	H	L	L	WRITE (select column and start Write burst)	1)2)3)4)5)6)7)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1)2)3)4)5)6)
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (truncate Read and start new Read burst)	1)2)3)4)5)6)7)
	L	H	L	L	WRITE (truncate Read and start Write burst)	1)2)3)4)5)6)7)8)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1)2)3)4)5)6)
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (truncate Write and start Read burst)	1)2)3)4)5)6)7)9)
	L	H	L	L	WRITE (truncate Write and start new Write burst)	1)2)3)4)5)6)7)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1)2)3)4)5)6)
Read(with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (truncate Read and start new Read burst)	1)2)3)4)5)6)7)
	L	H	L	L	WRITE (truncate Read and start Write burst)	1)2)3)4)5)6)7)8)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1)2)3)4)5)6)
Write(with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (truncate Write and start Read burst)	1)2)3)4)5)6)7)
	L	H	L	L	WRITE (truncate Write and start new Write burst)	1)2)3)4)5)6)7)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1)2)3)4)5)6)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH (see **Table 7**) and after t_{XP} or t_{XSR} has been met (if the previous state was power-down or self refresh).
2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3) Current state definitions:Idle: The bank has been precharged, and t_{RP} has been met.Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.Read: A read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.Write: A write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.Read with AP enabled: Starts with registration of a READ command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank is in the idle state.Write with AP enabled: Starts with registration of a WRITE command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank is in the idle state.
4) AUTO REFRESH, SELF REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6) All states and sequences not shown are illegal or reserved.
7) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8) A WRITE command may be applied after the completion of the Read burst; otherwise, a BURST TERMINATE command must be used to end the Read burst prior to issuing a WRITE command.
9) Requires appropriate DM masking.

3 Electrical Characteristics

3.1 Operating Conditions

TABLE 8
Absolute Maximum Ratings

Parameter		Symbol	Values		Unit	Note
			Min.	Max.		
Power Supply Voltage		V_{DD}	-0.3	2.7	V	–
Power Supply Voltage for Output Buffer		V_{DDQ}	-0.3	2.7	V	–
Input Voltage		V_{IN}	-0.3	V_{DDQ} + 0.3	V	–
Output Voltage		V_{OUT}	-0.3	V_{DDQ} + 0.3	V	–
Operation Case Temperature	Extended	T_C	-25°	+85	°C	–
Storage Temperature		T_{STG}	-55	+150	°C	–
Power Dissipation		P_D	–	0.7	W	–
Short Circuit Output Current		I_{OUT}	–	50	mA	–

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

TABLE 9
Pin Capacitances

Parameter	Symbol	Values		Unit	Note[1) 2)3)]
		Min.	Max.		
Input capacitance: CK, $\overline{CK}$	C_{I1}	2.5	5.0	pF	–
Input capacitance: all other input-only pins	C_{I2}	1.5	3.5	pF	–
Input/output capacitance: DQ, DQS, DM	C_{IO}	2.0	4.5	pF	–

1) These values are not subject to production test but verified by device characterization.
2) Input capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{DD}, V_{DDQ} are applied and all other pins (except the pin under test) are floating. DQ's should be in high impedance state. This may be achieved by pulling CKE to low level.
3) Although DM is an input-only pin, it's input capacitance models the input capacitance of the DQ and DQS pins.

TABLE 10
Electrical Characteristics

Parameter	Symbol	Values		Unit	Note[1)2)]
		Min.	Max.		
Power Supply Voltage	V_{DD}	1.70	1.95	V	–
Power Supply Voltage for DQ Output Buffer	V_{DDQ}	1.70	1.95	V	–
Input leakage current	I_{IL}	-1.0	1.0	µA	–
Output leakage current	I_{OL}	-1.0	1.0	µA	–
Address and Command Inputs (BA, BA1, CKE, CS, RAS, CAS, WE)					
Input high voltage	V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	–
Input low voltage	V_{IL}	-0.3	0.2 × V_{DDQ}	V	–
Clock Inputs (CK, $\overline{CK}$)					
DC input voltage	V_{IN}	-0.3	V_{DDQ} + 0.3	V	–
DC input differential voltage	$V_{ID(DC)}$	0.4 × V_{DDQ}	V_{DDQ} + 0.6	V	3)
AC input differential voltage	$V_{ID(AC)}$	0.6 × V_{DDQ}	V_{DDQ} + 0.6	V	3)
AC differential cross point voltage	V_{IX}	0.4 × V_{DDQ}	0.6 × V_{DDQ}	V	4)
Data Inputs (DQ, DM, DQS)					
DC input high voltage	$V_{IHD(DC)}$	0.7 × V_{DDQ}	V_{DDQ} + 0.3	V	–
DC input low voltage	$V_{ILD(DC)}$	-0.3	0.3 x V_{DDQ}	V	–
AC input high voltage	$V_{IHD(AC)}$	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	–
AC input low voltage	$V_{ILD(AC)}$	-0.3	0.2 × V_{DDQ}	V	–
Data Outputs (DQ, DQS)					
Output high voltage (I_{OH} = -0.1 mA)	V_{OH}	0.9 × V_{DDQ}	–	V	–
Output low voltage (I_{OL} = 0.1 mA)	V_{OL}	–	0.1 × V_{DDQ}	V	–

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25°C ≤ T_C ≤ 85 °C (ext.)All voltages referenced to V_{SS}. V_{SS} and V_{SSQ} must be at same potential.
2) See **Table 12** and **Figure 4** for overshoot and undershoot definition.
3) V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK.
4) The value of V_{IX} is expected to be equal to 0.5 x V_{DDQ} and must track variations in the DC level.

3.2 AC Characteristics

TABLE 11
AC Characteristics

Parameter		Symbol	– 6		– 7.5		Unit	Note 1)2)3)4)
			Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$		t_{AC}	2.0	5.5	2.5	6.0	ns	5)6)
DQS output access time from CK/$\overline{CK}$		t_{DQSCK}	2.0	5.5	2.5	6.0	ns	5)6)
Clock high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	–
Clock low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	–
Clock half period		t_{HP}	min(t_{CL}, t_{CH})		min(t_{CL}, t_{CH})		ns	7)8)
Clock cycle time	CL = 3	t_{CK}	6	–	7.5	–	ns	
	CL = 2		12	–	12	–		
DQ and DM input Setup time	fast slew rate	t_{DS}	0.6	–	0.75	–	ns	9)10)11)
	slow slew rate		0.7	–	0.85	–		9)10)12)
DQ and DM input hold time	Fast slew rate	t_{DH}	0.6	–	0.75	–	ns	9)10)12)
	Slow slew rate		0.7	–	0.85	–		9)10)13)
DQ and DM input pulse width		t_{DIPW}	1.5	–	1.7	–	ns	13)
Address and control input Setup time	fast slew rate	t_{IS}	1.1	–	1.3	–	ns	12)14)15)
	slow slew rate		1.3	–	1.5	–		13)15)16)
Address and control input hold time	fast slew rate	t_{IH}	1.1	–	1.3	–	ns	12)15)16)
	slow slew rate		1.3	–	1.5	–		13)15)16)
Address and control input pulse width		t_{IPW}	2.6	–	3.0	–	ns	14)
DQ & DQS low-impedance time from CK/$\overline{CK}$		t_{LZ}	1.0	–	1.0	–	ns	16)
DQ & DQS high-impedance time from CK/$\overline{CK}$		t_{HZ}	–	5.5	–	6.0	ns	17)
DQS - DQ skew		t_{DQSQ}	–	0.5	–	0.6	ns	17)
DQ / DQS output hold time from DQS		t_{QH}	t_{HP}-t_{QHS}	–	t_{HP}-t_{QHS}	–	ns	8)
Data hold skew factor		t_{QHS}	–	0.55	–	0.75	ns	8)
Write command to 1st DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	–
DQS input high-level width		t_{DQSH}	0.4	0.6	0.4	0.6	t_{CK}	–
DQS input low-level width		t_{DQSL}	0.4	0.6	0.4	0.6	t_{CK}	–
DQS input cycle time		t_{DSC}	0.9	1.1	0.9	1.1	t_{CK}	–
DQS falling edge to CK setup time		t_{DSS}	0.2	–	0.2	–	t_{CK}	–
DQS falling edge hold time from CK		t_{DSH}	0.2	–	0.2	–	t_{CK}	–
MODE REGISTER SET command period		t_{MRD}	2	–	2	–	t_{CK}	–
Write preamble setup time		t_{WPRES}	0	–	0	–	ns	18)
Write preamble hold time		t_{WPREH}	0.25	–	0.25	–	t_{CK}	–
Write postamble		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}	19)
Write preamble		t_{WPRE}	0.25	–	0.25	–	t_{CK}	–

Parameter		Symbol	– 6		– 7.5		Unit	Note 1)2)3)4)
			Min.	Max.	Min.	Max.		
Read preamble	CL = 3	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	20)
	CL = 2		–	–	0.5	1.1		
Read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}	–
ACTIVE to PRECHARGE command period		t_{RAS}	42	70k	45	70k	ns	21)
ACTIVE to ACTIVE command period		t_{RC}	60	–	67	–	ns	22)
AUTO REFRESH to ACTIVE/AUTO REFRESH command period		t_{RFC}	72	–	75	–	ns	22)
ACTIVE to READ or WRITE delay		t_{RCD}	18	–	22.5	–	ns	22)
Col address to col address delay		t_{CCD}	1	–	1	–	t_{CK}	
PRECHARGE command period		t_{RP}	18	–	22.5	–	ns	22)
ACTIVE bank A to ACTIVE bank B delay		t_{RRD}	12	–	15	–	ns	22)
WRITE recovery time		t_{WR}	15	–	15	–	ns	22)
Auto precharge write recovery + precharge time		t_{DAL}	$(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$				t_{CK}	22)
Internal write to Read command delay		t_{WTR}	1	–	1	–	t_{CK}	23)
Self refresh exit to next valid command delay		t_{XSR}	120	–	120	–	ns	22)
Exit power down delay		t_{XP}	$t_{CK} + t_{IS}$	–	$t_{CK} + t_{IS}$	–	ns	–
CKE minimum low time		t_{CKE}	2	–	2	–	t_{CK}	–
Refresh period		t_{REF}	–	64	–	64	ms	
Average periodic refresh interval		t_{REFI}	–	7.8 (× 16) 15.6 (x32)	–	7.8 (× 16) 15.6 (x32)	µs	24)

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25°C ≤ T_C ≤ 85 °C (ext.);V_{DD} = 1.70 V - 1.95 V, V_{DDQ} = 1.70 V - 1.95 V. All voltages referenced to V_{SS}.
2) All parameters assume proper device initialization.
3) The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$; the input reference level for signals other than CK/$\overline{CK}$ is V_{DDQ}/2.
4) All AC timing characteristics assume an input slew rate of 1.0 V/ns.
5) The output timing reference level is V_{DDQ}/2.
6) Parameters t_{AC} and t_{QH} are specified for full drive strength and a reference load see **Figure 3**. This circuit is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. For half drive strength with a nominal load of 10pF parameters t_{AC} and t_{QH} are expected to be in the same range. However, these parameters are not subject to production test but are estimated by device characterization. Use of IBIS or other simulation tools for system validation is suggested.
7) Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
8) t_{QH} = t_{HP} - t_{QHS}, where tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
9) DQ, DM and DQS input slew rate is measured between $V_{ILD(DC)}$ and $V_{IHD(AC)}$ (rising) or $V_{IHD(DC)}$ and $V_{ILD(AC)}$ (falling).
10) DQ, DM and DQS input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
11) Input slew rate ≥ 1.0 V/ns.
12) Input slew rate ≥ 0.5V/ns and < 1.0 V/ns.
13) These parameters guarantee device timing. They are verified by device characterization but are not subject to production test.
14) The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
15) A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for this parameter.
16) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

17) t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
18) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
19) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
20) A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
21) These parameters account for the number of clock cycles and depend on the operating frequency, as follows:no. of clock cycles = specified delay / clock period; round to the next higher integer.
22) t_{DAL} = (t_{WR} / t_{CK}) + (t_{RP} / t_{CK}): for each of the terms above, if not already an integer, round to the next higher integer.
23) t_{WTR} is also referred to as t_{CDLR}
24) A maximum of eight AUTOREFRESH commands can be posted to the DDR Mobile-RAM device, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8 * t_{REFI}.

FIGURE 3
Measurement with Reference Load

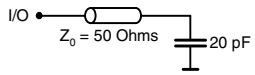
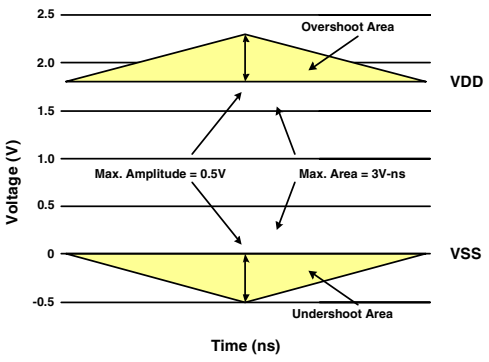


TABLE 12
AC Overshoot / Undershoot Specification

Parameter	Max.	Unit	Note
Maximum peak amplitude allowed for overshoot	0.5	V	–
Maximum peak amplitude allowed for undershoot	0.5	V	–
Maximum overshoot area above V_{DD}	3.0	V-ns	–
Maximum undershoot area below V_{SS}	3.0	V-ns	–

FIGURE 4
AC Overshoot and Undershoot Definition



3.3 Operating Currents

TABLE 13
Maximum Operating Currents

Parameter & Test Conditions	Symbol	Values		Unit	Note 1)2)3)4)5)
		– 6	– 7.5		
Operating one bank active-precharge current: $t_{RC} = t_{RCmin}$; $t_{CK} = t_{CKmin}$; CKE is HIGH; CS is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	I_{DD0}	45 (x16) 60 (x32)	40 (x16) 55 (x32)	mA	
Precharge power-down standby current: All banks idle, CKE is LOW; CS is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2P}	0.7	0.7	mA	
Precharge power-down standby current with clock stop: All banks idle, CKE is LOW; CS is HIGH, CK = LOW, CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2PS}	0.3	0.3	mA	
Precharge non power-down standby current: All banks idle, CKE is HIGH; CS is HIGH, $t_{CK} = t_{CKmin}$;address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2N}	15	15	mA	
Precharge non power-down standby current with clock stop: All banks idle, CKE is HIGH; CS is HIGH, CK = LOW, CK = HIGH;address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2NS}	8	8	mA	
Active power-down standby current: One bank active, CKE is LOW; CS is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3P}	2.0	2.0	mA	
Active power-down standby current with clock stop: One bank active, CKE is LOW; CS is HIGH, CK = LOW, CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3PS}	1.5	1.5	mA	
Active non power-down standby current: One bank active, CKE is HIGH; CS is HIGH, $t_{CK} = t_{CKmin}$;address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3N}	25	23	mA	
Active non power-down standby current with clock stop: One bank active, CKE is HIGH; CS is HIGH, CK = LOW, CK = HIGH;address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3NS}	20	20	mA	
Operating burst read current: One bank active; BL = 4; CL = 3; $t_{CK} = t_{CKmin}$; continuous read bursts; IOUT = 0 mAaddress inputs are SWITCHING; 50% data change each burst transfer	I_{DD4R}	115 (x16) 140 (x32)	90 (x16) 110 (x32)	mA	
Operating burst write current: One bank active; BL = 4; $t_{CK} = t_{CKmin}$; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	I_{DD4W}	110 (x16) 115 (x32)	85 (x16) 90 (x32)	mA	
Auto-Refresh current: $t_{RC} = t_{RFCmin}$; $t_{CK} = t_{CKmin}$; burst refresh; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD5}	75 (x16) 120 (x32)	70 (x16) 110 (x32)	mA	

Parameter & Test Conditions	Symbol	Values		Unit	Note 1)2)3)4)5)
		– 6	– 7.5		
Self refresh current: CKE is LOW; CK = LOW, CK = HIGH; address and control inputs are STABLE; data bus inputs are STABLE	I_{DD6}	See **Table 14**		µA	
Deep Power Down current	I_{DD8}	10	10	µA	6)

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25°C ≤ T_C ≤ 85 °C (ext.); V_{DD} = 1.70 V - 1.95 V, V_{DDQ} = 1.70 V - 1.95 V.Recommended Operating Conditions unless otherwise noted
2) IDD specifications are tested after the device is properly initialized and measured at 133 MHz for -7.5 speed grade, and 166 MHz for -6 speed grade.
3) Input slew rate is 1.0 V/ns.
4) Definitions for I_{DD}:LOW is defined as VIN ≤ 0.1 * VDDQ;HIGH is defined as VIN ≥ 0.9 * VDDQ;STABLE is defined as inputs stable at a HIGH or LOW level;SWITCHING is defined as:- address and command: inputs changing between HIGH and LOW once per two clock cycles;- data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE
5) All parameters are measured with no output loads.
6) Value shown as typical and measured at 25 °C.

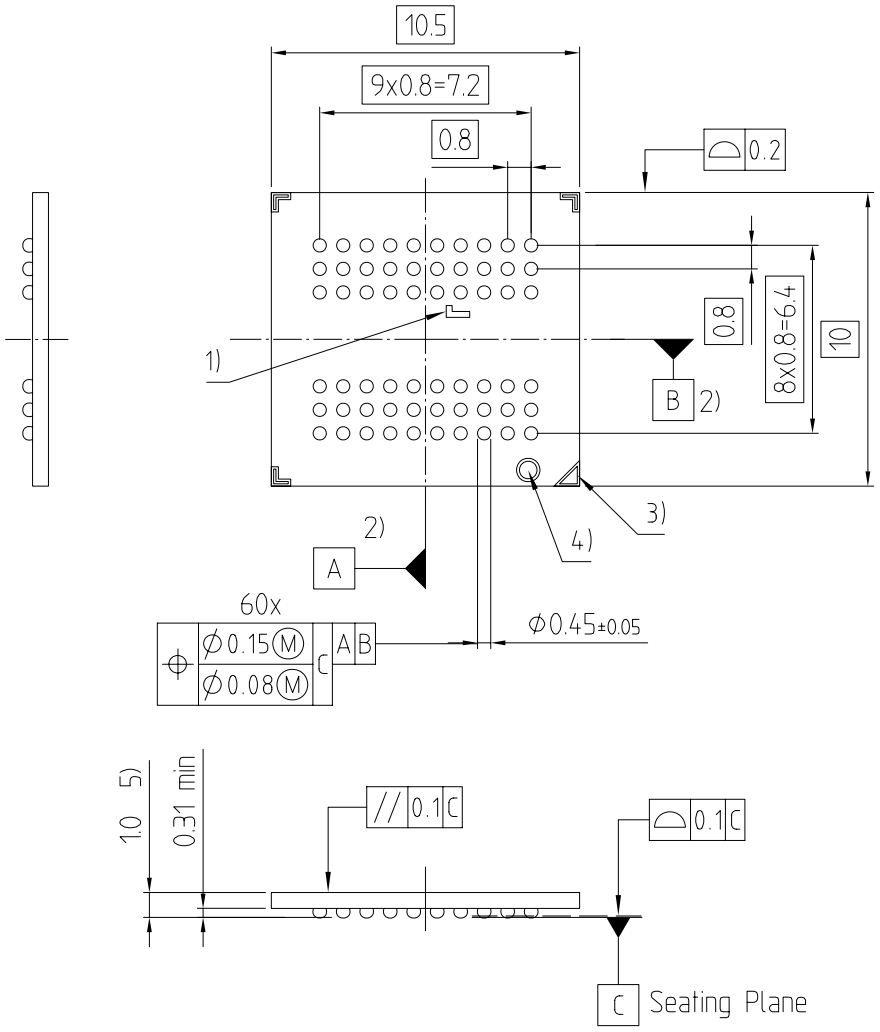
TABLE 14
Self Refresh Currents

Parameter & Test Conditions	Max. Temperature	Symbol	Values		Units	Note
			Typ.	Max.		
Self refresh mode, Full array (PASR = 000)	85 °C	I_{DD6}	275	400	µA	1)2)
	40 °C		145	–		
Self refresh mode, Half array (PASR = 001)	85 °C		210	340		
	40 °C		115	–		
Self refresh mode, Quarter array (PASR = 010)	85 °C		185	310		
	40 °C		100	–		

1) -25 °C ≤ T_J ≤ 85 °C (ext.); V_{DD} = V_{DDQ} = 1.70V to 1.95V
2) For commercial temperature range part (HYB), the max value indicated for 85 °C applies to 70 °C

4 Package Outlines

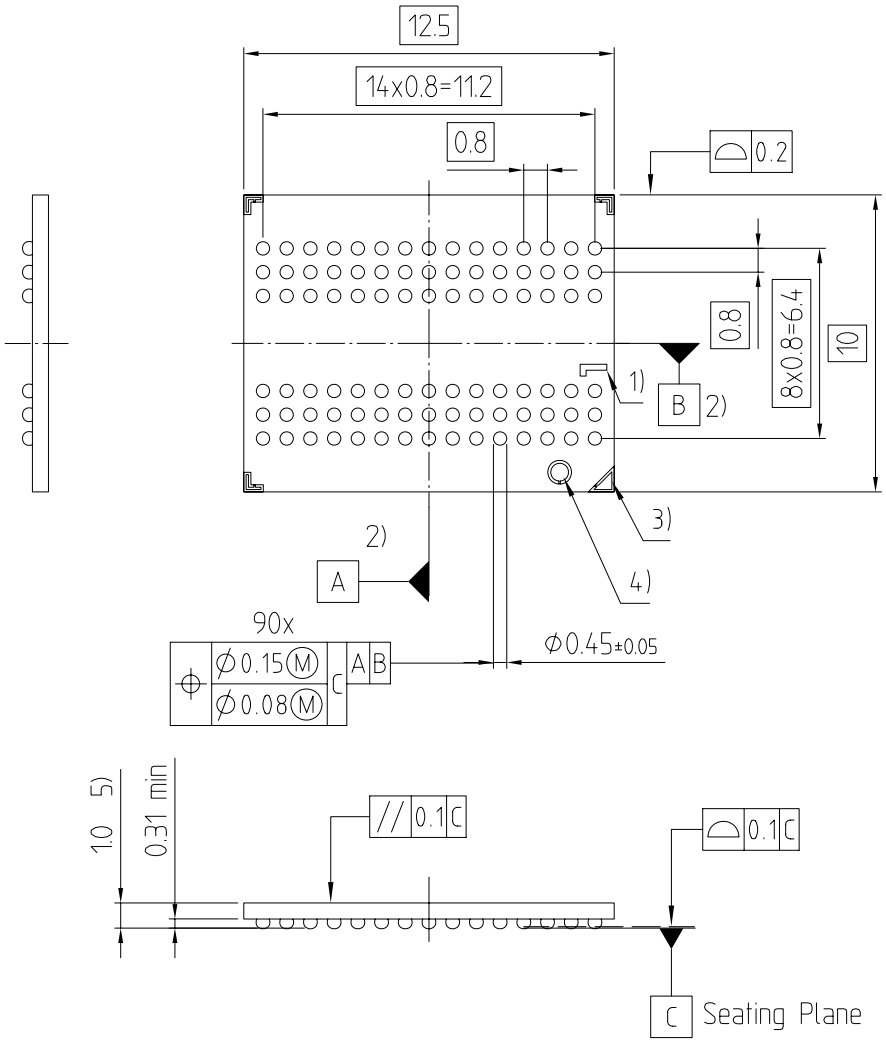
FIGURE 5
60–ball PG-VFBGA-60-4 (x16)



Notes

1. *Solder ball attach fiducial (SBA)*
2. *Middle of package edges*
3. *Package orientation mark A1*
4. *Bad unit marking (BUM)*
5. *Tolerances regarding ISO 2768-mK*
6. *Dimensions in mm*

FIGURE 6
90–ball PG-VFBGA-60-3 (x32)



Notes

1. *Solder ball attach fiducial (SBA)*
2. *Middle of package edges*
3. *Package orientation mark A1*
4. *Bad unit marking (BUM)*
5. *Tolerances regarding ISO 2768-mK*
6. *Dimensions in mm*

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