



STD36NH02L

N-channel 24V - 0.011 Ω - 30A - DPAK
STripFET™ III Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STD36NH02L	24V	<0.0145 Ω	30A ⁽¹⁾

1. Guaranteed when external R_g=4.7 Ω and t_f < t_{fmax}

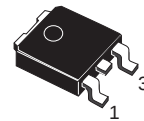
- R_{DS(on)} * Q_g industry's benchmark
- Conduction losses reduced
- Switching losses reduced

Description

This series of products utilizes the last advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

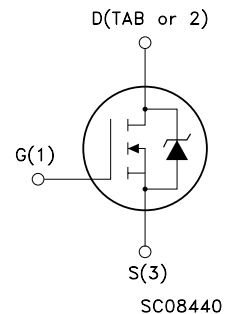
Applications

- Switching application



TO-252

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD36NH02L	D36NH02L	DPAK	Tape & reel

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuit** 8

4 **Package mechanical data** 9

5 **Packaging mechanical data** 11

6 **Revision history** 12

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{\text{spike}}^{(1)}$	Drain-source voltage rating	30	V
V_{DS}	Drain-Source Voltage ($V_{\text{GS}} = 0$)	24	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_{\text{D}}^{(2)}$	Drain Current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	30	A
I_{D}	Drain Current (continuous) at $T_{\text{C}}=100^{\circ}\text{C}$	30	A
$I_{\text{DM}}^{(3)}$	Drain Current (pulsed)	120	A
P_{TOT}	Total Dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	45	W
	Derating Factor	0.27	W/ $^{\circ}\text{C}$
$E_{\text{AS}}^{(4)}$	Single pulse avalanche energy	200	mJ
T_{J} T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 175	$^{\circ}\text{C}$

1. Guaranteed when external $R_{\text{g}}=4.7\Omega$ and $t_{\text{f}} < t_{\text{fmax}}$

2. Value limited by wire bonding

3. Pulse width limited by safe operating area.

4. Starting $T_{\text{J}}=25^{\circ}\text{C}$, $I_{\text{D}}=19\text{A}$, $V_{\text{DD}}=18\text{V}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{\text{thj-case}}$	Thermal resistance junction-case Max	3.33	$^{\circ}\text{C}/\text{W}$
$R_{\text{thj-amb}}$	Thermal resistance junction-ambient Max	100	$^{\circ}\text{C}/\text{W}$
T_{I}	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1mA, V _{GS} = 0	24			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 20V, V _{DS} = 20V @125°C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1	1.8	2.5	V
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10V, I _D = 15A V _{GS} = 5V, I _D = 15A		0.011 0.013	0.0145 0.026	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 10V, I _D = 15A		18		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output Capacitance Reverse transfer capacitance	V _{DS} = 15V, f = 1 MHz, V _{GS} = 0		860 255 45		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	0.44V ≤ V _{DD} ≤ 10V, I _D = 30A, V _{GS} = 10V (see Figure 14)		15.5 4.1 1.7	20	nC nC nC
Q _{OSS} ⁽²⁾	Output charge	V _{DS} = 16V, V _{GS} = 0		6		ns
R _G	Gate input resistance	f = 1 MHz Gate DC Bias = 0 Test signal level = 20mV open drain		3		Ω

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

2. Q_{OSS} = C_{oss} * ΔV_{IN}, C_{oss} = C_{gd} + C_{ds}

Table 5. Switching times

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=10V$, $I_D=15A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 13)		8		ns
t_r	Rise time			70		ns
$t_{d(off)}$	Turn-off delay time			22		ns
t_f	Fall time			15		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				30	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				120	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15A$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 30A$, $di/dt = 100A/\mu s$, $V_{DD}=15V$, $T_j=150^\circ C$ (see Figure 15)		24		ns
Q_{rr}	Reverse recovery charge			16		nC
I_{RRM}	Reverse recovery current			1.3		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

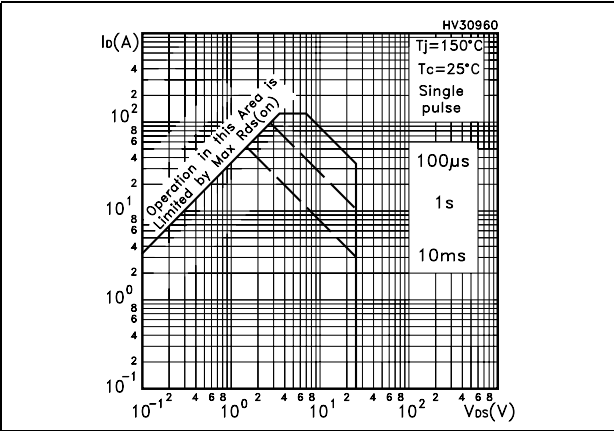


Figure 2. Thermal impedance

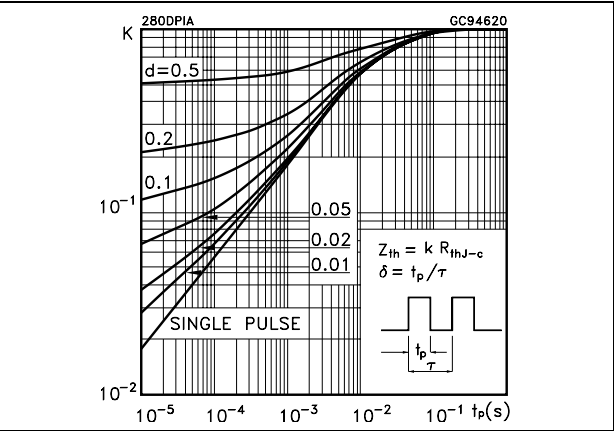


Figure 3. Output characteristics

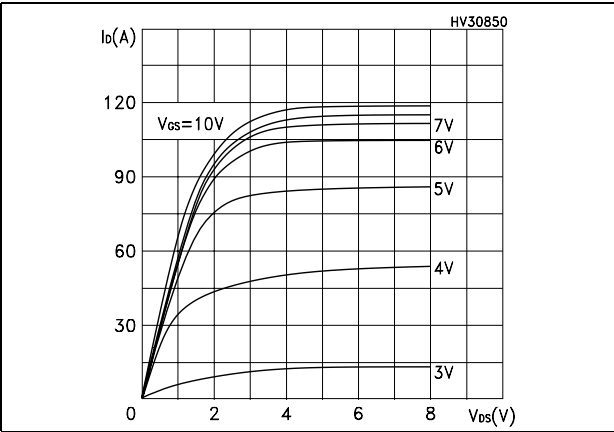


Figure 4. Transfer characteristics

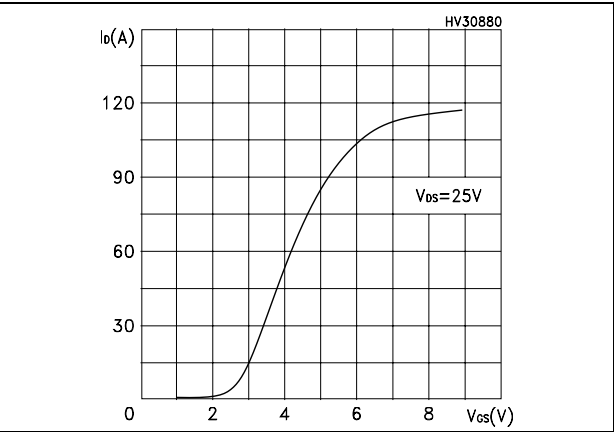


Figure 5. Transconductance

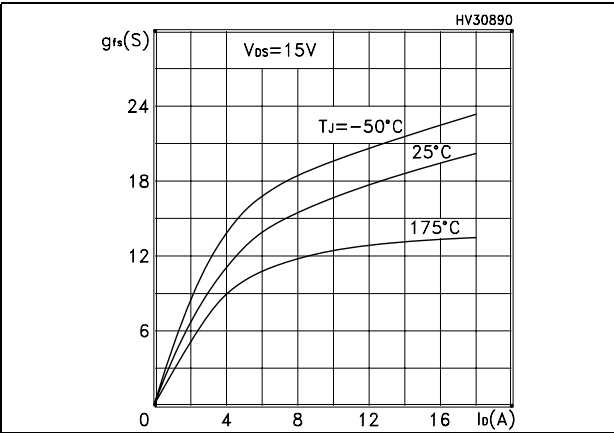


Figure 6. Static drain-source on resistance

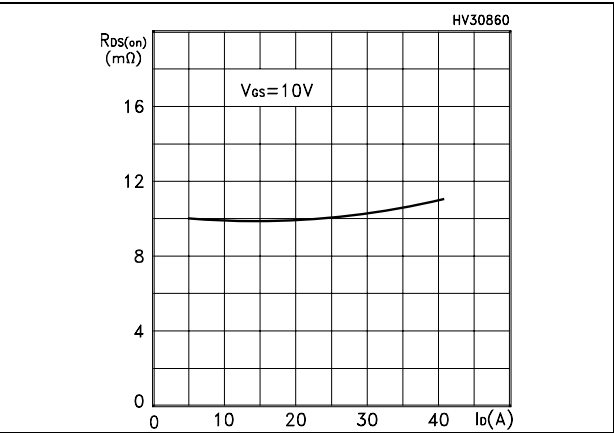


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

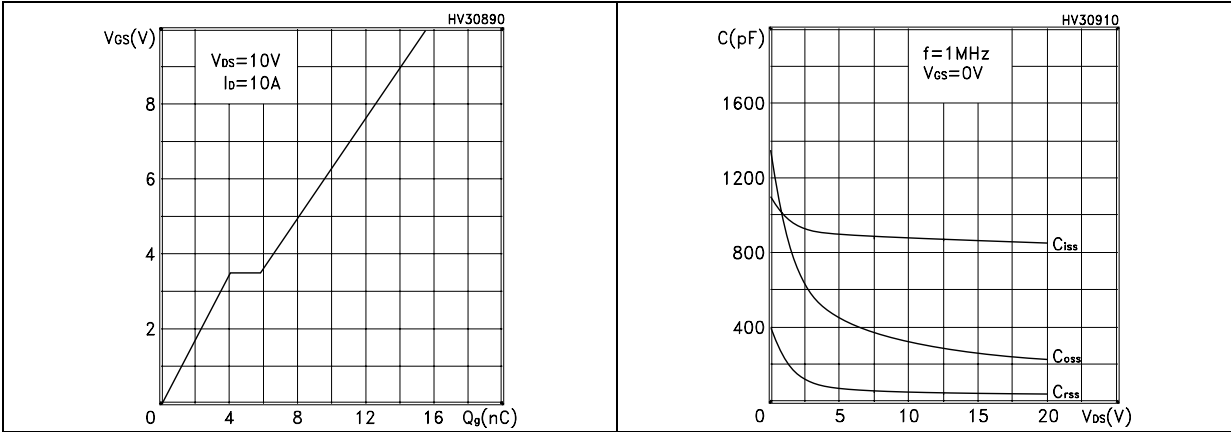


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

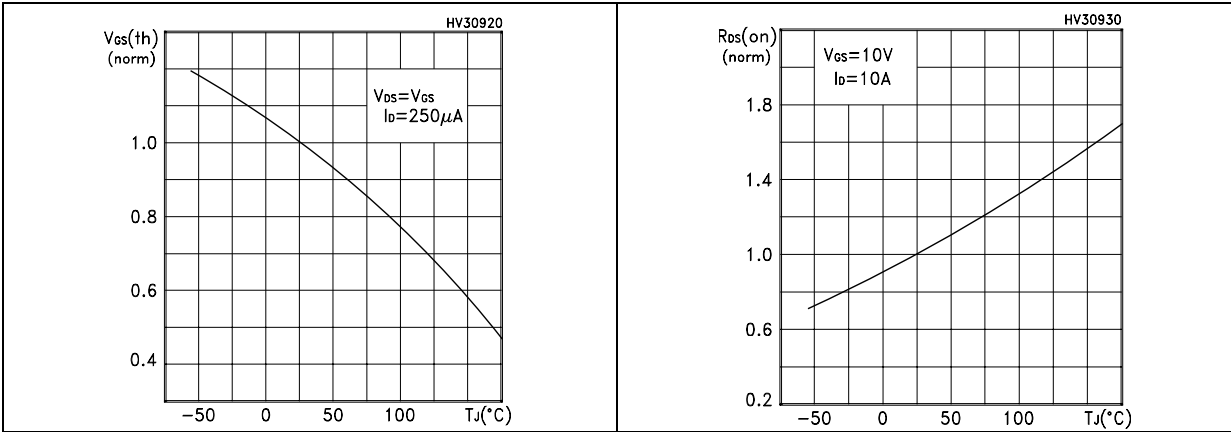
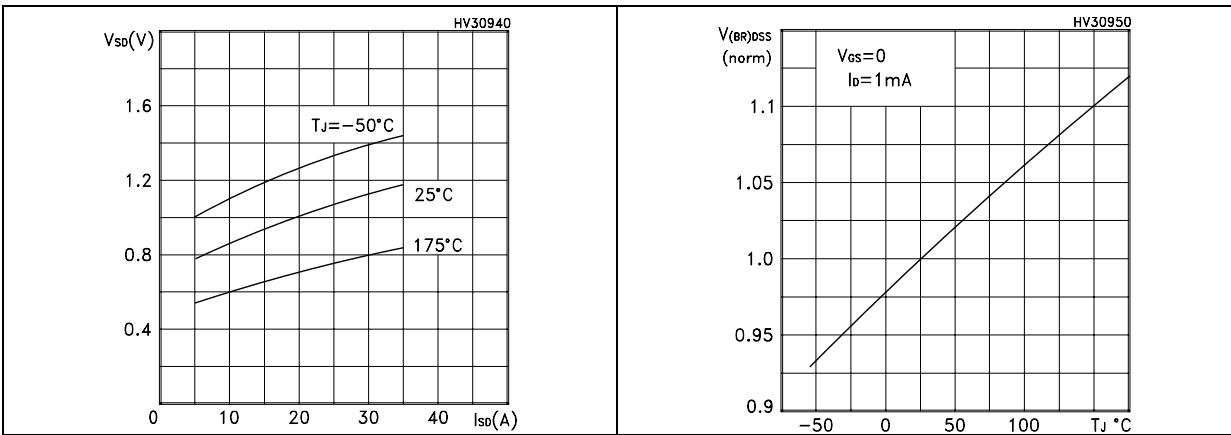


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized B_{VDS} vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

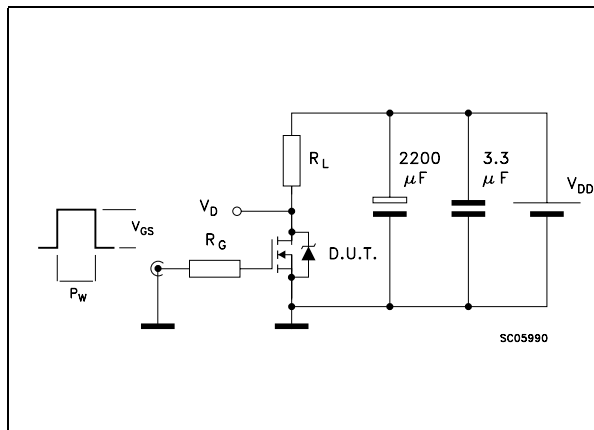


Figure 14. Gate charge test circuit

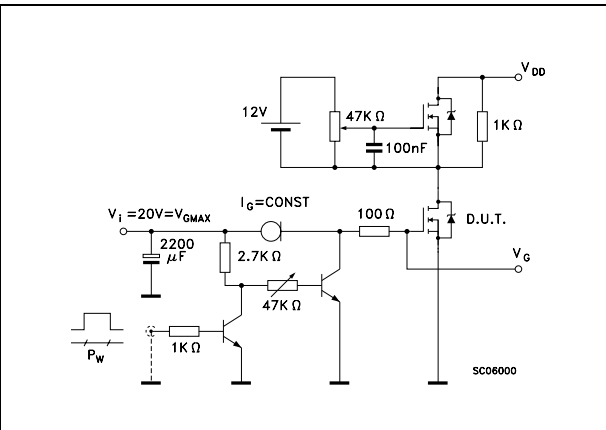


Figure 15. Test circuit for inductive load switching and diode recovery times

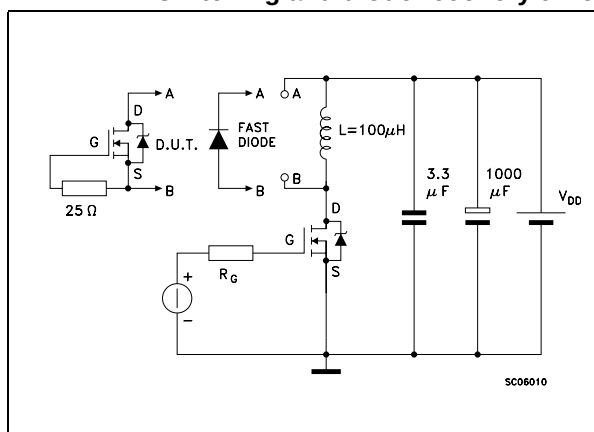


Figure 16. Unclamped inductive load test circuit

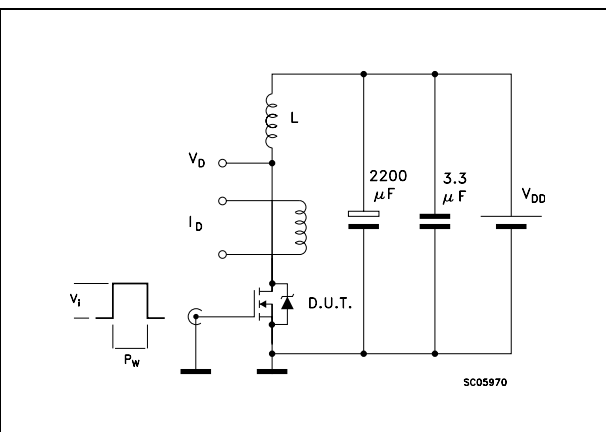


Figure 17. Unclamped inductive waveform

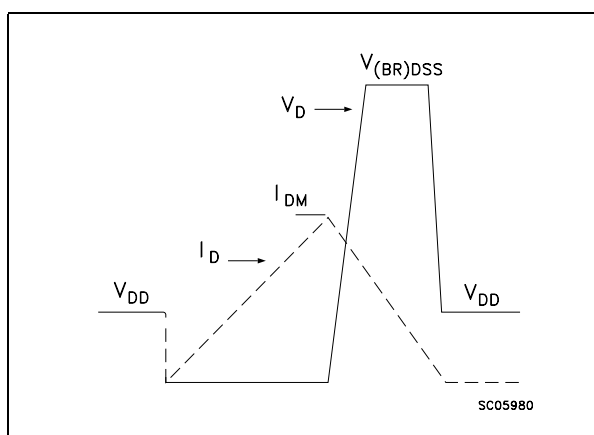
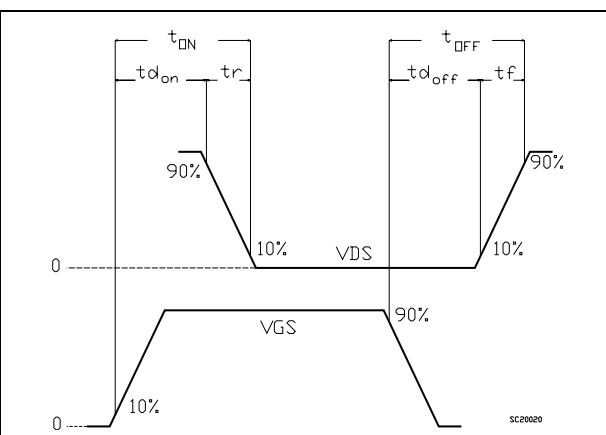


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

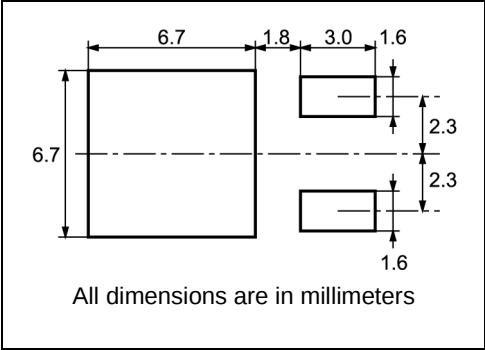
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The drawing illustrates the mechanical specifications of the STD36NH02L DPAK package. It includes a top view showing dimensions A, A1, A2, B, b4, C, C2, D, D1, E, E1, e, e1, H, L, (L1), L2, L4, R, and V2. A side view shows dimensions A, A1, A2, B, b4, C, C2, D, D1, E, E1, e, e1, H, L, (L1), L2, L4, R, and V2. A detail view of the thermal pad shows dimensions A2, (L1), L, V2, and GAUGE PLANE. A detail view of the seating plane shows dimensions A2, (L1), L, V2, and GAUGE PLANE. A detail view of the thermal pad shows dimensions A2, (L1), L, V2, and GAUGE PLANE.

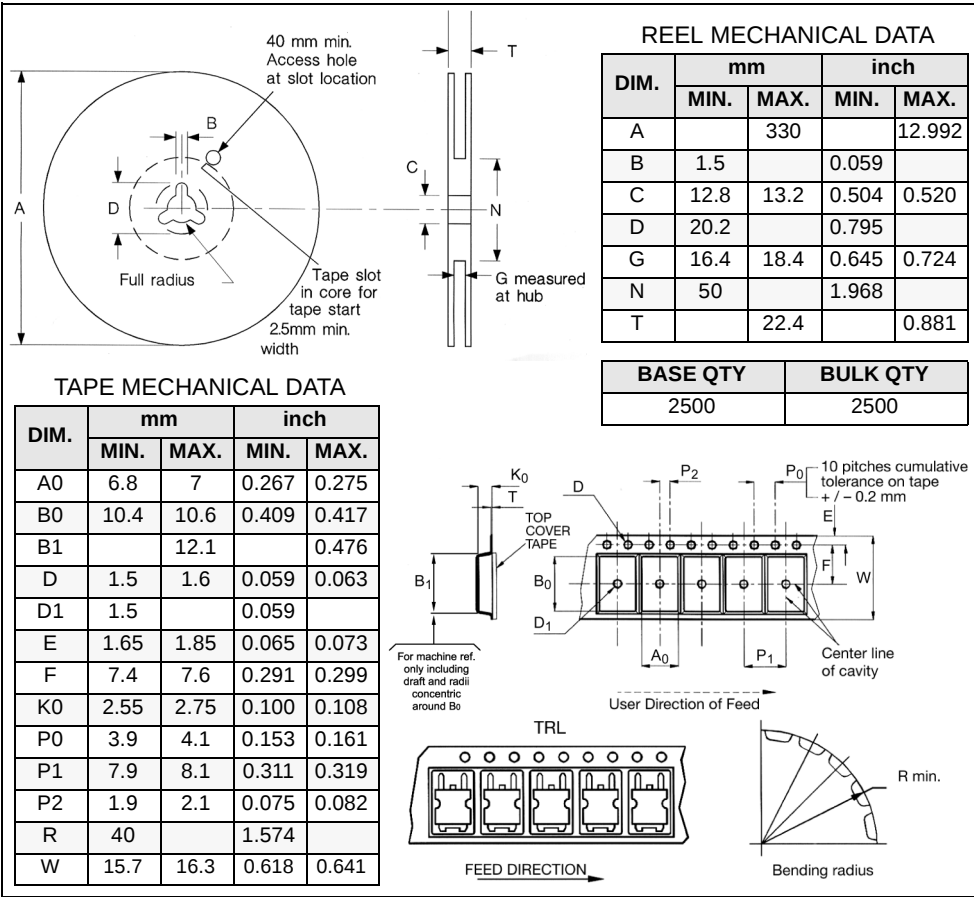
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5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 7. Revision history

Date	Revision	Changes
27-Apr-2006	1	First Release

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