FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-29120-1E

Spread Spectrum Clock Generator

MB88156

■ DESCRIPTION

MB88156 is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. The modulation corresponds to the center spread and down spread. The multiplication ratio can be changed by the pin setting.

Also, the pin can be set whether the modulation is changed. For no modulation, it has the center-non-spread to fix to the output frequency conforming to the multiplication setting and down-non-spread to fix the output frequency to center frequency of the down spread.

■ FEATURES

- Input frequency : 12.5 MHz to 50 MHz (multiplied by 1)
  12.5 MHz to 25 MHz (multiplied by 2)
  12.5 MHz to 20 MHz (multiplied by 4)
- Output frequency : CKOUT 12.5 MHz to 80 MHz
  REFOUT the same as input frequency (not multiplied)

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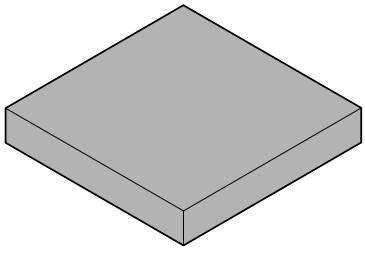
■ PACKAGE

16-pin plastic BCC



(LCC-16P-M09)

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- Modulation rate : ±0.5%, ±1.0% (center spread) , –1.0%, –2.0% (down spread)
- Frequency down function : –0.5%, –1.0% (for down-non-spread)
- Equipped with oscillation circuit : Oscillation range 12.5 MHz to 40 MHz (Fundamental oscillation mode)
  40 MHz to 48 MHz (At 3rd over tone)
- Modulation clock output Duty : 40% to 60%
- Modulation clock Cycle-Cycle Jitter : Multiplied by 1 (input) 12.5 MHz to 20 MHz less than 150 ps
  Multiplied by 1 (input) 20.0 MHz to 50 MHz less than 100 ps
  Multiplied by 2 (input) 12.5 MHz to 25 MHz less than 200 ps
  Multiplied by 4 (input) 12.5 MHz to 20 MHz less than 200 ps
- Low current consumption by CMOS process : 5 mA (24 MHz : Typ-sample, no load)
- Power supply voltage : 3.3 V ± 0.3 V
- Operating temperature : –40 °C to +85 °C
- Package : BCC 16-pin

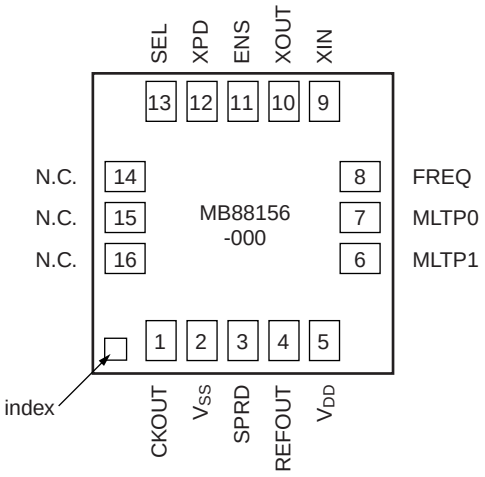
■ PRODUCT LINEUP

Product	Function
MB88156-000	With REFOUT
MB88156-001	Without REFOUT

■ PIN ASSIGNMENT

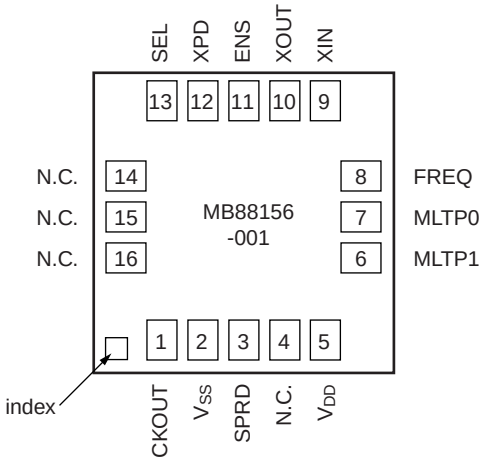
• MB88156-000

TOP VIEW



• MB88156-001

TOP VIEW



LCC-16P-M09

■ PIN DESCRIPTION

Pin no.	Pin name	I/O	Description
1	CKOUT	O	Modulated clock output pin Output “L” at power-down
2	V_{SS}	—	GND pin
3	SPRD	I	Modulation type setting pin/frequency down setting SPRD = “L” : Down spread/down-non-spread SPRD = “H” : Center spread/center-non-spread For details, see “Setting of ENS, SPRD, and SEL”.
4	REFOUT/N.C.	O	Non modulation clock output pin (output “L” at power-down) /non connection pin
5	V_{DD}	—	Power supply voltage pin
6	MLTP1	I	Multiplication rate setting pin For details, see “Setting of MLTP1, MLTP0, and FREQ”.
7	MLTP0	I	
8	FREQ	I	Frequency setting pin For details, see “Setting of MLTP1, MLTP0, and FREQ”.
9	XIN	I	Pin for the connection of resonator/clock input
10	XOUT	O	Connecting pin of resonator
11	ENS	I	Modulation enable setting pin ENS = “L” : Non modulation ENS = “H” : Modulation
12	XPD	I	Power down pin XPD = “L” : Power down XPD = “H” : Normal operation
13	SEL	I	Modulation rate setting pin/frequency falling width setting pin For details, see “Setting of ENS, SPRD, and SEL”.
14	N.C.	—	Non connection pin
15	N.C.	—	Non connection pin
16	N.C.	—	Non connection pin

• Setting of MLTP1, MLTP0, and FREQ (Setting of multiplication rate and input frequency)

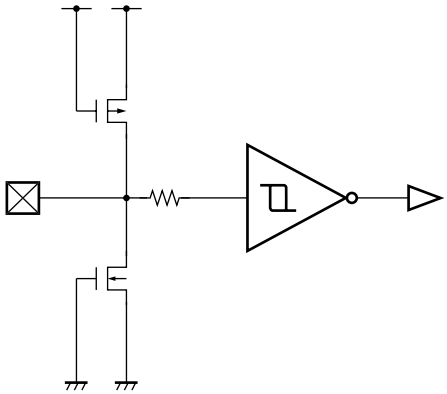
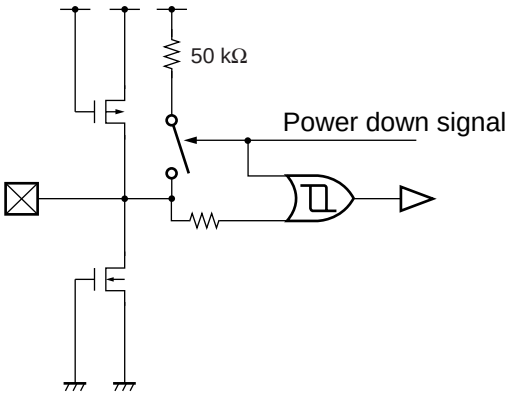
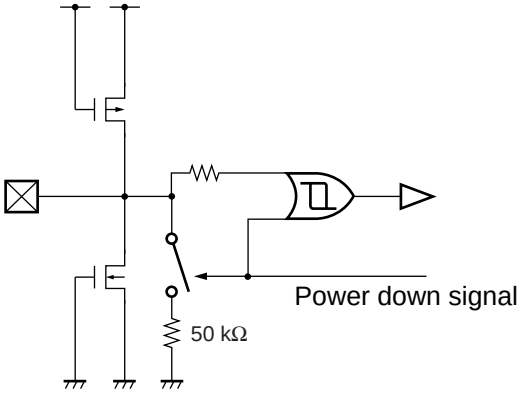
Input frequency	Output frequency	FREQ	Multiplication rate	MLTP1	MLTP0
12.5 MHz to 25 MHz	12.5 MHz to 25.0 MHz	L	Multiplied by 1	L	L
25.0 MHz to 50 MHz	25.0 MHz to 50.0 MHz	H			
12.5 MHz to 25 MHz	25.0 MHz to 50.0 MHz	L	Multiplied by 2	H	L
12.5 MHz to 20 MHz	50.0 MHz to 80.0 MHz	L	Multiplied by 4	H	H

Note : Setting other than above is disabled.

• Setting of ENS, SPRD, and SEL (setting of output frequency)

Setting pin			Output status			
ENS	**SPRD**	**SEL**	**Modulation**	**Modulation type**	**Modulation rate**	**Falling width**
L	L	L	None	Down-non-spread	—	–0.5%
		H			—	–1.0%
	H	L		Center-non-spread	—	0.0%
		H			—	0.0%
H	L	L	Provided	Down spread	–1.0%	—
		H			–2.0%	—
	H	L		Center spread	±0.5%	—
		H			± 1.0%	—

■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
SEL, XPD		• CMOS hysteresis input
ENS, SPRD		• CMOS hysteresis input with pull-up resistor 50 kΩ (Typ) • At power-down, pull-up resistance is shut off.
FREQ, MLTP1, MLTP0		• CMOS hysteresis input with pull-down resistor 50 kΩ (Typ) • At power-down, pull-down resistance is shut off.

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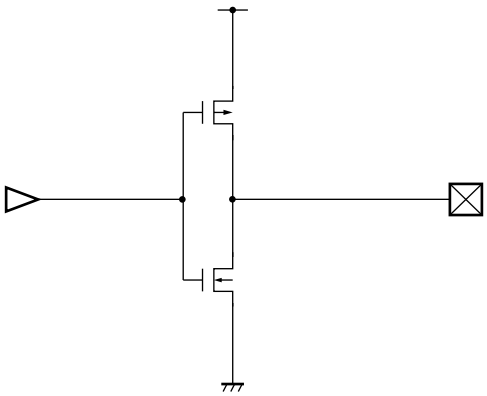
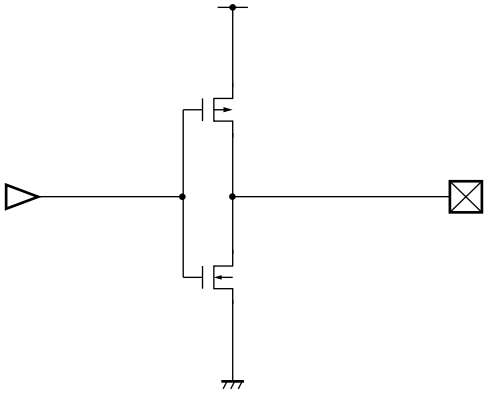
Pin	Circuit type	Remarks
REFOUT		• CMOS output • I_{OL} = 3 mA • Output “L” at power-down
CKOUT		• CMOS output • I_{OL} = 4 mA • Output “L” at power-down

Note : For XIN and XOUT pins, see “■ OSCILLATION CIRCUIT”.

■ HANDLING DEVICES

Preventing Latchup

A latchup can occur if, on this device, (a) a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input or output pin or (b) a voltage higher than the rating is applied between V_{DD} and V_{SS}. The latchup, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

Unused output pin should be opened.

The attention when the external clock is used

Input the clock to XIN pin, and XOUT pin should be opened when you use the external clock.
Please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN pin.

Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between V_{SS} and V_{DD} near the device, as a bypass capacitor.

Oscillation circuit

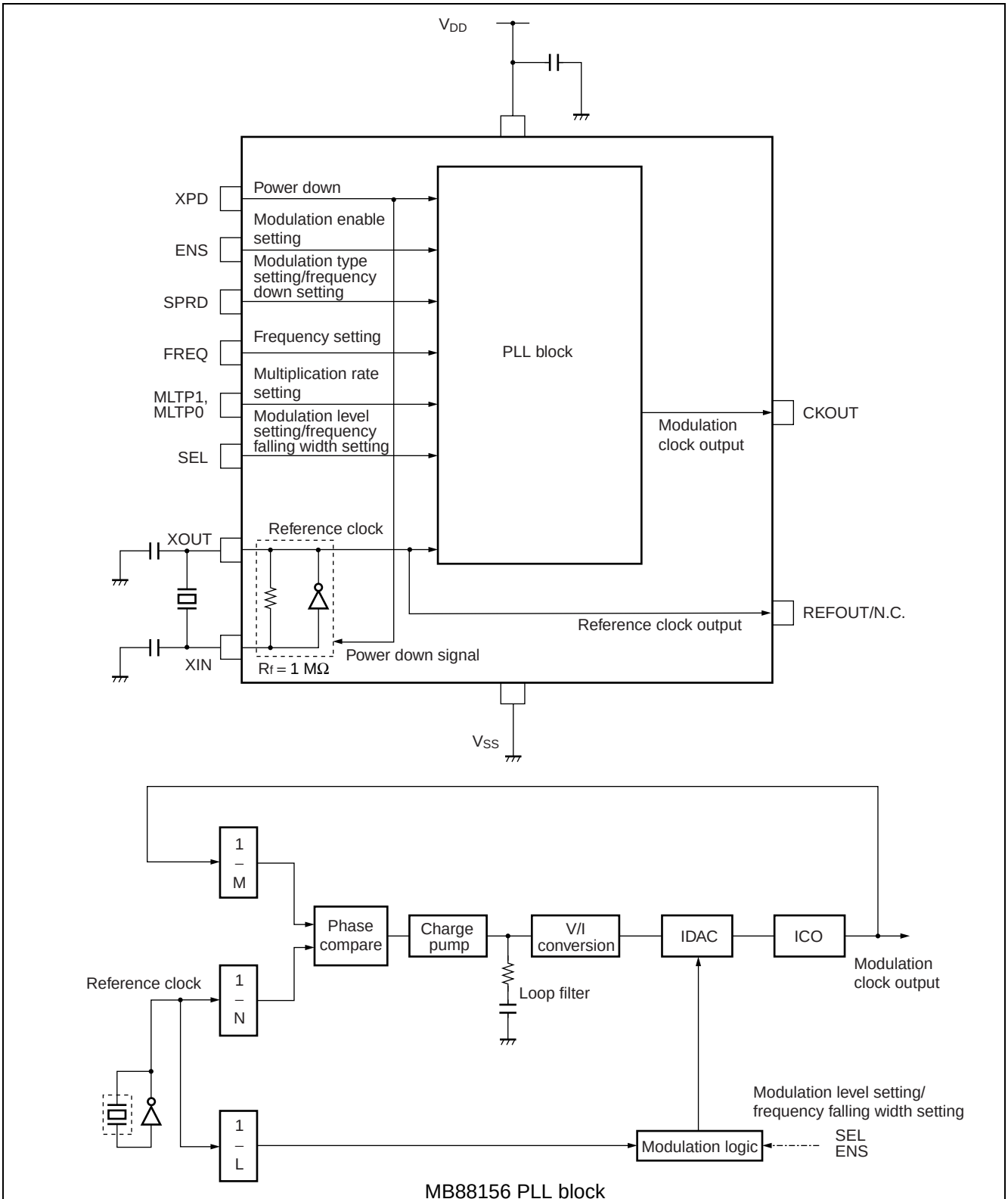
Noise near the XIN and XOUT pins may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN or XOUT pin and the resonator do not intersect other wiring.

Design the printed circuit board that surrounds the XIN and XOUT pins with ground.

Handling N.C. pin

Be sure to open the N.C. pin when it is used.

■ BLOCK DIAGRAM



MB88156 PLL block

A glitchless IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

■ PIN SETTING

After the pin setting is changed, the stabilization wait time of the modulation clock is required. The stabilization wait time of the modulation clock takes the maximum value of Lock-Up time in “AC Characteristics” in ■ ELECTRICAL CHARACTERISTICS.

ENS modulation enable/disable setting

ENS	Modulation
L	No modulation
H	Modulation

Spectrum does not spread when “L” is set to ENS pin.

XPD power down

XPD	Status
L	Power down status
H	Operating status

When setting “L” to XPD pin, it becomes power down mode (low power consumption mode) .
Both of CKOUT and REFOUT for the output pin fixes to “L” output during the power down.

SPRD modulation type setting/frequency down setting

SPRD	Status
L	Down spread/down-non-spread
H	Center spread/center-non-spread

SEL modulation level setting/frequency falling width setting

SEL	Status
L	±0.5 % (at center spread) /±0.0 % (at center-non-spread)
	–1.0 % (at down spread) /–0.5 % (at down-non-spread)
H	±1.0 % (at center spread) /±0.0 % (at center-non-spread)
	–2.0 % (at down spread) /–1.0 % (at down-non-spread)

MLTP1, MLTP0 multiplication rate setting

MLTP1	MLTP0	Multiplication rate
L	L	Multiplied by 1
H	L	Multiplied by 2
H	H	Multiplied by 4

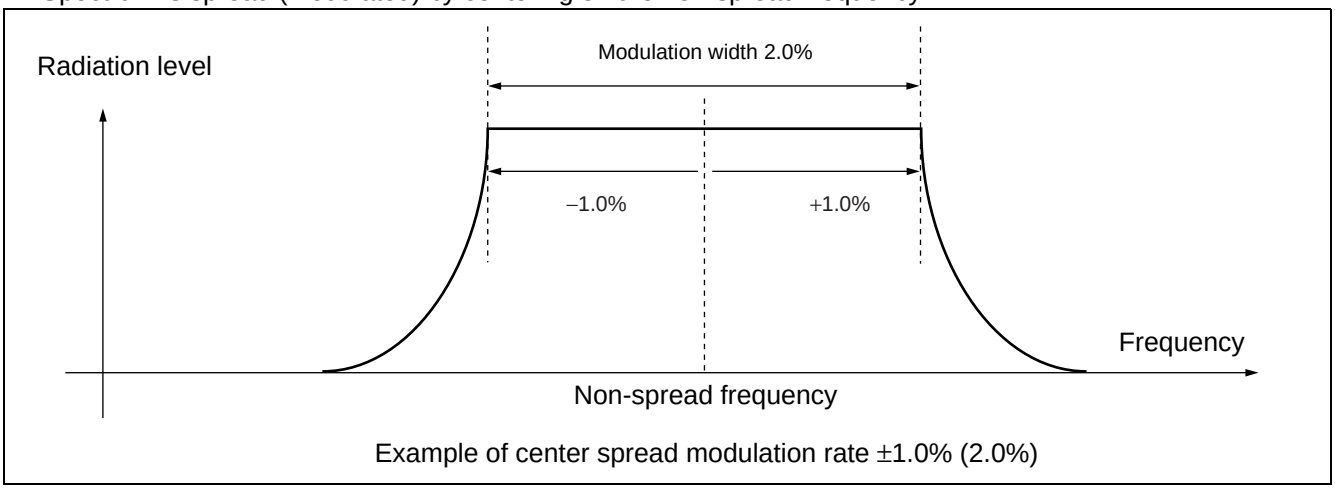
Note : REFOUT is not multiplied.

FREQ frequency setting

FREQ	Input frequency
L	12.5 MHz to 25 MHz (Multiplied by 1, 2) / 12.5 MHz to 20 MHz (Multiplied by 4)
H	25 MHz to 50 MHz (Multiplied by 1)

• Center spread

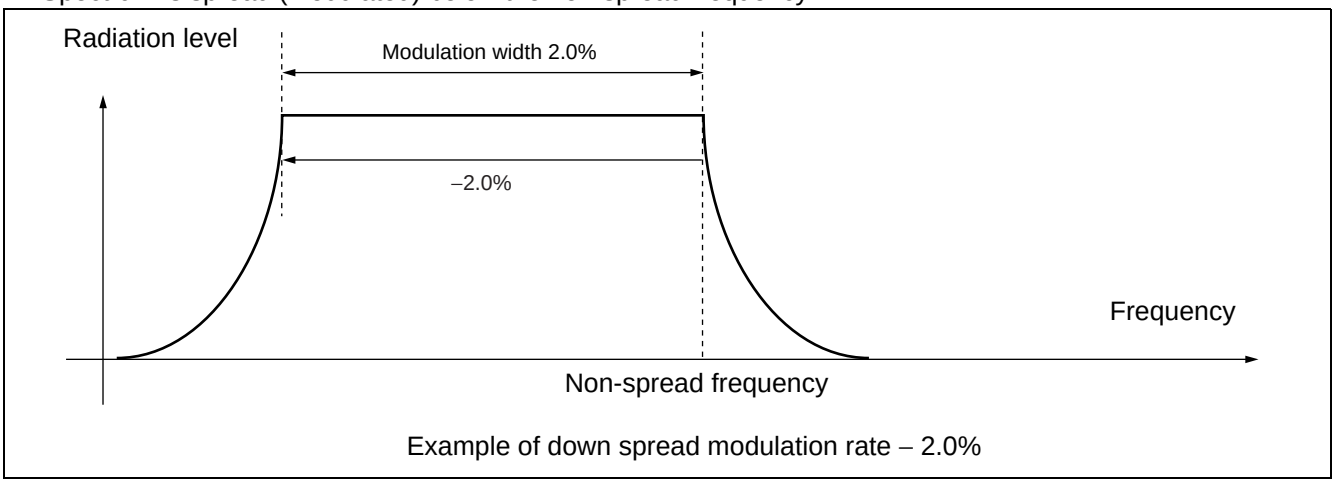
Spectrum is spread (modulated) by centering on the non-spread frequency.



Example of center spread modulation rate ±1.0% (2.0%)

• Down spread

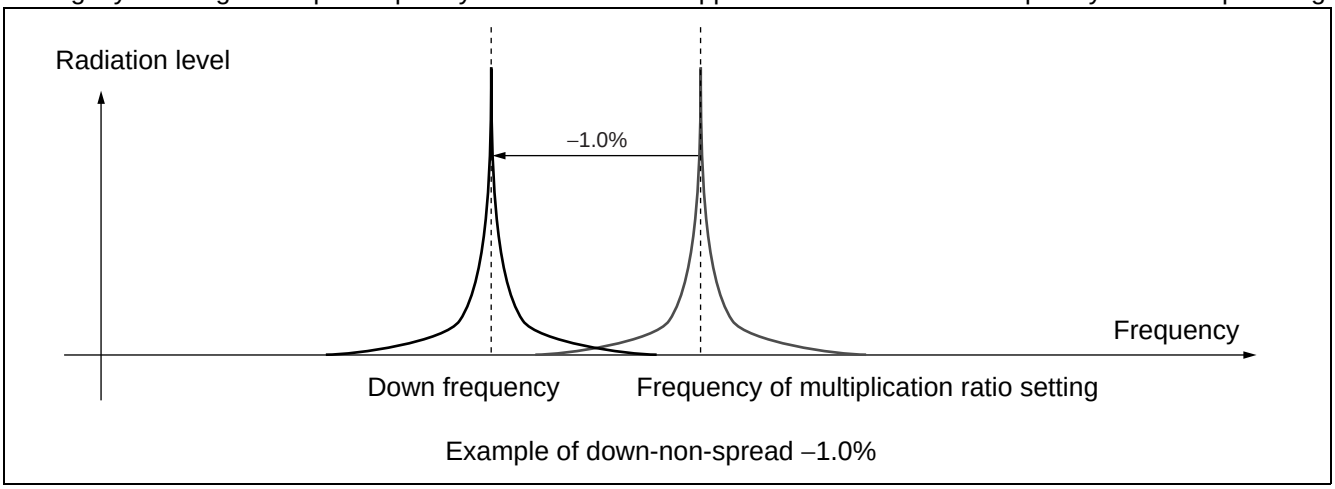
Spectrum is spread (modulated) below the non-spread frequency.



Example of down spread modulation rate – 2.0%

• Down-non-spread

Slightly lowering the output frequency with modulation stopped fixes it to the center frequency for down spreading.



Example of down-non-spread –1.0%

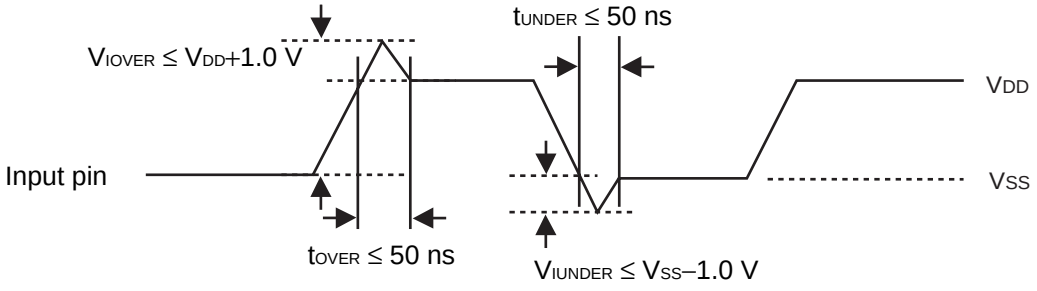
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	– 0.5	+4.0	V
Input voltage*	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	– 55	+125	°C
Operation junction temperature	T_J	– 40	+125	°C
Output current	I_O	– 14	+14	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 (t_{OVER} ≤ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS} – 1.0 (t_{UNDER} ≤ 50 ns)	—	V

*: The parameter is based on V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0.0 V)

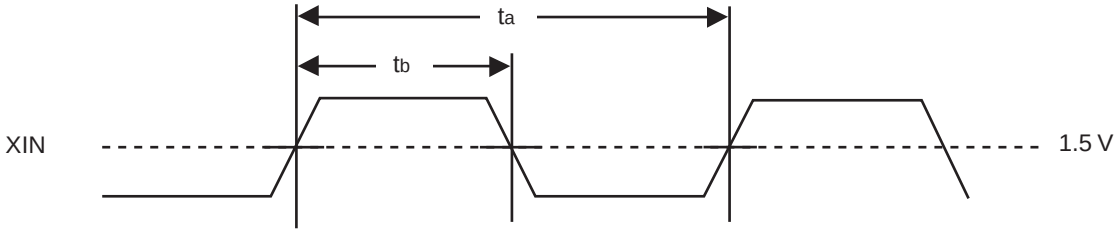
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	—	3.0	3.3	3.6	V
"H" level input voltage	V_{IH}	XIN, SEL, ENS, FREQ, MLTP1, MLTP0, SPRD, XPD	—	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
"L" level input voltage	V_{IL}	XIN, SEL, ENS, FREQ, MLTP1, MLTP0, SPRD, XPD	—	V_{SS}	—	$V_{DD} \times 0.2$	V
Input clock duty cycle	t_{DCI}	XIN	12.5 MHz to 50 MHz	40	50	60	%
Operating temperature	Ta	—	—	−40	—	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b/t_a$)



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

(Ta = − 40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	V_{DD}	24 MHz output No load capacitance	—	5.0	7.0	mA
			At power-down	—	10	—	µA
Output voltage	V_{OHC}	CKOUT	"H" level output I_{OH} = −4 mA	V_{DD} − 0.5	—	V_{DD}	V
	V_{OHR}	REFOUT	"H" level output I_{OH} = −3 mA				
	V_{OLC}	CKOUT	"L" level output I_{OL} = 4 mA	V_{SS}	—	0.4	V
	V_{OLR}	REFOUT	"L" level output I_{OL} = 3 mA				
Output impedance	Z_{OC}	CKOUT	12.5 MHz to 80 MHz	—	45	—	Ω
	Z_{OR}	REFOUT	12.5 MHz to 50 MHz	—	70	—	
Input capacitance	C_{IN}	SEL, ENS, FREQ, MLTP1, MLTP0, SPRD, XPD	Ta = +25 °C V_{DD} = V_I = 0.0 V f = 1 MHz	—	—	16	pF
Pull-up resistor	R_{PU}	ENS, SPRD	—	25	50	200	kΩ
Pull-down resistor	R_{PD}	FREQ, MLTP1, MLTP0	—	25	50	200	kΩ
Load capacitance	C_L	REFOUT	12.5 MHz to 50 MHz	—	—	15	pF
		CKOUT	12.5 MHz to 50 MHz	—	—	15	
			50 MHz to 80 MHz	—	—	7	

• AC Characteristics

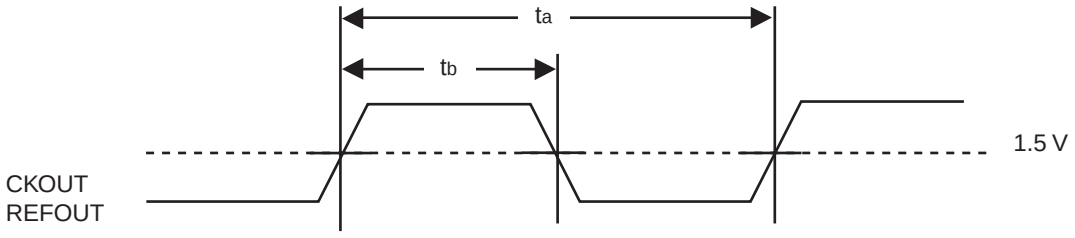
(Ta = − 40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Sym-bol	Pin	Conditions		Value			Unit
					Min	Typ	Max	
Oscillation frequency	f_x	XIN, XOUT	Fundamental oscillation		12.5	—	40	MHz
			3rd overtone		40	—	48	
Input frequency	f_{in}	XIN	FREQ = 0	Multiplied by 1	12.5	—	25	MHz
				Multiplied by 2	12.5	—	25	
				Multiplied by 4	12.5	—	20	
			FREQ = 1	Multiplied by 1	25	—	50	
Output frequency	f_{OUT}	REFOUT	FREQ = 0	Multiplied by 1	12.5	—	25	MHz
				Multiplied by 2	12.5	—	25	
				Multiplied by 4	12.5	—	20	
			FREQ = 1	Multiplied by 1	25	—	50	
		CKOUT	FREQ = 0	Multiplied by 1	12.5	—	25	
				Multiplied by 2	25	—	50	
				Multiplied by 4	50	—	80	
			FREQ = 1	Multiplied by 1	25	—	50	
Output slew rate	SR_C	CKOUT	Load capacitance 15 pF 0.4 to 2.4 V		0.4	—	4.0	V/ns
	SR_R	REFOUT	Load capacitance 15pF 0.4 to 2.4 V		0.3	—	2.0	
Output clock Duty Cycle	t_{DCC}	CKOUT	1.5 V reference level		40	—	60	%
	t_{DCR}	REFOUT	1.5 V reference level		t_{DCI} − 10*1	—	t_{DCI} + 10*1	
Modulation frequency	f_{MOD}	CKOUT	Input frequency at 24 MHz		—	32.4	—	kHz
Lock-Up time*2	t_{LK}	CKOUT	—		—	2	5	ms
Cycle-cycle jitter	t_{JC}	CKOUT	Multiplied by 1 No load capacitance Standard deviation σ	Input frequency 12.5 MHz to 20 MHz	—	—	150	ps
				Input frequency 20 MHz to 50 MHz	—	—	100	
			Multiplied by 2 No load capacitance Standard deviation σ	Input frequency 12.5 MHz to 25 MHz	—	—	200	
			Multiplied by 4 No load capacitance Standard deviation σ	Input frequency 12.5 MHz to 20 MHz	—	—	200	

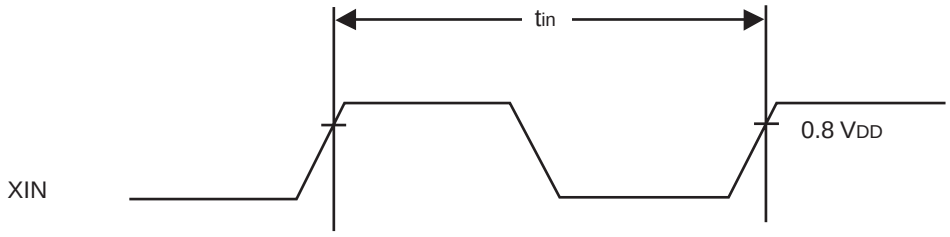
*1 : Because the duty of REFOUT pin output depends on t_{DCI} of the input clock duty, it is assured only when either A or B condition is used as follow:
A : Resonator input : When the resonator is connected to the XIN pin and XOUT pin and oscillates normally.
B : External clock input : The input level is full swing (V_{SS} – V_{DD}) .

*2 : After power on and release of power down or changing the pin setting (SEL, ENS, FREQ, MLTP1 and MLTP0, and SPRD) , the stabilization wait time of the modulation clock is required. The stabilization wait time of the modulation clock takes the maximum value of Lock-Up time.

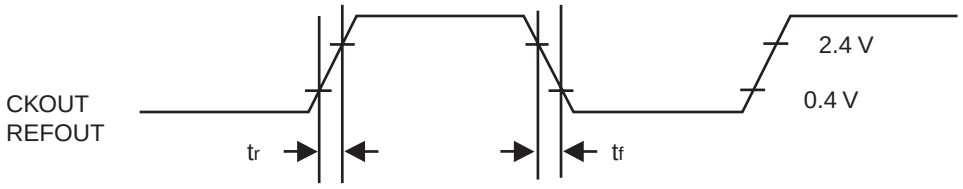
■ OUTPUT CLOCK Duty Cycle (t_{DCC}, $t_{DCR} = t_b/t_a$)



■ INPUT FREQUENCY ($f_{in} = 1/t_{in}$)

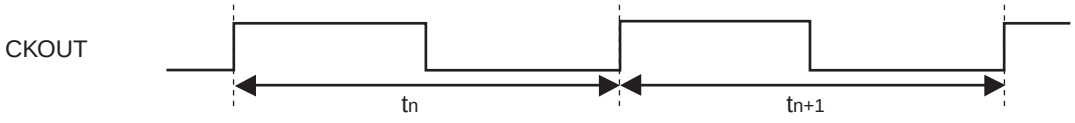


■ OUTPUT SLEW RATE (SR_C, SR_R)



Note : $SR_C = (2.4–0.4)/t_r$, $SR_C = (2.4–0.4)/t_f$
$SR_R = (2.4–0.4)/t_r$, $SR_R = (2.4–0.4)/t_f$

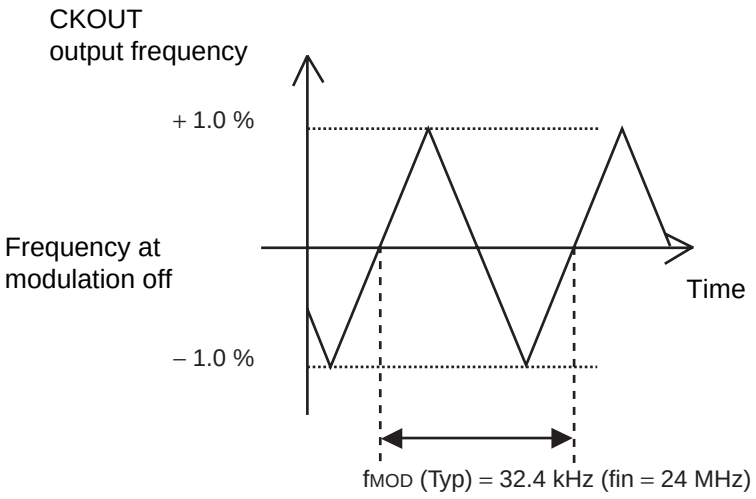
■ CYCLE-CYCLE JITTER ($t_{JC} = |t_n - t_{n+1}|$)



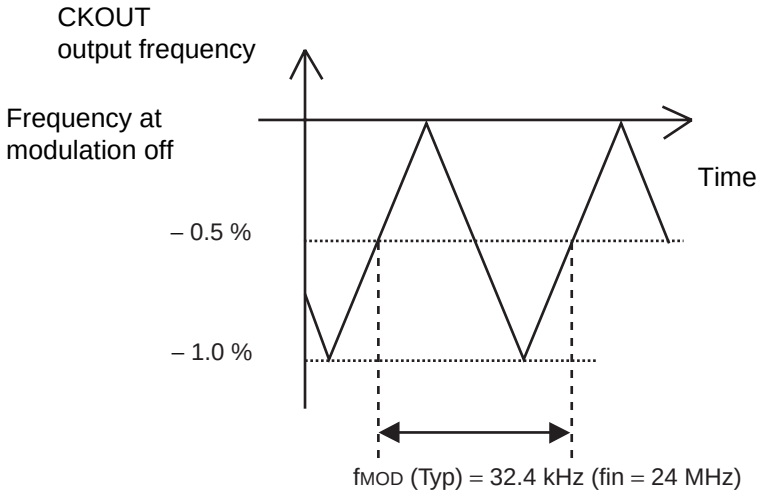
Note : Cycle-cycle jitter indicates the difference between a certain cycle and the immediately succeeding (or preceding) cycle.

■ MODULATION WAVEFORM

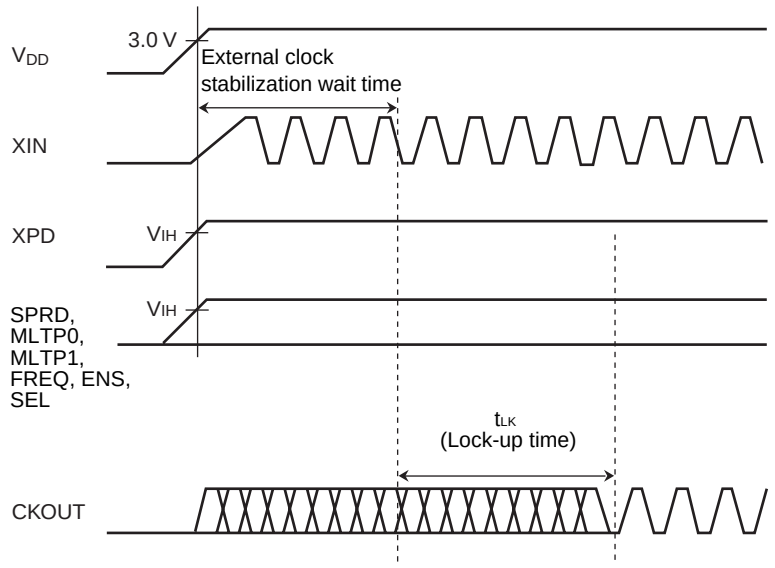
• Modulation rate ±1.0%, example of center spread



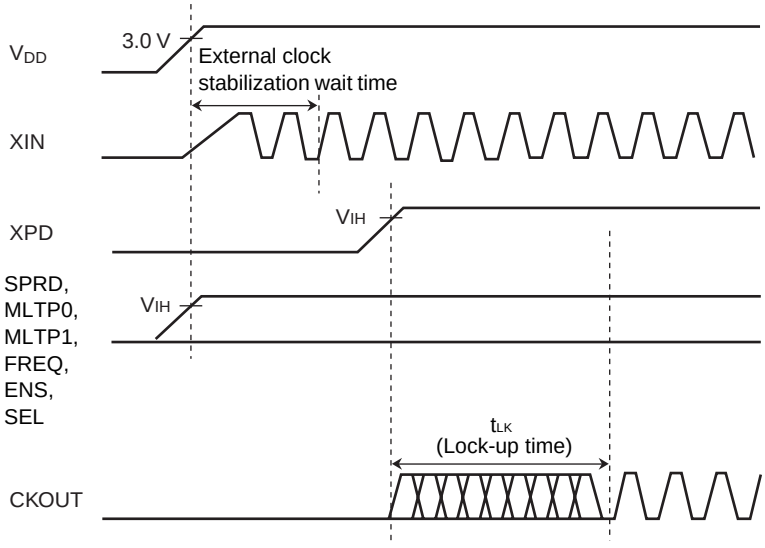
• Modulation rate –1.0%, example of down spread



■ LOCK-UP TIME



If the XPD pin is fixed at the “H” level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to XIN pin) + (the lock-up time “t_{LK}”). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.



If the XPD pin is used for power-down control, the set clock signal is output from the CKOUT pin at most the lock-up time “t_{LK}” after the XPD pin goes “H” level.

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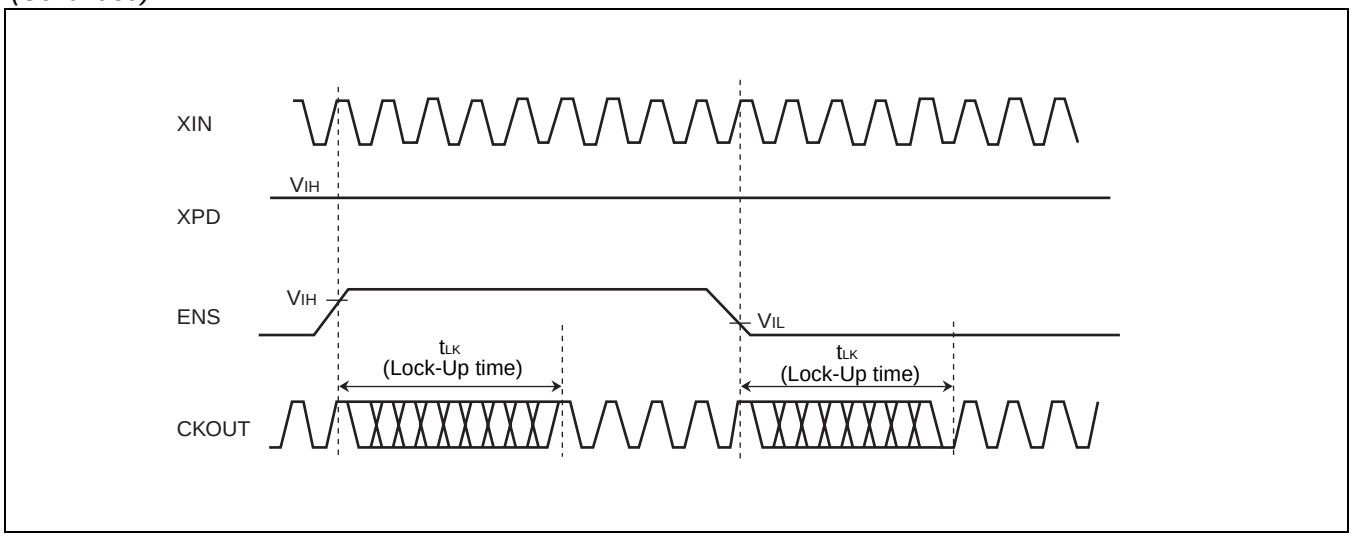


If the ENS pin is used for modulation enable control during normal operation, the set clock signal is output from the CKOUT pin at most the lock-up time "t_{LK}" after the level at the ENS pin is determined.

Note : The wait time for the clock signal output from the CKOUT pin to become stable is required after the IC is released from power-down mode by the XPD pin or after another pin's setting is changed. During the period until the output clock signal becomes stable, neither of the output frequency, output clock duty cycle, modulation period, and cycle-cycle jitter characteristic cannot be guaranteed. It is therefore advisable to take action, such as cancelling a device reset at the stage after the lock-up time has passed.

■ OSCILLATION CIRCUIT

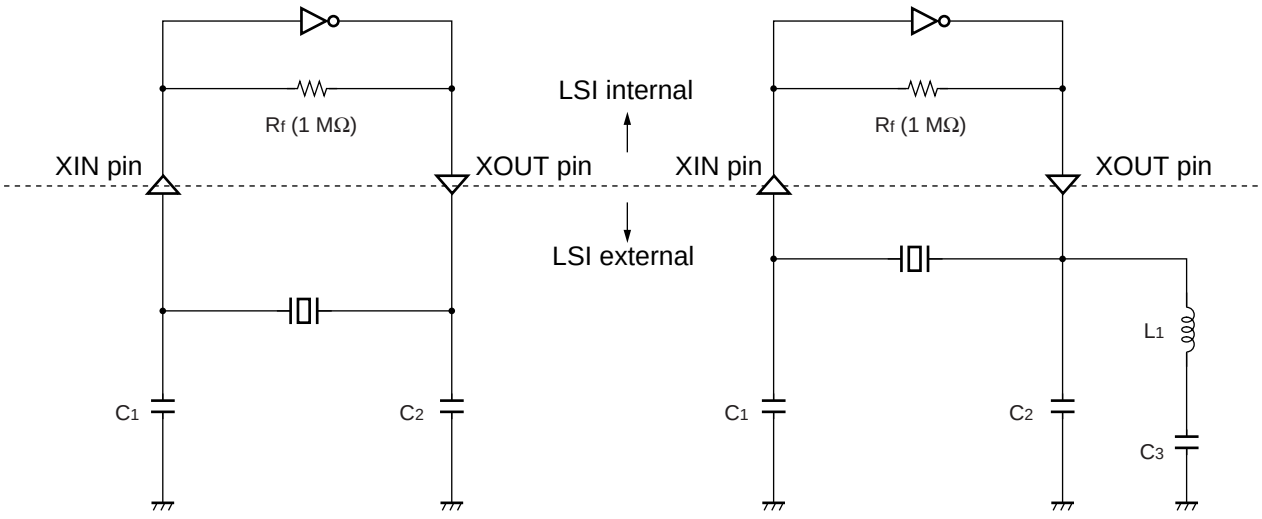
The following schematic on the left-hand side shows a sample connection of a general resonator. The oscillation circuit contains a feedback resistor (1 MΩ) . The values of capacitors (C_1 and C_2) must be adjusted to the optimum constant of the resonator used.

The following schematic on the right-hand side shows a sample connection of a 3rd overtone resonator. The values of capacitors (C_1, C_2, and C_3) and inductor (L_1) must be adjusted to the optimum constant of the resonator used.

The most suitable value is different by individual resonator. Please refer to the resonator manufacturer which you use for the most suitable value.

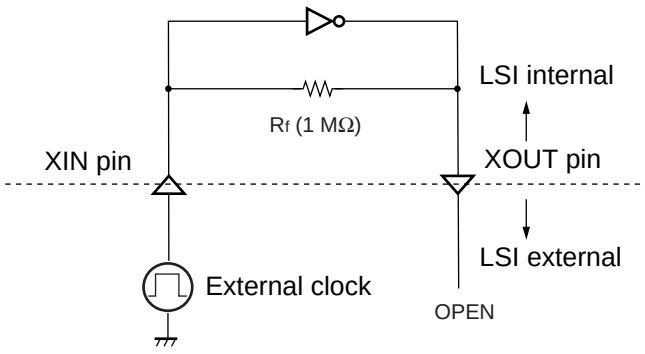
To use an external clock signal (without using the resonator) , input the clock signal to the XIN pin with the XOUT pin connected to nothing .

• When using the resonator



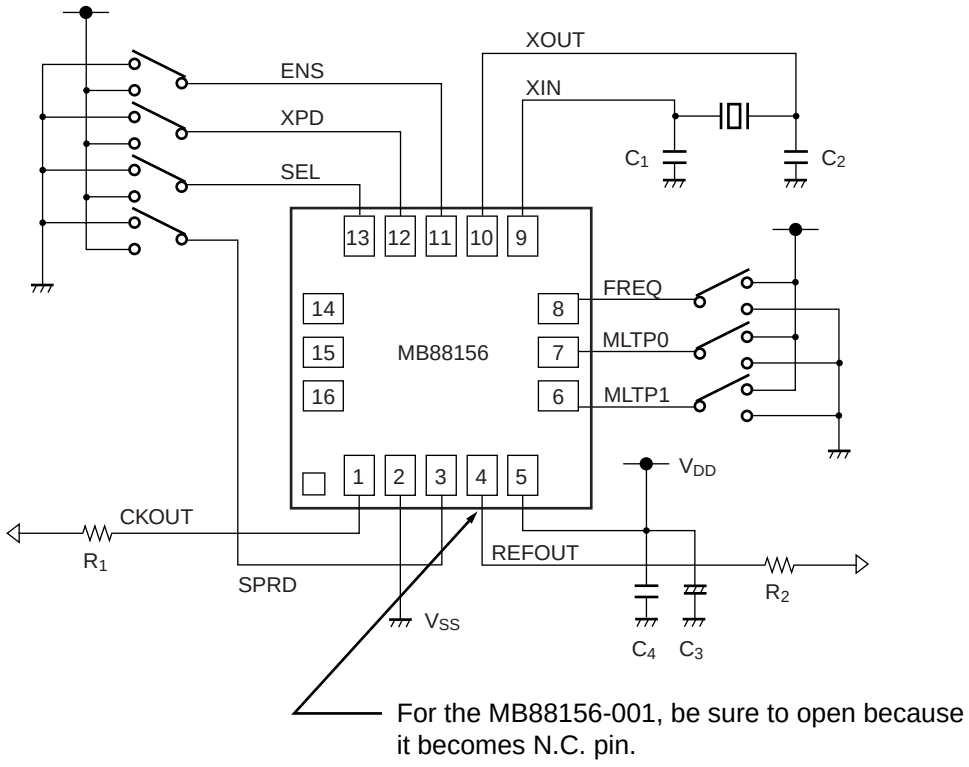
Fundamental resonator　　3rd overtone resonator

• When using the external clock



Note : Note that the jitter characteristic of the input clock signal may affect the cycle-cycle jitter characteristic.

■ INTERCONNECTION CIRCUIT EXAMPLE



C_1, C_2 : Oscillation stabilization capacitance (see ■ OSCILLATION CIRCUIT)

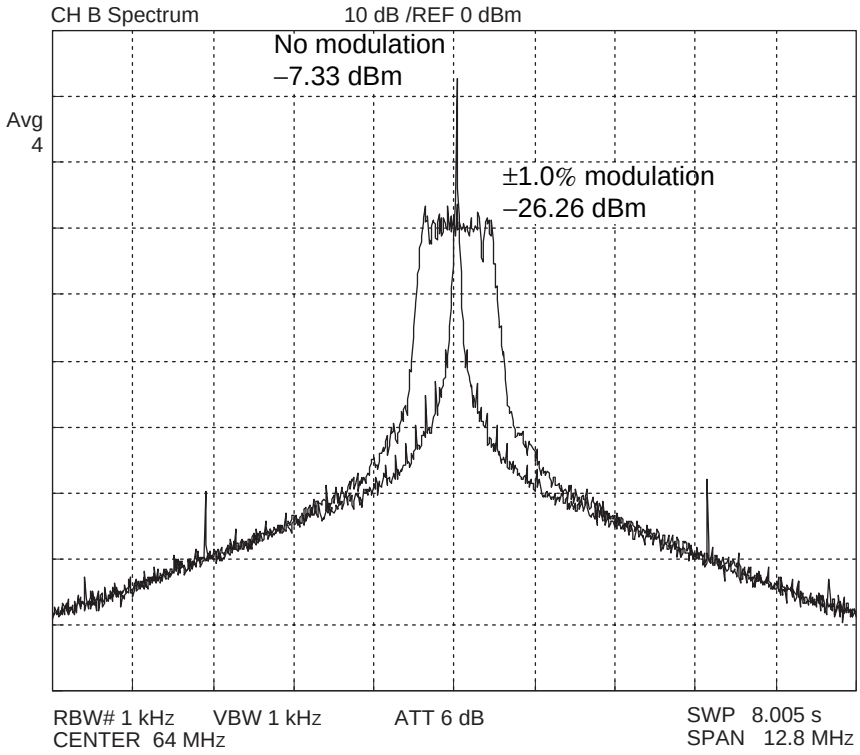
C_3 : Capacitor of 10 μF or higher

C_4 : Capacitor of about 0.01 μF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)

R_1, R_2 : Impedance matching resistor for board pattern

■ SPECTRUM EXAMPLE CHARACTERISTICS

The condition of the examples of the characteristic is shown as follows : Input frequency = 16 MHz (Output frequency = 64 MHz : Using MB88156-001 (Multiplied by 4))
Power-supply voltage = 3.3 V, None load capacity. Modulation rate = ± 1.0% (center spread).
Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with RBW = 1 kHz (ATT use for −6 dB) .

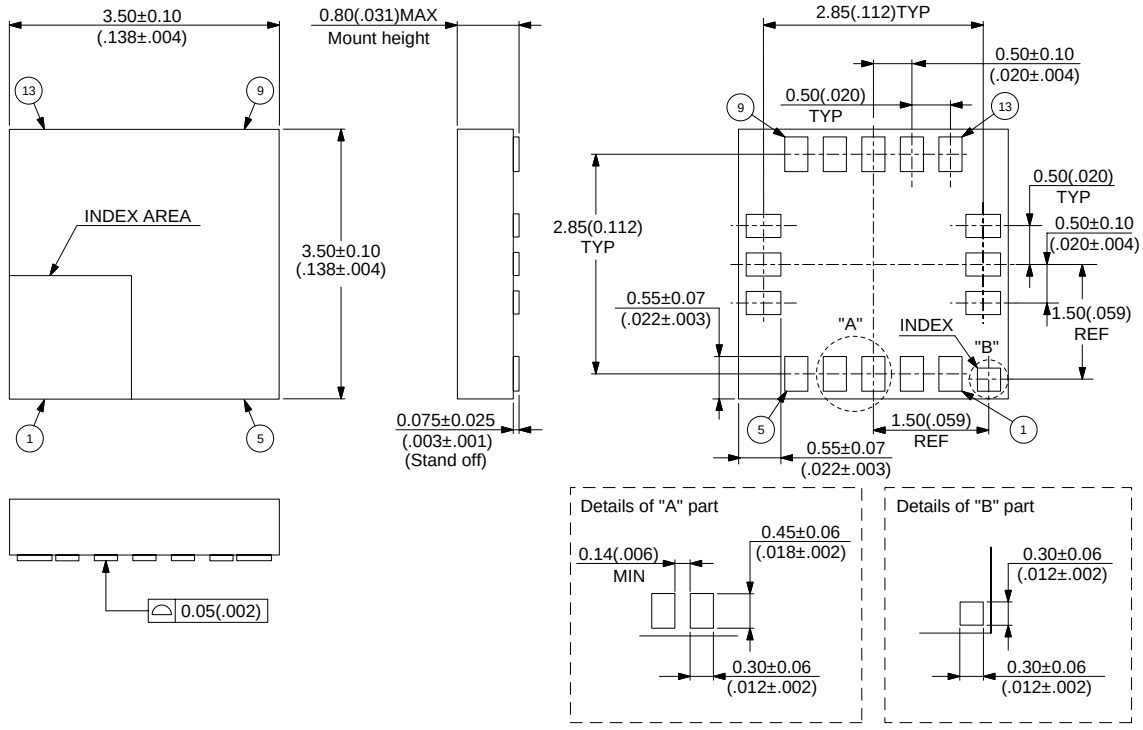


■ ORDERING INFORMATION

Part number	REFOUT pin	Package	Emboss taping
MB88156PV-G-000-EFE1	Provided	16-pin plastic BCC (LCC-16P-M09)	EF type
MB88156PV-G-000-ERE1			ER type
MB88156PV-G-001-EFE1	None		EF type
MB88156PV-G-001-ERE1			ER type

■ PACKAGE DIMENSION

16-pin plastic BCC
(LCC-16P-M09)



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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