1Mb x 16 Pseudo Static RAM

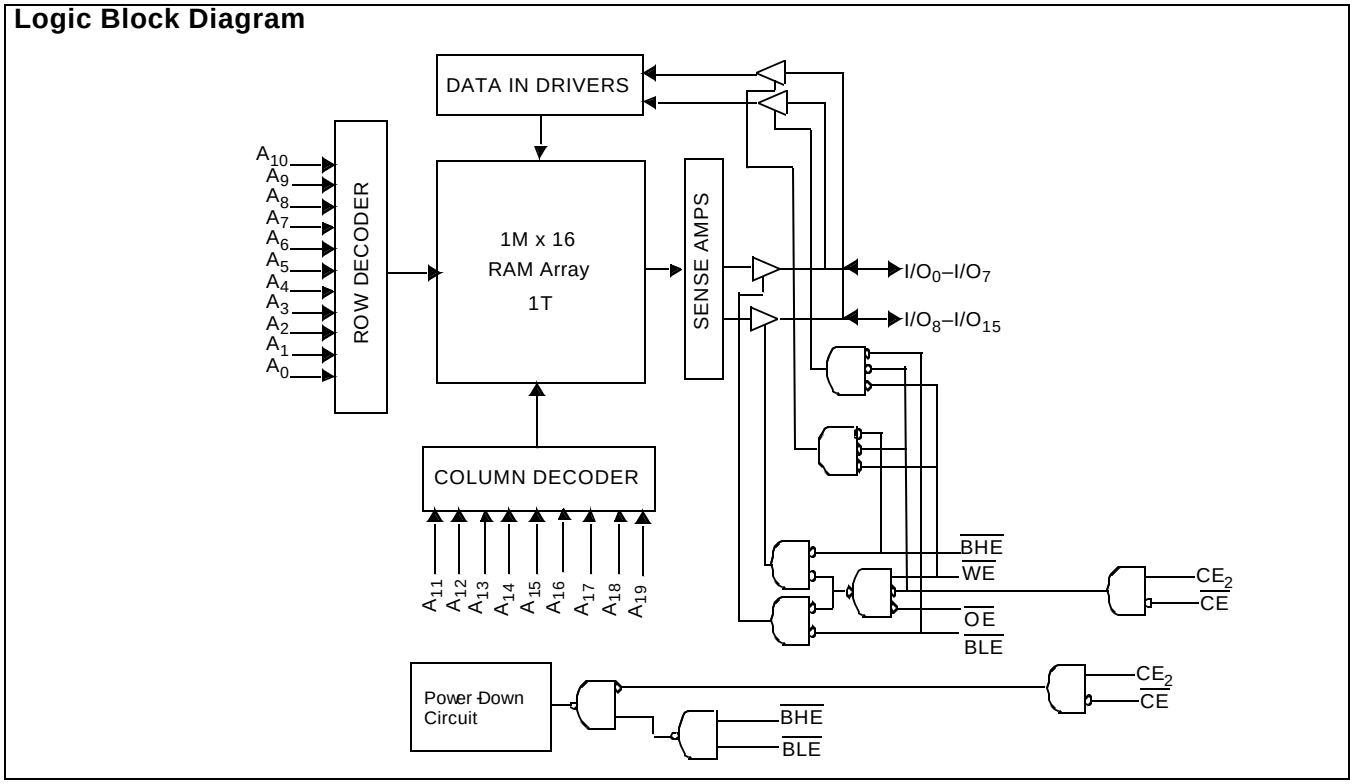
Features

- 1T Cell, PSRAM Architecture
- High speed: 70 ns
- Wide Voltage range:
  - **— V_{CC} range: 2.7V to 3.3V**
- Low active power
  - **— Typical active current: 2 mA @ f = 1 MHz**
  - **— Typical active current: 13 mA @ f = f_{MAX}**
- Low standby power
- Automatic power-down when deselected

Functional Description[1]

The WCMC1616V9X is a high-performance CMOS pseudo static RAMs (PSRAM) organized as 1M words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device can be put into standby mode reducing power consumption by more than 99% when deselected using $\overline{CE}$ LOW, CE_2 HIGH or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH. The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH, CE_2 LOW $\overline{OE}$ is deasserted HIGH), or during a write operation (Chip Enabled and Write Enable $\overline{WE}$ LOW). The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling even when the chip is selected (Chip Enable $\overline{CE}$ LOW, CE_2 HIGH and both $\overline{BHE}$ and $\overline{BLE}$ are LOW). Reading from the device is accomplished by asserting the Chip Enables ($\overline{CE}$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the Truth Table for a complete description of read and write modes.

Logic Block Diagram



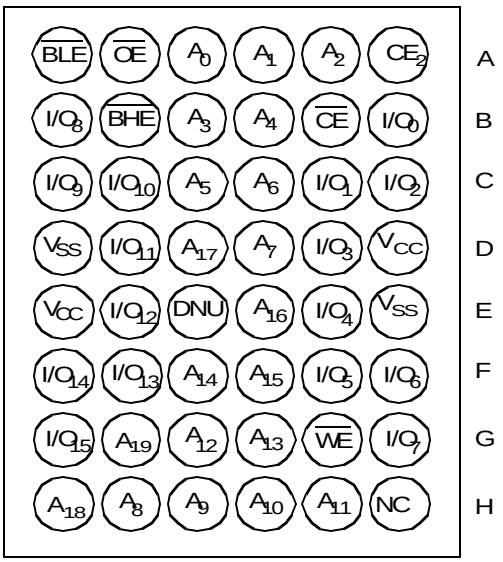
Note:

1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration[2, 3, 4]

FBGA

Top View



Note:

2. DNU pins are to be left floating or tied to Vss.
3. Ball H6 is the address expansion pin for the 32Mb density.
4. NC “no connect” - not connected internally to the die.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied .....–40°C to +85°C

Supply Voltage to Ground Potential ..... –0.4V to 4.6V

DC Voltage Applied to Outputs in High-Z State[5, 6, 7] ....–0.4V to 3.3V

DC Input Voltage[5, 6, 7] ....–0.4V to 3.3V

Output Current into Outputs (LOW).....20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current .....> 200 mA

Operating Range[9]

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–25°C to +85°C	2.7V to 3.3V

Product Portfolio

Product	V_{CC} Range(V)			Speed (ns)	Power Dissipation					
					Operating, Icc (mA)				Standby, I_{SB2} (mA)	
					f = 1 MHz		f = f_{MAX}			
	Min.	Typ.	Max.		Typ.[8]	Max.	Typ.[8]	Max.	Typ.[8]	Max.
WCMC1616V9X-FI70	2.7	3.0	3.3	70	2	3.5	13	17	80	150

Notes:

5. $V_{IH(MAX)} = V_{CC} + 0.5V$ for pulse durations less than 20ns.
6. $V_{IL(MIN)} = -0.5V$ for pulse durations less than 20ns.
7. Overshoot and undershoot specifications are characterized and are not 100% tested.
8. Typical values are included for reference only and are not guranteed or tested. Typical values are measured at $V_{CC} = V_{CC}$ (typ) and $T_A = 25C$
9. Vcc must be at minimal operational levels before inputs are turned ON.

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		WCMC1616V9X-70 Min.	Typ.[8]	Max.	Unit
Vcc	Supply Voltage			2.7		3.3	V
V_{OH}	Output HIGH Voltage	I_{OH} = –1 mA		V_{CC} - 0.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA				0.4	V
V_{IH}	Input HIGH Voltage			0.8*V_{CC}		V_{CC} + 0.4	V
V_{IL}	Input LOW Voltage	F = 0		–0.4		0.4	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ Vcc		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ Vcc, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	Vcc = 3.3V, I_{OUT} = 0mA, CMOS level		13	17	mA
		f = 1 MHz			2	3.5	
I_{SB1}	Automatic CE Power-down Current – CMOS Inputs	CE ≥ V_{CCQ} – 0.2V, CE_2 ≤ 0.2V V_{IN} ≥ V_{CCQ} – 0.2V, V_{IN} ≤ 0.2V, f = f_{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)			100	525	µA
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	CE ≥ V_{CCQ} – 0.2V, CE_2 ≤ 0.2V V_{IN} ≥ V_{CCQ} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} =3.3V			80	150	µA

Capacitance [10]

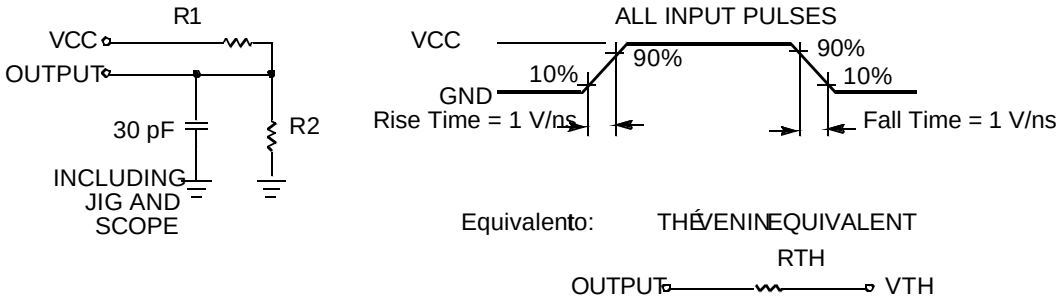
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = $V_{CC(typ)}$	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance[10]

Parameter	Description	Test Conditions	FBGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		17	°C/W

Note:
10. Tested initially and after design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Parameters	3.0V Vcc	Unit
R1	1179	W
R2	1941	W
R_{TH}	733	W
V_{TH}	1.87	V

Switching Characteristics (Over the Operating Range)[11]

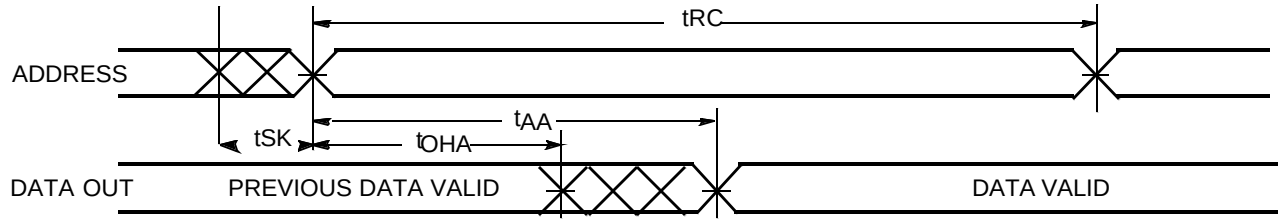
Parameter	Description	WCMC1616V9X-70		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	CE LOW and CE_2 HIGH to Data Valid		70	ns
t_{DOE}	OE LOW to Data Valid		35	ns
t_{LZOE}	OE LOW to Low Z[12, 14]	5		ns
t_{HZOE}	OE HIGH to High Z[12, 14]		25	ns
t_{LZCE}	CE LOW and CE_2 HIGH to Low Z[12, 14]	5		ns
t_{HZCE}	CE HIGH and CE_2 LOW to High Z[12, 14]		25	ns
t_{DBE}	BLE/BHE LOW to Data Valid		70	ns
t_{LZBE}	BLE/BHE LOW to Low Z[12, 14]	5		ns
t_{HZBE}	BLE/BHE HIGH to High-Z[12, 14]		25	ns
t_{SK}	Address Skew		10	ns
Write Cycle[13]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	CE LOW and CE_2 HIGH to Write End	55		ns
t_{AW}	Address Set-up to Write End	55		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	WE Pulse Width	55		ns
t_{BW}	BLE/BHE LOW to Write End	55		ns
t_{SD}	Data Set-up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	WE LOW to High Z[12, 14]		25	ns
t_{LZWE}	WE HIGH to Low Z[12, 14]	5		ns

Notes:

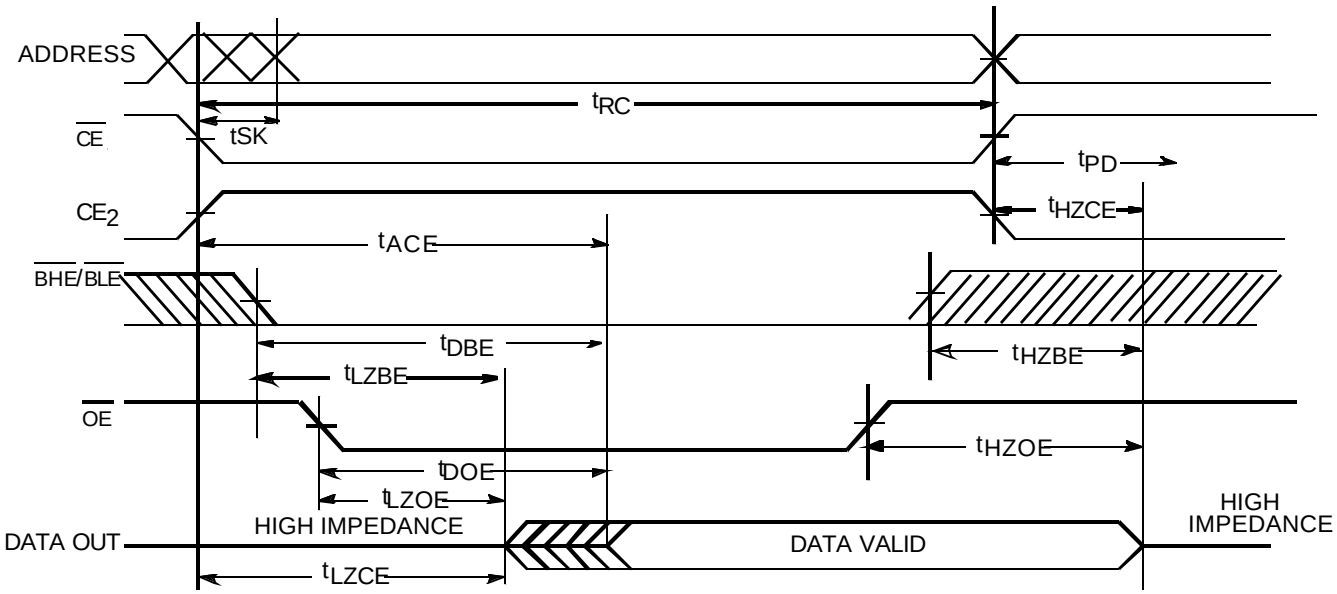
11. Test conditions assume signal transition time of 1V/ns or higher , timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0V to $V_{CC(typ),}$ and output loading of the specified I_{OL}/I_{OH} and 30-pF load cpacitance
12. t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
13. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write
14. High-Z and Low-Z parameters are characterized and are not 100% tested.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled) [15]

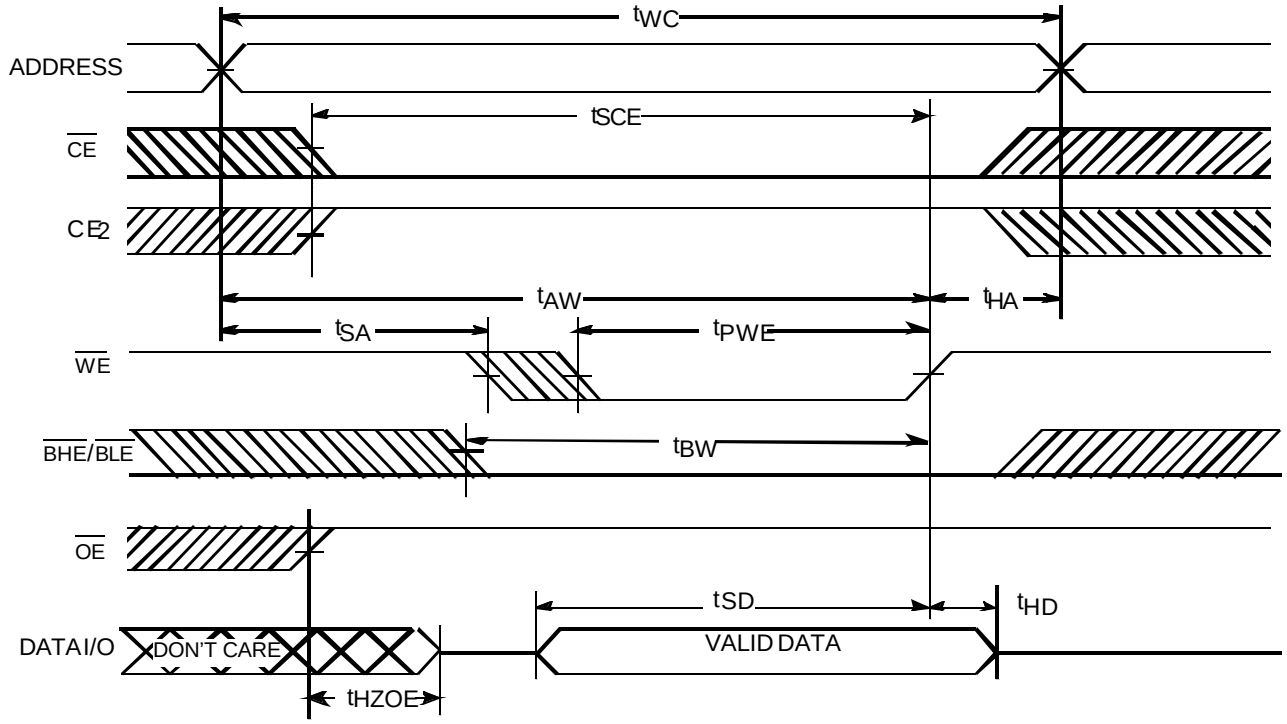


Read Cycle No. 2 ($\overline{OE}$ Controlled)[15]

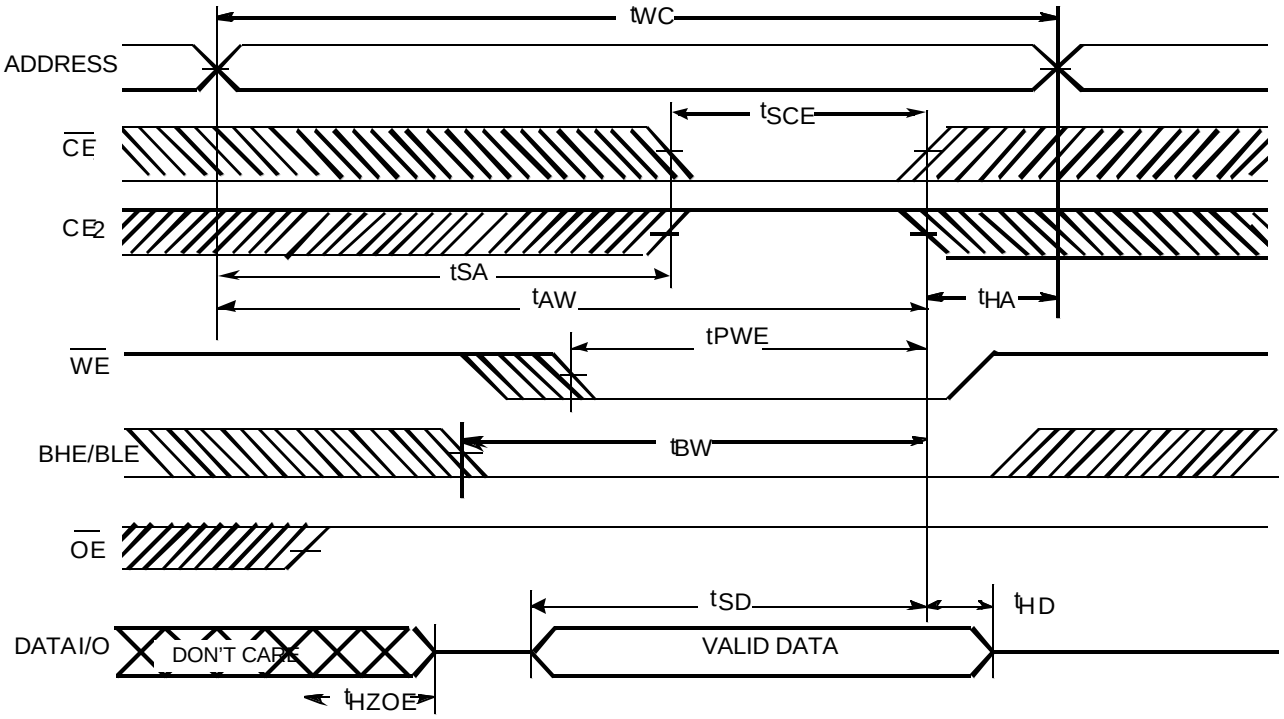


Note:
15. $\overline{WE}$ is HIGH for Read Cycle.

Write Cycle No. 1(WE Controlled)[13, 14, 16, 17, 18,]

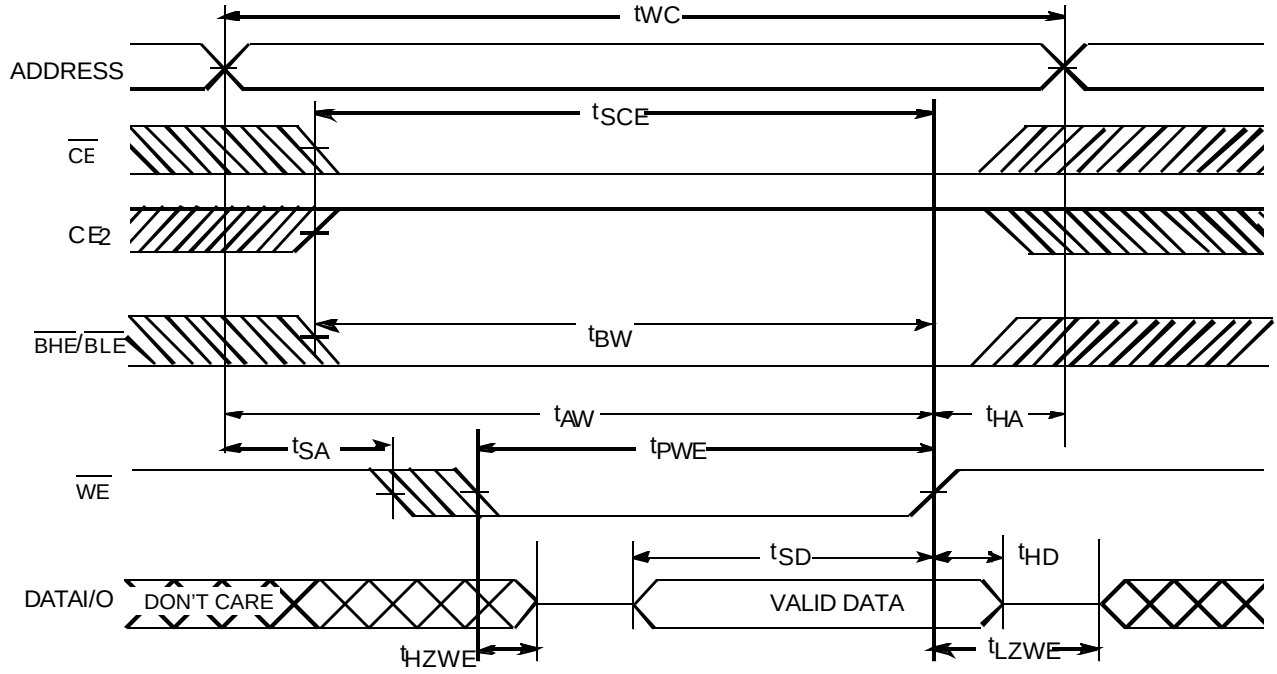


Write Cycle No. 2 (CE Controlled)[13, 14, 16, 17, 18]

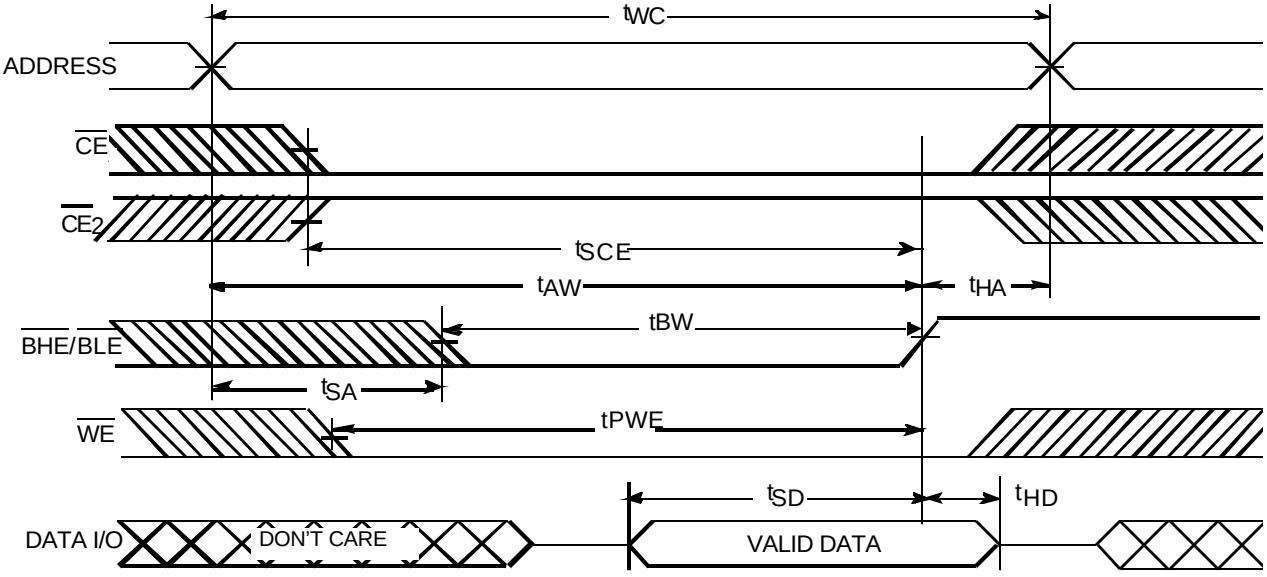


Notes:
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
17. If Chip Enable goes INACTIVE simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[17, 18]



Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[17, 18]



Truth Table[19]

$\overline{CE}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	H	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	L	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write (Upper Byte and Lower Byte)	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write (Lower Byte Only)	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0 –I/O_7 in High Z	Write (Upper Byte Only)	Active (I_{CC})

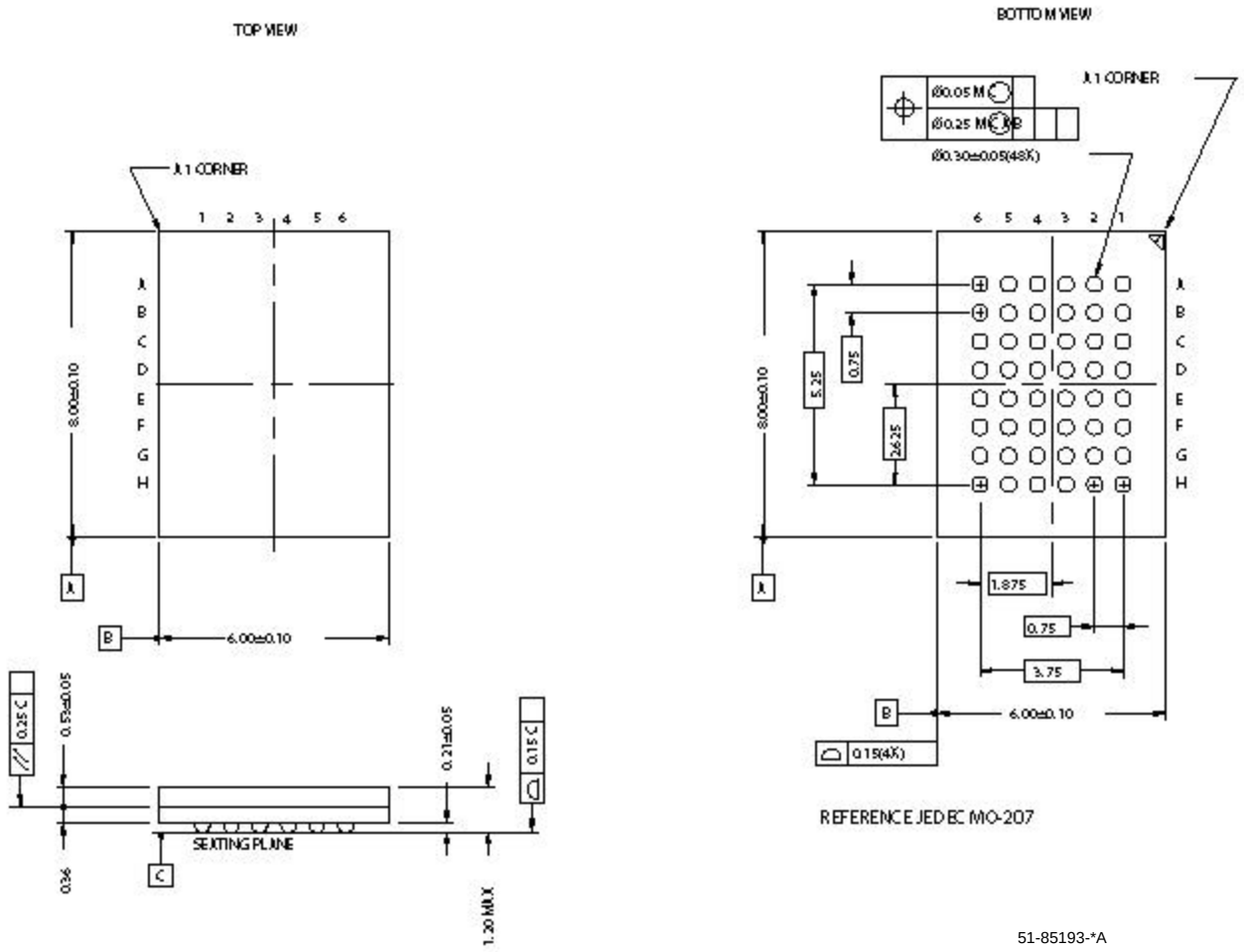
Notes:
19. H = V_{IH}, L = V_{IL}, X = Don't Care

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMC1616V9X-FI70	BV48A	48-ball Fine Pitch BGA (6.0 x 8.0 x 1.2 mm)	Industrial

Package Diagrams

48-Ball (6 mm x 8 mm x 1.2 mm) FBGA BA48K



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Document History Table

Document Title: WCMC1616V9X MoBL3™® 16Mb (1Mb x 16) Pseudo Static RAM Document Number: 38-14027				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	130544	10/16/03	MPR	New Data Sheet