Step Down Converter with Bypass Mode for Ultra Low Power Wireless Applications

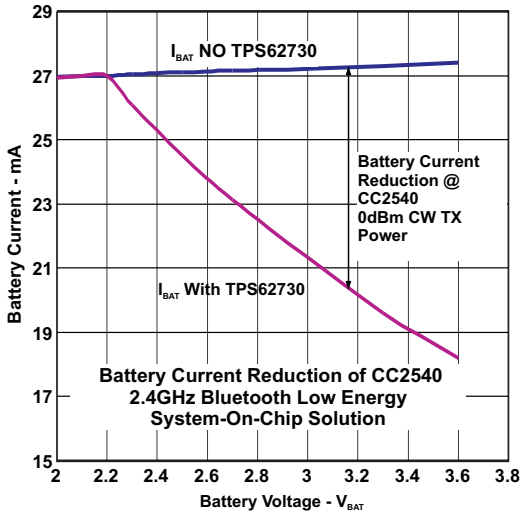
Check for Samples: TPS62730

FEATURES

- **Input Voltage Range V_{IN} from 1.9V to 3.9V**
- **Typ. 30nA Ultra Low Power Bypass Mode**
- **Typ. 25 µA DC/DC Quiescent Current**
- **Internal Feedback Divider Disconnect**
- **Typ. 2.1Ω Bypass Switch between V_{IN} and V_{OUT}**
- **Automatic Transition from DC/DC to Bypass Mode**
- **Up To 3MHz switch frequency**
- **Up to 95% DC/DC Efficiency**
- **Open Drain Status Output STAT**
- **Output Peak Current up to 100mA**
- **Fixed Output Voltage 2.1V**
- **Small External Output Filter Components 2.2µH/ 2.2µF**
- **Optimized For Low Output Ripple Voltage**
- **Small 1 × 1.5 × 0.6mm³ SON Package**
- **12 mm² Minimum Solution Size**

APPLICATIONS

- **CC2540 Bluetooth Low Energy System-On-Chip Solution**
- **Low Power Wireless Applications**
- **RF4CE, Metering**

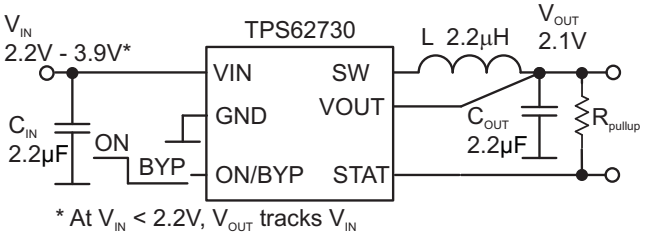


DESCRIPTION

The TPS62730 is a high frequency synchronous step down DC-DC converter optimized for ultra low power wireless applications. The device is optimized to supply TI's Low Power Wireless sub 1GHz and 2.4GHz RF transceivers and System-On-Chip-solutions. The TPS62730 reduces the current consumption drawn from the battery during TX and RX mode by a high efficient step down voltage conversion. It provides up to 100mA output current and allows the use of tiny and low cost chip inductors and capacitors. With an input voltage range of 1.9V to 3.9V the device supports Li-primary battery chemistries such as Li-SOCl2, Li-SO2, Li-MnO2 and also two cell alkaline batteries.

The TPS62730 features an Ultra Low Power bypass mode with typical 30nA current consumption to support sleep and low power modes of TI's CC2540 Bluetooth Low Energy and CC430 System-On-Chip solutions. In this bypass mode, the output capacitor of the DC/DC converter is connected via an integrated typ. 2.1Ω Bypass switch to the battery.

In DC/DC operation mode the device provides a regulated output voltage of 2.1V to the system. With a switch frequency up to 3MHz, the TPS62730 features low output ripple voltage and low noise even with a small 2.2uF output capacitor. The automatic transition into bypass mode during DC/DC operation prevents an increase of output ripple voltage and noise once the DC/DC converter operates close to 100% duty cycle. The device automatically enters bypass mode once the battery voltage falls below the transition threshold $V_{IT\ BYP}$. The TPS62730 is available in a 1 × 1.5mm² 6 pin QFN package.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PART NUMBER(1)	OUTPUT VOLTAGE [V](2)	Automatic Bypass Mode Transition Thresholds $V_{IT\ BYP}$			ORDERING	PACKAGE MARKING
			$V_{IT\ BYP}$ [V] rising V_{IN}	$V_{IT\ BYP}$ [V] falling V_{IN}	$V_{IT\ BYP}$ [mV] hysteresis		
–40°C to 85°C	TPS62730	2.10	2.25	2.20	50	TPS62730DRY	RP
	TPS62731 (2)	2.05	2.2	2.15	50	TPS62731DRY	RQ
	TPS62732 (2)	1.90	2.10	2.05	50	TPS62732DRY	RR
	TPS62734 (2)	2.10	2.28	2.23	50	TPS62734DRY	SL
	TPS62735 (2)	2.10	2.33	2.23	100	TPS62735DRY	SM

(1) The DRY package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.
(2) Device status is product preview, contact TI for more details

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	VIN, SW, VOUT	–0.3	4.2	V
	ON/BYP, STAT	–0.3	V_{IN} +0.3, ≤4.2	V
Temperature range	Operating junction temperature, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	°C
ESD rating(3)	Human Body Model - (HBM)		2	kV
	Machine Model (MM)		150	V
	Charge Device Model - (CDM)		1	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		DRY / 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	293.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	165.1	
θ_{JB}	Junction-to-board thermal resistance	160.8	
ψ_{JT}	Junction-to-top characterization parameter	27.3	
ψ_{JB}	Junction-to-board characterization parameter	159.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	65.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

operating ambient temperature T_A = –40 to 85°C (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage V_{IN}	1.9		3.9	V
Effective inductance	1.5	2.2	3	µH
Effective output capacitance connected to V_{OUT}	1.0		10	µF
Operating junction temperature range, T_J	–40		125	°C
T_A Operating free air temperature range	-40		85	

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.0V, V_{OUT} = 2.1V, ON/BYP = V_{IN}, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted), C_{IN} = 2.2µF, L = 2.2µH, C_{OUT} = 2.2µF, see parameter measurement information

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY								
V_{IN}	Input voltage range				1.9		3.9	V
I_Q	Operating quiescent current		ON/BYP = high, I_{OUT} = 0mA. V_{IN} = 3V device not switching			25	40	µA
			I_{OUT} = 0mA. device switching, V_{IN} = 3.0V, V_{OUT} = 2.1V			34		
			ON/BYP = high, Bypass switch active, V_{IN} = V_{OUT} = 2.1V			23		
I_{SD}	Shutdown current, Bypass Switch Activated		ON/BYP = GND, leakage current into V_{IN} (1)			30	550	nA
			ON/BYP = GND, leakage current into V_{IN}, T_A = 60°C (1)			110		
ON/BYP								
$V_{IH\ TH}$	Threshold for detecting high ON/BYP		1.9 V ≤ V_{IN} ≤ 3.9V , rising edge			0.8	1	V
$V_{IL\ TH}$	Threshold for detecting low ON/BYP		1.9 V ≤ V_{IN} ≤ 3.9V , falling edge		0.4	0.6		V
I_{IN}	Input bias Current					0	50	nA
POWER SWITCH								
$R_{DS(ON)}$	High side MOSFET on-resistance		V_{IN} = 3.0V			600		mΩ
	Low Side MOSFET on-resistance					350		
I_{LIMF}	Forward current limit MOSFET high-side		V_{IN} = 3.0V, open loop			410		mA
	Forward current limit MOSFET low side					410		mA
BYPASS SWITCH								
$R_{DS(ON)}$	Bypass Switch on-resistance		V_{IN} = 2.1V, I_{OUT} = 20mA, $T_J$max = 85°C			2.9	3.8	Ω
			V_{IN} = 3V			2.1		
$V_{IT\ BYP}$	Automatic Bypass Switch Transition Threshold (Activation / Deactivation)	ON/BYP = high	TPS62730 (2.1V)	ON / falling V_{IN}	2.14	2.20	2.3	V
				OFF/ rising V_{IN}	2.19	2.25	2.35	
			TPS62731 (2.05V)	ON / falling V_{IN}		2.15		
				OFF / rising V_{IN}		2.20		
			TPS62732 (1.9V)	ON / falling V_{IN}		2.05		
				OFF / rising V_{IN}		2.10		
			TPS62734 (2.1V)	ON / falling V_{IN}		2.23		
				OFF / rising V_{IN}		2.28		
			TPS62735 (2.3V)	ON / falling V_{IN}		2.23		
				OFF / rising V_{IN}		2.33		
STAT Status Output (Open Drain)								
V_{TSTAT}	Threshold level for STAT OUTPUT in % from V_{OUT}		ON/BYP = high and regulator is ready, V_{IN} falling			95		%
			ON/BYP = high and regulator is ready, V_{IN} rising			98		
V_{OL}	Output Low Voltage		Current into STAT pin I = 500µA, V_{IN} = 2.3V				0.4	V
V_{OH}	Output High Voltage		Open drain output, external pullup resistor				V_{IN}	
I_{LKG}	Leakage into STAT pin		ON/BYP = GND, V_{IN} = V_{OUT} = 3V			0	50	nA
REGULATOR								
t_{ONmin}	Minimum ON time		V_{IN} = 3.0V, V_{OUT} = 2.1V, I_{OUT} = 0 mA			180		ns
t_{OFFmin}	Minimum OFF time		V_{IN} = 2.3V			50		ns
t_{Start}	Regulator start up time from transition ON/BYP = high to STAT = low		V_{IN} = 3.0V, V_{OUT} = 3.0V			50		µs

(1) Shutdown current into VIN pin, includes internal leakage

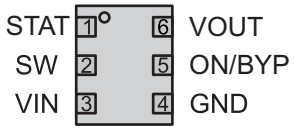
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.0V, V_{OUT} = 2.1V, ON/BYP = V_{IN}, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted), C_{IN} = 2.2µF, L = 2.2µH, C_{OUT} = 2.2µF, see parameter measurement information

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_{REF}	Internal Reference Voltage				0.70		V
V_{VOUT}	VOUT Feedback Voltage Comparator Threshold Accuracy	V_{IN} = 3.0V	T_A = 25°C	–1.5	0	1.5	%
			T_A = –40°C to 85°C	–2.5	0	2.5	
	DC output voltage load regulation	I_{OUT} = 1mA to 50mA V_{IN} = 3.0V, V_{OUT} = 2.1 V			-0.01		%/mA
	DC output voltage line regulation	I_{OUT} = 20 mA, 2.4V ≤ V_{IN} ≤ 3.9V			0.01		%/V
I_{LK_SW}	Leakage current into SW pin	V_{IN} = V_{OUT} = V_{SW} = 3.0 V, ON/Byp= GND (2)			0.0	100	nA

(2) The internal resistor divider network is disconnected from VOUT pin.

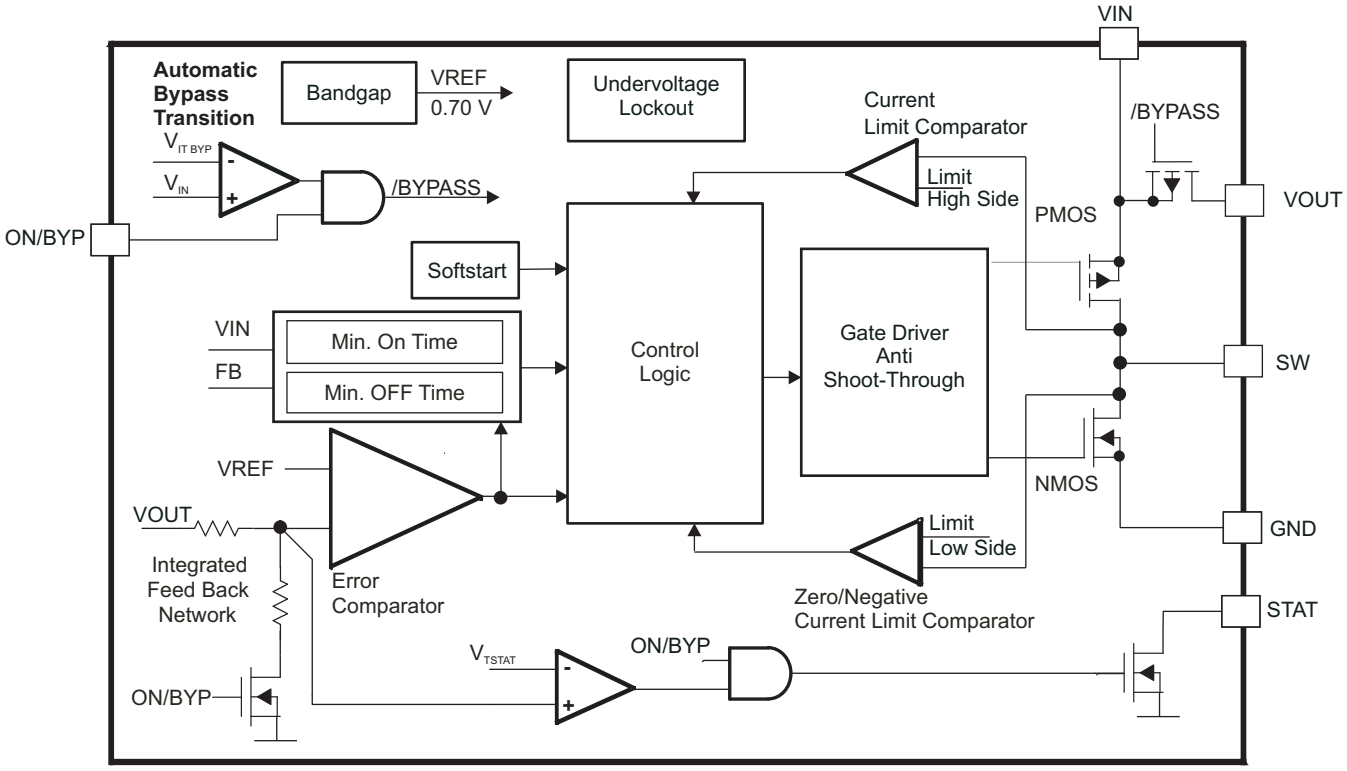
DRY PACKAGE
(TOP VIEW)



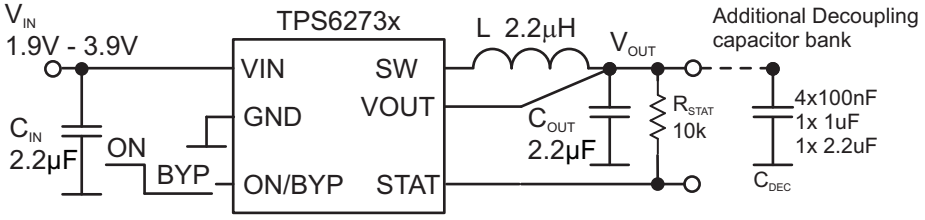
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO		
VIN	3	PWR	V_{IN} power supply pin. Connect this pin close to the VIN terminal of the input capacitor. A ceramic capacitor of 2.2µF is required.
GND	4	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
ON/BYP	5	IN	This is the mode selection pin of the device. Pulling this pin to low forces the device into ultra low power bypass mode. The output of the DC/DC converter is connected to VIN via an internal bypass switch. Pulling this pin to high enables the DC/DC converter operation. This pin must be terminated and is controlled by the system. In case of CC2540, connect this to the power down signal which is output on one of the P1.x ports (see CC2540 user guide).
SW	2	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal.
VOUT	6	IN	Feedback Pin for the internal feedback divider network and regulation loop. The internal bypass switch is connected between this pin and VIN. Connect this pin directly to the output capacitor with short trace.
STAT	1	OUT	This is the open drain status output with active low level. An internal comparator drives this output. The pin is high impedance with ON/BYP = low. With ON/BYP set to high the device and the internal VOUT comparator becomes active. The STAT pin is set to low once the output voltage is higher than 93% of nominal VOUT and high impedance once it is below this threshold. If not used, this pin can be left open.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



C_{IN}, C_{OUT}: Murata GRM155R60J225ME15D 2.2 µF 0402 size
C_{Load}: 4 x Murata GRM155R61A104KA01D 100nF
1 x 2.2 µF GRM155R60J225ME15D
1 x 1µF GRM155R61A105KE15D

L: Murata LQM21PN2R2NGC 2.2 µH, FDK MIPSZ2012 2R2

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Output current	1
η	Efficiency	vs Input voltage	2
V_{OUT}	Output voltage	vs Output current	3
	Output Voltage	vs Input voltage	4
I_{SD}	Shutdown current bypass mode	vs Input voltage	5
I_Q	Operating quiescent current	vs Input voltage	6
$r_{DS(ON)}$	Bypass Drain-source on-state resistance	vs Input voltage and ambient temperature	7
	PMOS Static drain-source on-state resistance	vs Input voltage and ambient temperature	8
	NMOS Static drain-source on-state resistance	vs Input voltage and ambient temperature	9
	Automatic transition into bypass	Falling V_{IN}	10
	Automatic transition into bypass	Rising V_{IN}	11
	Switching frequency	vs I_{OUT} vs V_{IN}	12
V_{OUT}	Output ripple voltage	vs I_{OUT} vs V_{IN}	13
	PSRR	vs Frequency	14
	Noise Density	vs Frequency	15
	DC/DC mode operation	I_{OUT} = 10 mA	16
		I_{OUT} = 1 mA	17
		I_{OUT} = 18 mA	18
		I_{OUT} = 50 mA	19
	DC/DC mode operation line and load transient performance		20
	Automatic bypass transition with falling/rising input voltage		21
	DC/DC mode V_{OUT} AC load regulation performance		22
	Bypass mode operation V_{OUT} AC behavior ON/BYP = GND		23
	Startup behavior		24
	Spurious output noise		25
	Battery current reduction	vs Battery voltage	26
	Mode transition ON/BYP behavior		27

TYPICAL CHARACTERISTICS (continued)

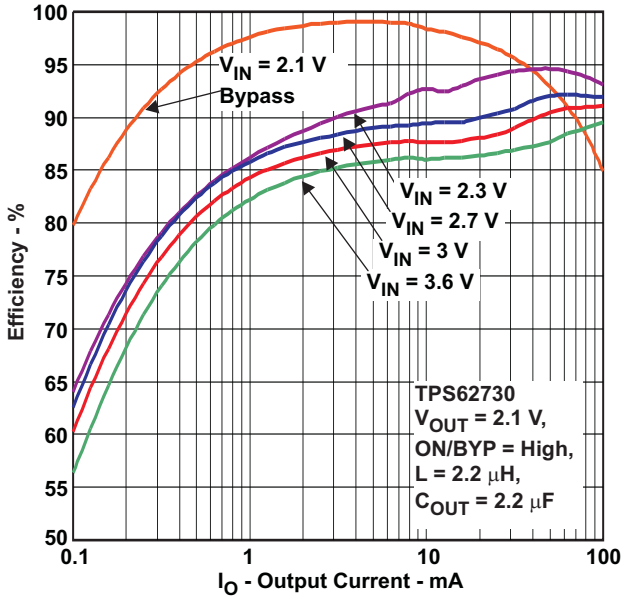


Figure 1. Efficiency vs Output Current

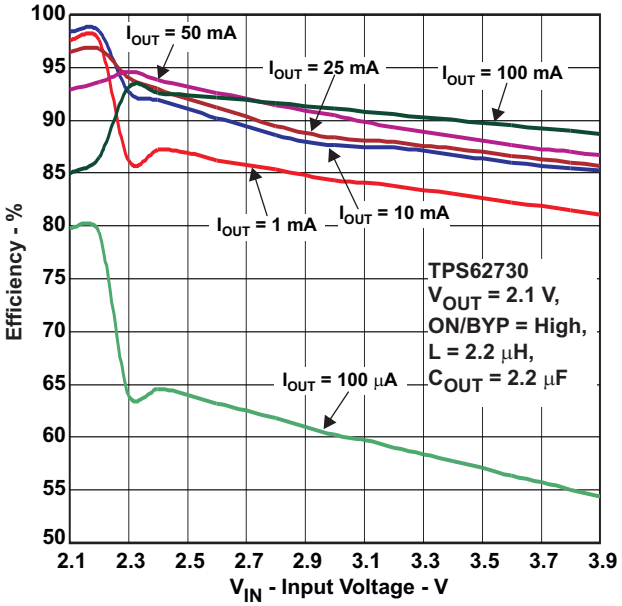


Figure 2. Efficiency vs Input Voltage

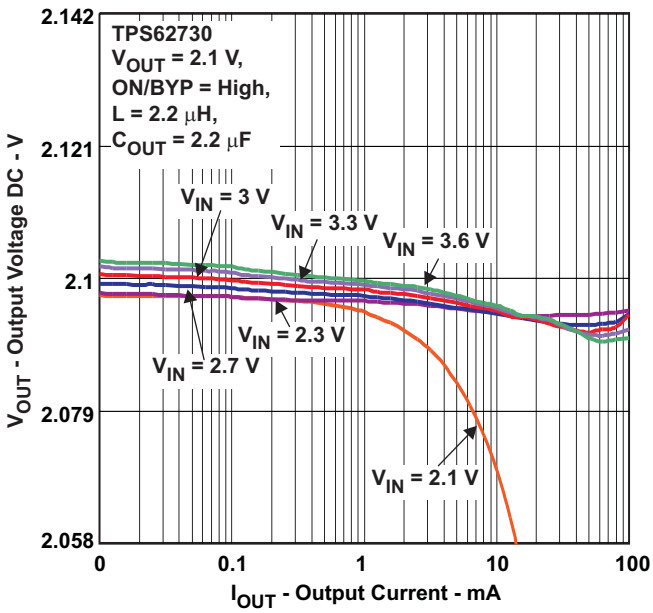


Figure 3. Output Voltage vs Output Current

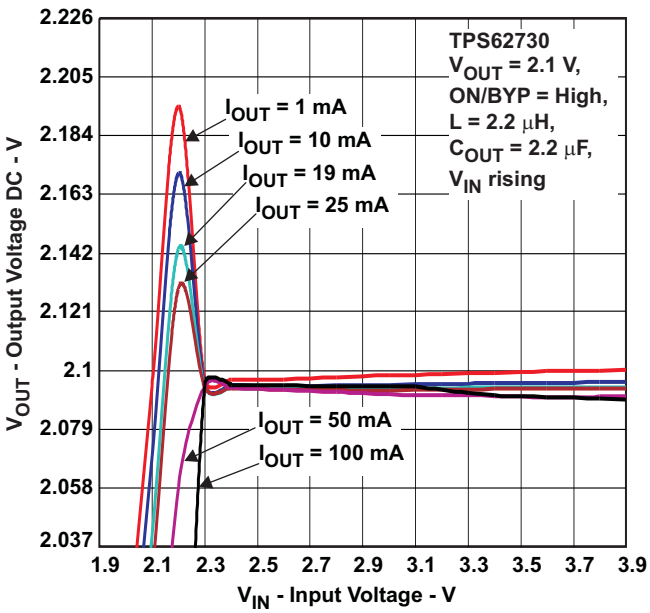


Figure 4. Output Voltage vs Input Voltage

TYPICAL CHARACTERISTICS (continued)

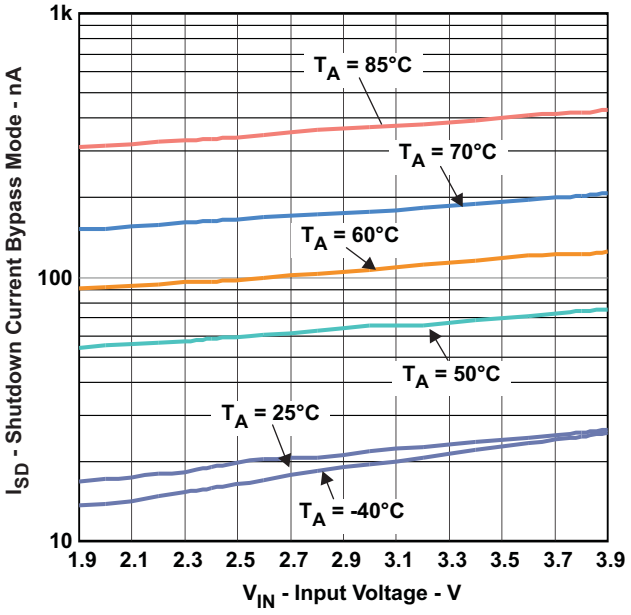


Figure 5. Shutdown Current Bypass Mode vs Input Voltage

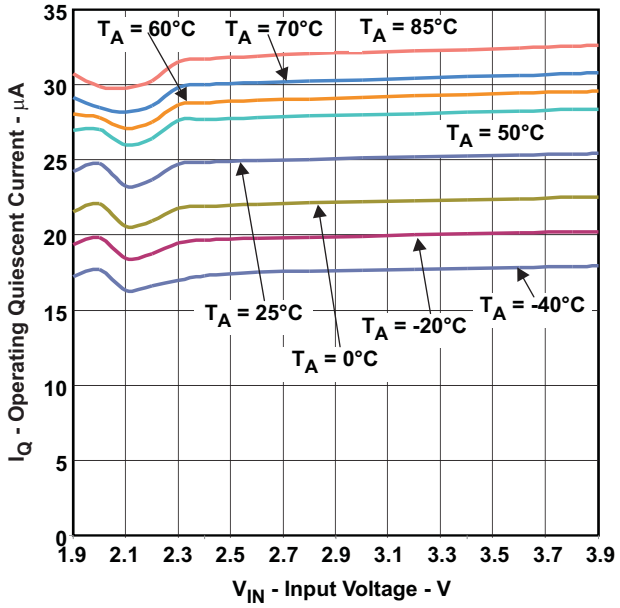


Figure 6. Operating Quiescent Current vs Input Voltage

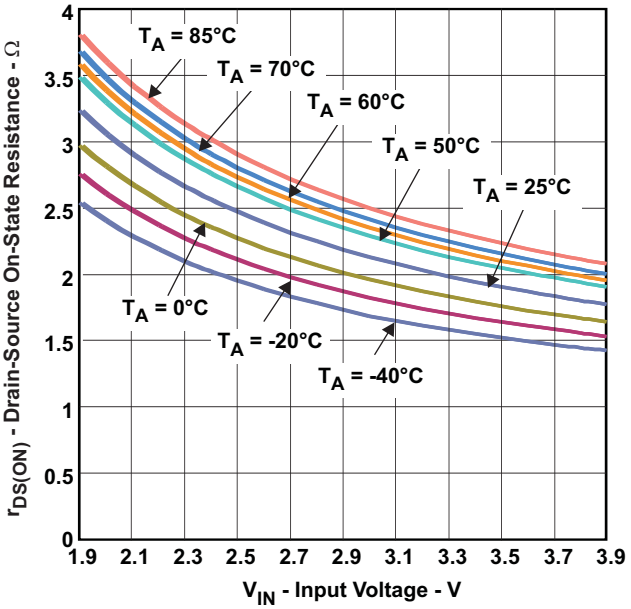


Figure 7. $r_{DS(ON)}$ Bypass vs Input Voltage

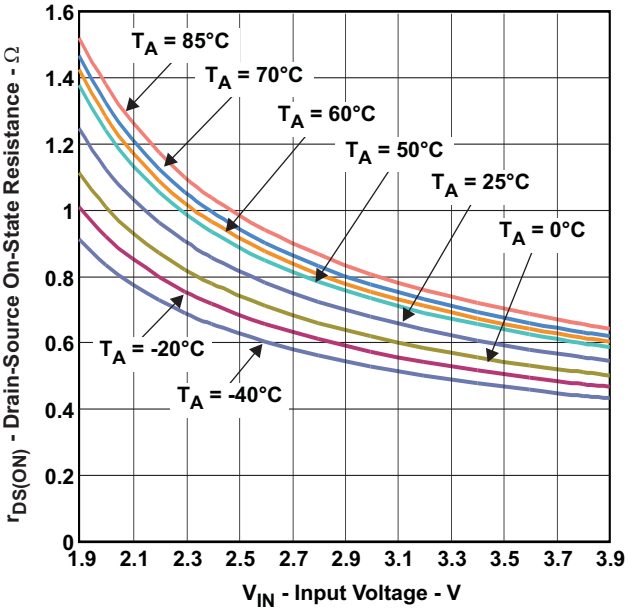


Figure 8. $r_{DS(ON)}$ PMOS vs Input Voltage

TYPICAL CHARACTERISTICS (continued)

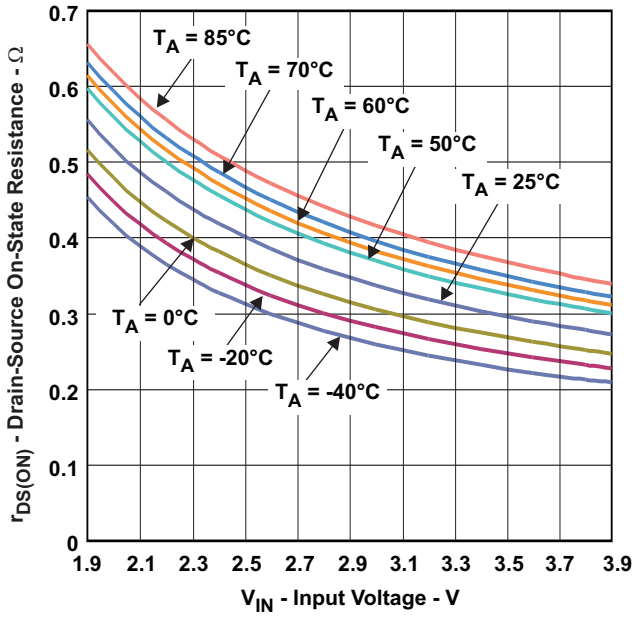


Figure 9. $r_{DS(ON)}$ NMOS vs Input Voltage

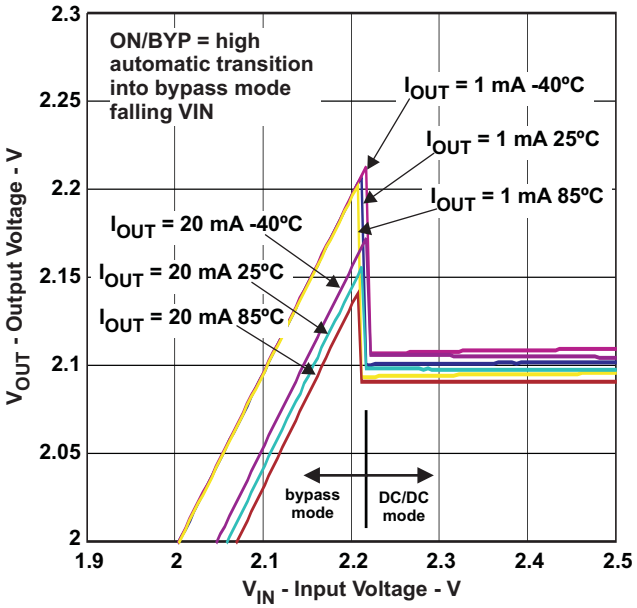


Figure 10. Automatic Transition into Bypass Mode - Falling V_{IN}

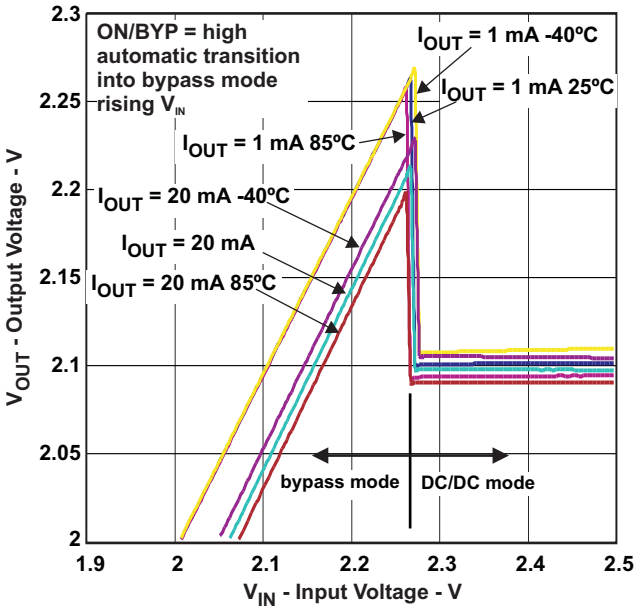


Figure 11. Automatic Transition into Bypass Mode - Rising V_{IN}

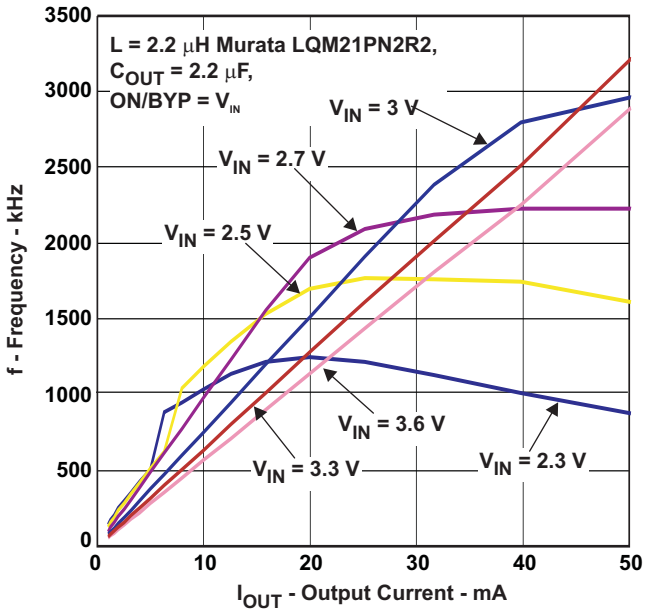


Figure 12. Switching Frequency vs I_{OUT} vs V_{IN}

TYPICAL CHARACTERISTICS (continued)

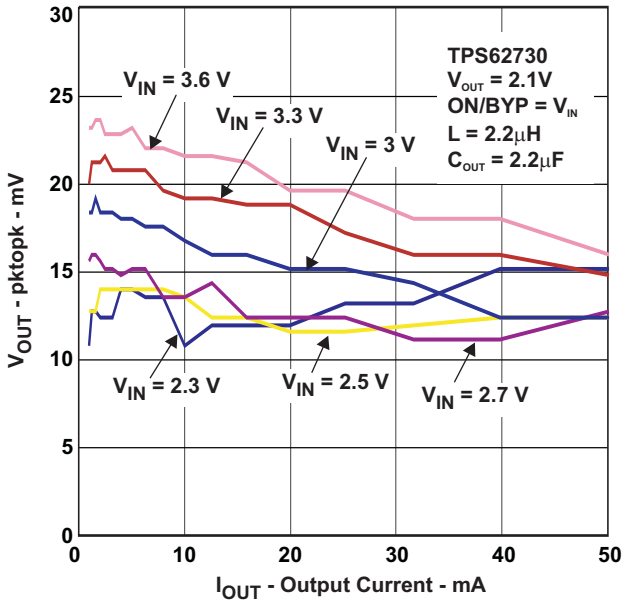


Figure 13. V_{OUT} vs I_{OUT} vs V_{IN}

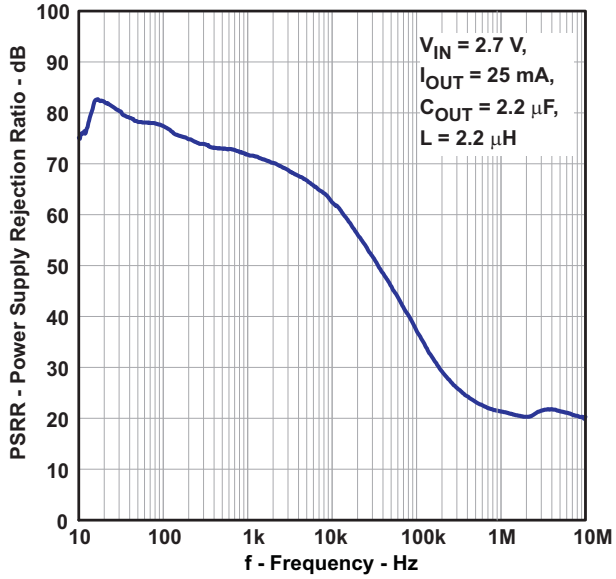


Figure 14. PSRR vs Frequency

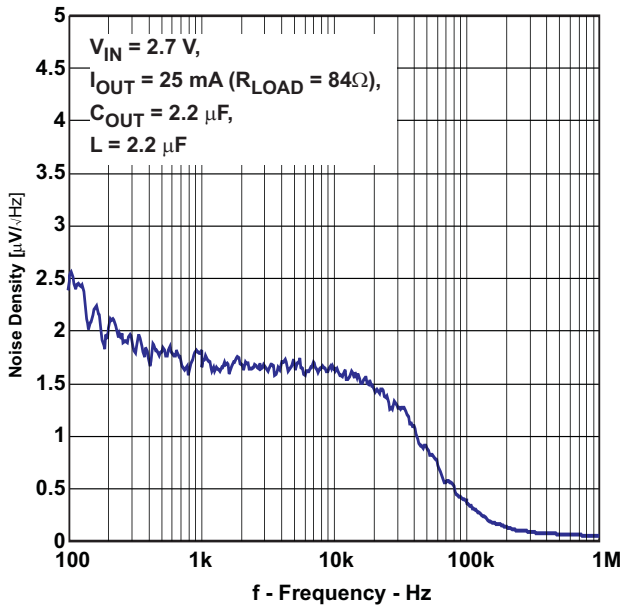


Figure 15. Noise Density vs Frequency

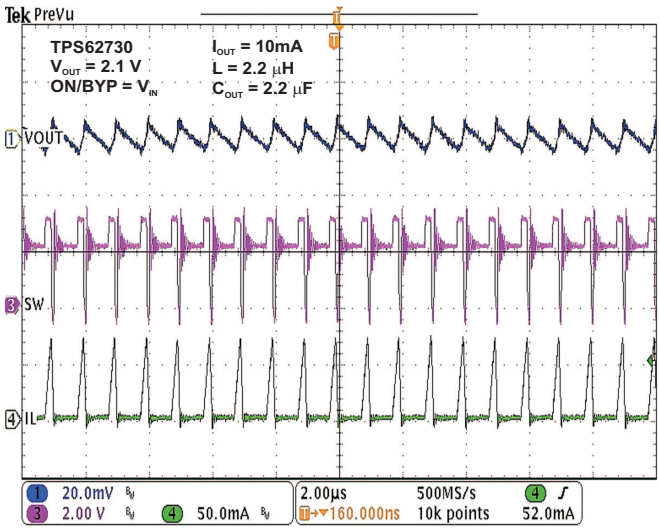


Figure 16. DC/DC Mode Operation I_{OUT} = 10mA

TYPICAL CHARACTERISTICS (continued)

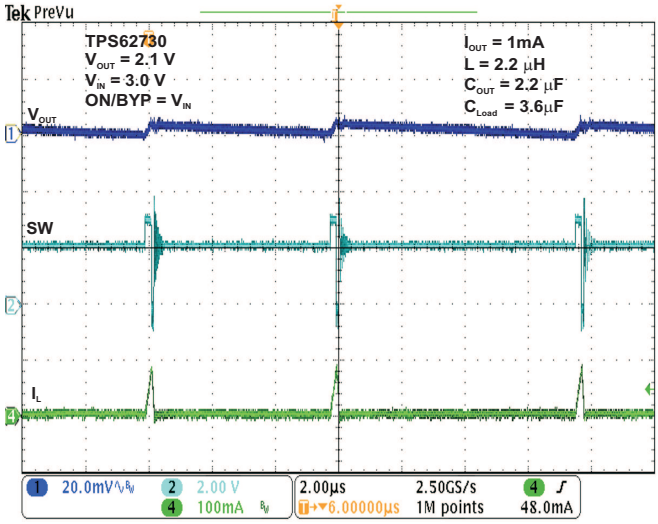


Figure 17. DC/DC Mode Operation I_{OUT} = 1mA

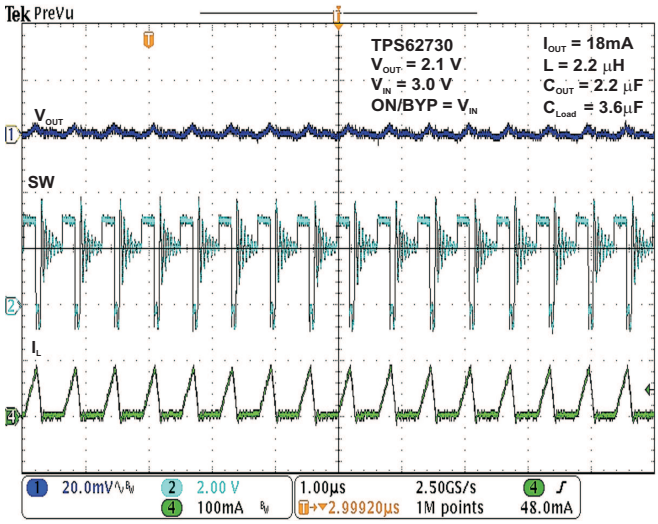


Figure 18. DC/DC Mode Operation I_{OUT} = 18mA

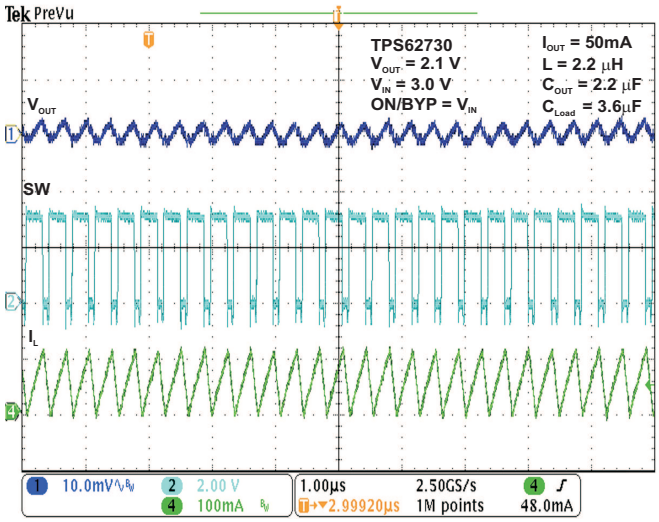


Figure 19. DC/DC Mode Operation I_{OUT} = 50mA

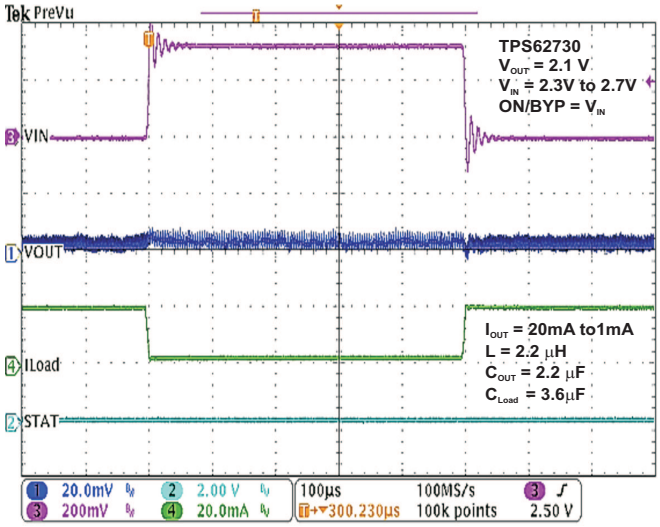


Figure 20. DC/DC Mode Operation Line and Load Transient Performance

TYPICAL CHARACTERISTICS (continued)

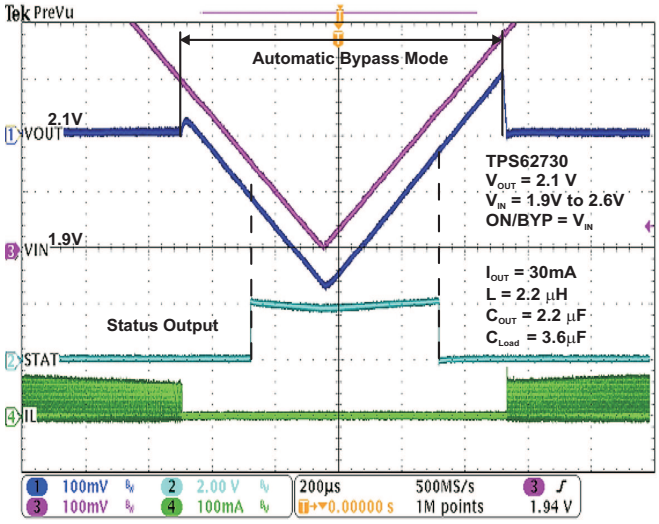


Figure 21. Automatic Bypass Transition with Falling / Rising Input Voltage V_{IN}

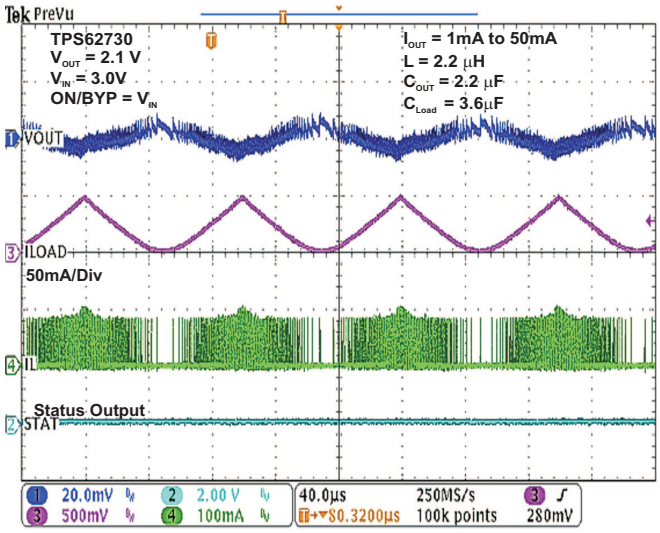


Figure 22. DC/DC Mode V_{OUT} AC Load Regulation Performance

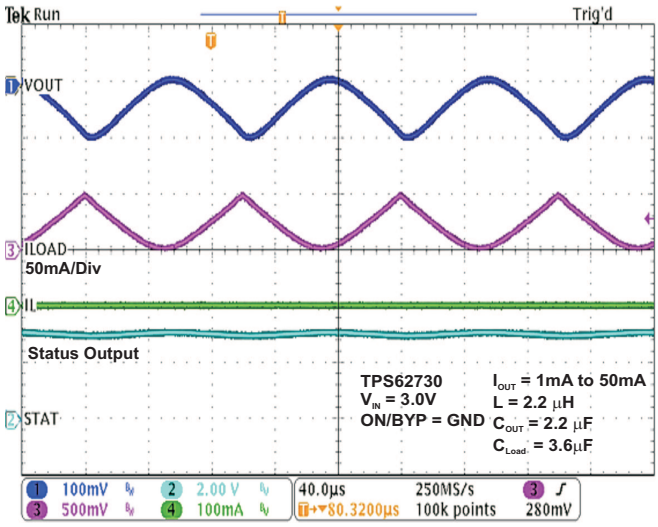


Figure 23. Bypass Mode Operation V_{OUT} AC Behavior ON/BYP = GND

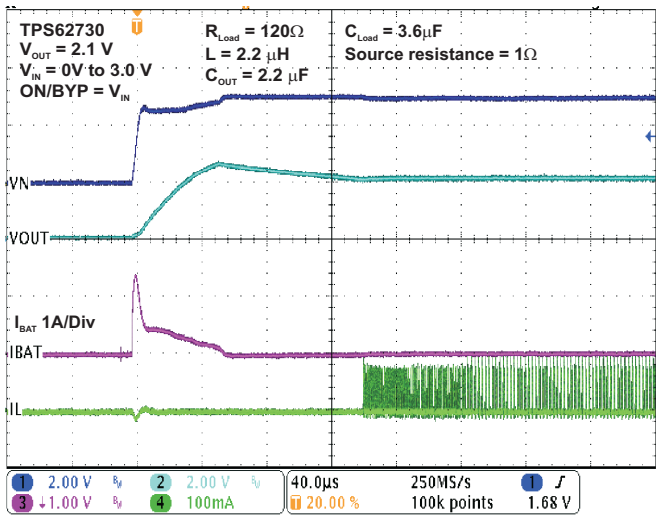


Figure 24. Startup Behavior

TYPICAL CHARACTERISTICS (continued)

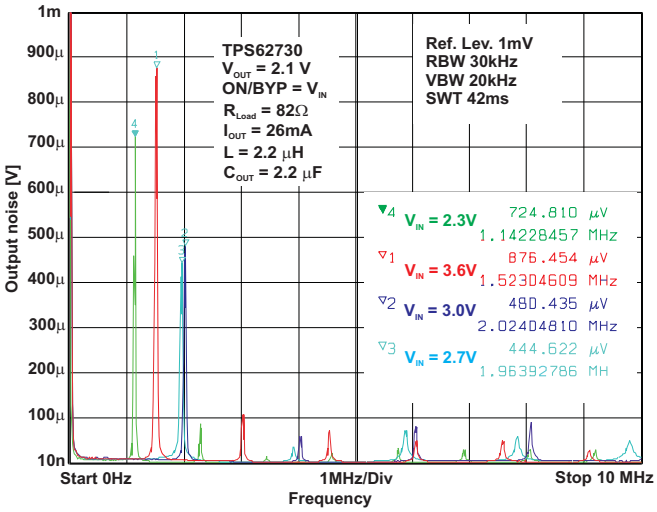


Figure 25. Spurious Output Noise TPS62730 I_{OUT} 26mA

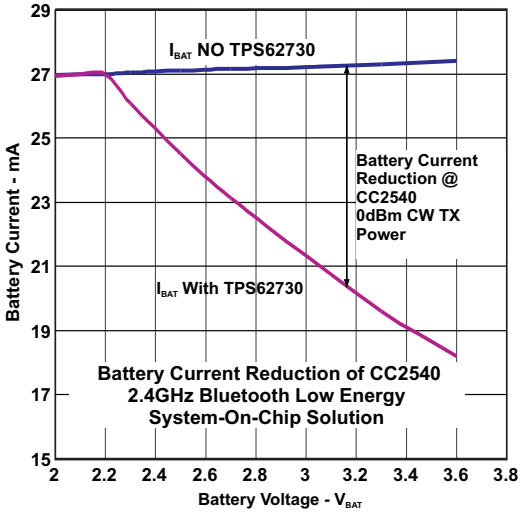


Figure 26. Battery Current Reduction vs Battery Voltage

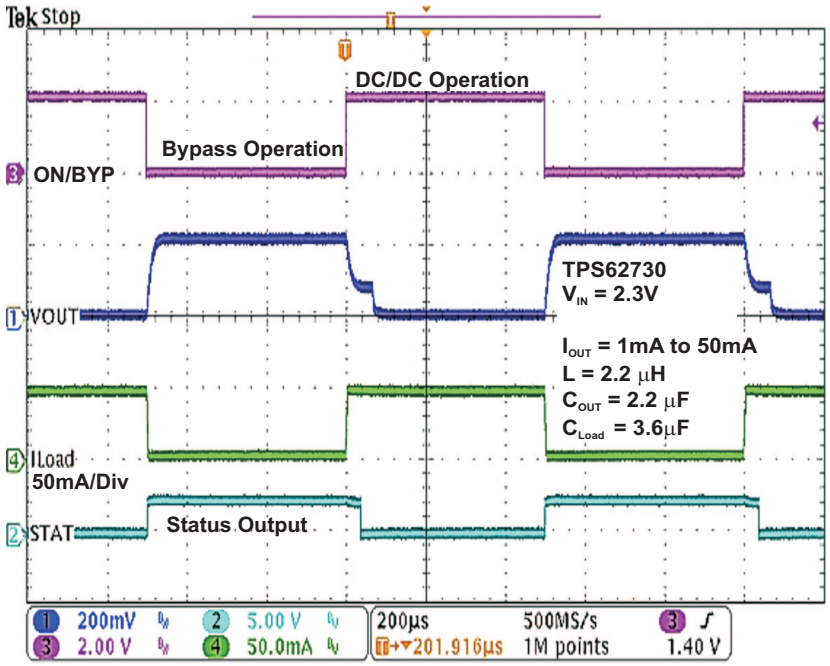


Figure 27. Mode Transition ON/BYP Behavior

DETAILED DESCRIPTION

The TPS62730 combines a synchronous buck converter for high efficient voltage conversion and an integrated ultra low power bypass switch to support low power modes of modern micro controllers and RF IC's. The synchronous buck converter includes TI's DCS-Control™, an advanced regulation topology, that combines the advantages of hysteretic and voltage mode control architectures. While a comparator stage provides excellent load transient response, an additional voltage feedback loop ensures high DC accuracy as well. The DCS-Control™ enables switch frequencies up to 3MHz, excellent transient and AC load regulation as well as operation with small and cost competitive external components. The TPS6273x devices offer fixed output voltage options featuring smallest solution size by using only three external components. Furthermore this step down converter provides excellent low output voltage ripple over the entire load range which makes this part ideal for RF applications. In the ultra low power bypass mode, the output of the device VOUT is directly connected to the input VIN via the internal bypass switch. In this mode, the buck converter is shut down and consumes only 30nA typical input current. Once the device is turned from ultra low power bypass mode into buck converter operation for a RF transmission, all the internal circuits of the regulator are activated within a start up time tStart of typ. 50µs. During this time the bypass switch is still turned on and maintains the output VOUT connected to the input VIN. Once the DC/DC converter is settled and ready to operate, the internal bypass switch is turned off and the system is supplied by the output capacitor and the other decoupling capacitors. The buck converter kicks in once the capacitors connected to VOUT are discharged to the level of the nominal buck converter output voltage. Once the output voltage falls below the threshold of the internal error comparator, a switch pulse is initiated, and the high side switch of the DC/DC converter is turned on. It remains turned on until a minimum on time of t_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high side switch current limit. Once the high side switch turns off, the low side switch rectifier is turned on and the inductor current ramps down until the high side switch turns on again or the inductor current reaches zero. The converter operates in the PFM (Pulse Frequency Modulation) mode during light loads, which maintains high efficiency over a wide load current range. In PFM Mode, the device starts to skip switch pulses and generates only single pulses with an on time of t_{ONmin}. The PFM mode of TPS62730 is optimized for low output ripple voltage if small external components are used.

The on time t_{ONmin} can be estimated to:

$$t_{ONmin} = \frac{V_{OUT}}{V_{IN}} \times 260\ ns \quad (1)$$

Therefore, the peak inductor current in PFM mode is approximately:

$$I_{LPFMpeak} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ONmin} \quad (2)$$

With

t_{ONmin}: High side switch on time [ns]
V_{IN}: Input voltage [V]
V_{OUT}: Output voltage [V]
L : Inductance [µH]
$I_{LPFMpeak}$: PFM inductor peak current [mA]

ON/BYP MODE SELECTION

The DC/DC converter is activated when ON/BYP is set high. For proper operation, the ON/BYP pin must be terminated and may not be left floating. This pin is controlled by the RF transceiver or micro controller for proper mode selection. Pulling the ON/BYP pin low activates the Ultra Low Power Bypass Mode with typical 30nA current consumption. In this mode, the internal bypass switch is turned on and the output of the DC/DC converter is connected to the battery VIN. All other circuits like the entire internal-control circuitry, the High Side and Low Side MOSFET's of the DC/DC output stage are turned off as well the internal resistor feedback divider is disconnected. The ON/BYP need to be controlled by a Micro controller for proper mode selection.

START UP

Once the device is supplied with a battery voltage, the bypass switch is activated. If the ON/BYP pin is set to high, the device operates in bypass mode until the DC/DC converter has settled and can kick in. During start up, high peak currents can flow over the bypass switch to charge up the output capacitor and the additional decoupling capacitors in the system.

AUTOMATIC TRANSITION FROM DC/DC TO BYPASS OPERATION

With pin ON/BYP set to high, the TPS62730 features an automatic transition between DC/DC and bypass mode to reduce the output ripple voltage to zero. Once the input voltage comes close to the output voltage of the DC/DC converter, the DC/DC converters operates close to 100% duty cycle operation. At this operating condition, the switch frequency would start to drop and would lead to increased output ripple voltage. The internal bypass switch is turned on once the battery voltage at VIN trips the Automatic Bypass Transition Threshold VIT BYP for falling VIN. The DC/DC regulator is turned off and therefore it generates no output ripple voltage. Due to the output is connected via the bypass switch to the input, the output voltage follows the input voltage minus the voltage drop across the internal bypass switch. In this mode the current consumption of the DC/DC converter is reduced to typically 23µA. Once the input voltage increases and trips the bypass deactivation threshold VIT BYP for rising VIN, the DC/DC regulator turns on and the bypass switch is turned off.

INTERNAL CURRENT LIMIT

The TPS62730 integrates a High Side and Low Side MOSFET current limit to protect the device against heavy load or short circuit when the DC/DC converter is active. The current in the switches is monitored by current limit comparators. When the current in the High Side MOSFET reaches its current limit, the High Side MOSFET is turned off and the Low Side MOSFET is turned on to ramp down the current in the inductor. The High Side MOSFET switch can only turn on again, once the current in the Low Side MOSFET switch has decreased below the threshold of its current limit comparator. The bypass switch doesn't feature a current limit to support lowest current consumption.

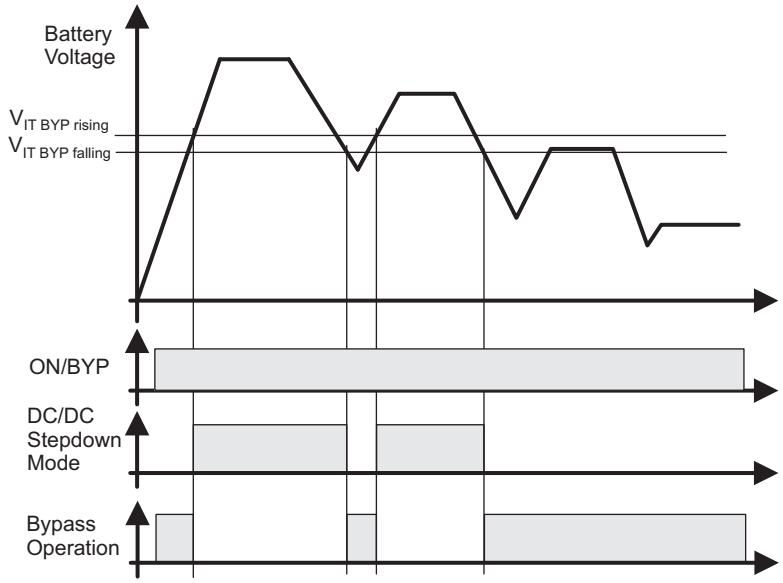


Figure 28. Operation Mode Diagram with ON/BYP = High

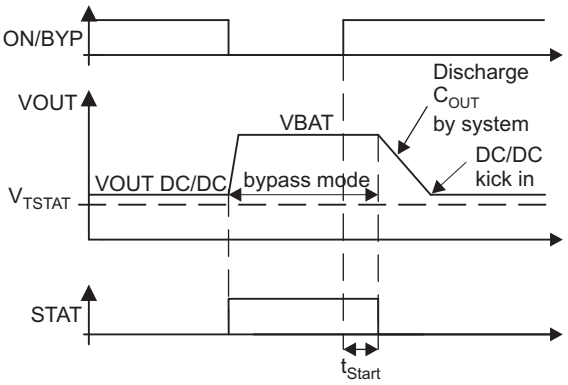


Figure 29. Signal Status Diagram ON/BYP, VOUT, STAT

APPLICATION INFORMATION

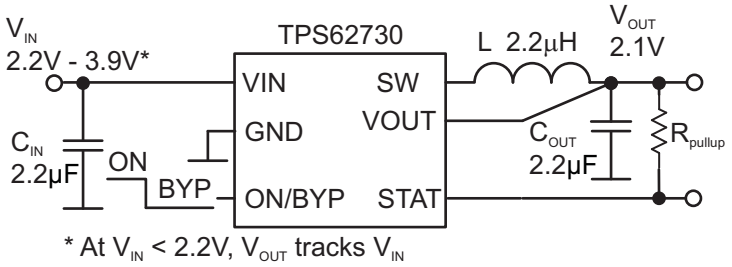


Figure 30. Typical Application

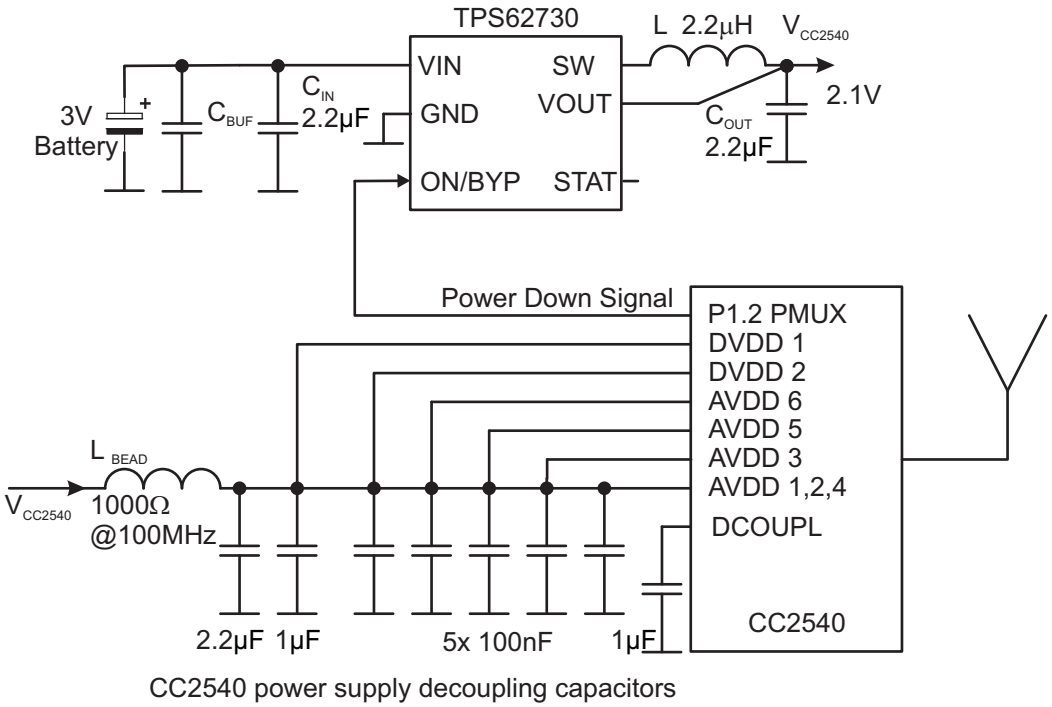
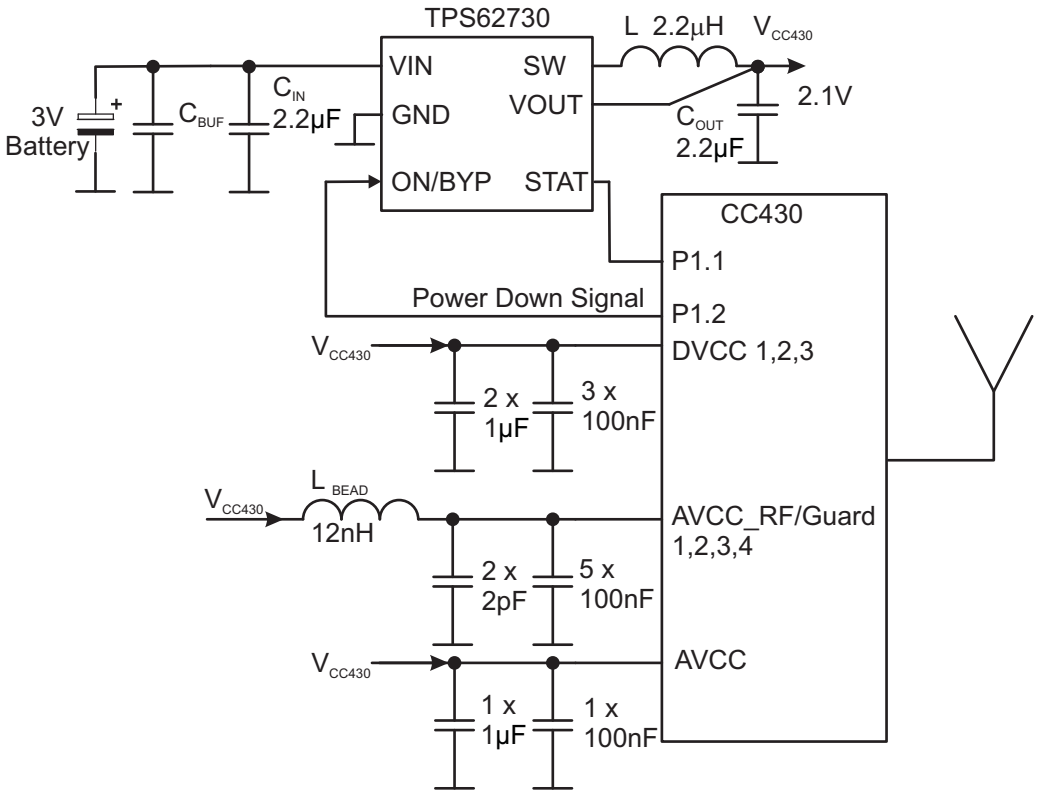


Figure 31. Application Example CC2540



CC430 power supply decoupling capacitors

Figure 32. Application Example CC430

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS62730 is optimized to operate with effective inductance values in the range of 1.5µH to 3µH and with effective output capacitance in the range of 1.0µF to 10µF. The internal compensation is optimized to operate with an output filter of L = 2.2µH and C_{OUT} = 2.2µF, which gives and LC output filter corner frequency of:

$$f_C = \frac{1}{2 \times \pi \times \sqrt{(2.2\mu H \times 2.2\mu F)}} = 72kHz \quad (3)$$

INDUCTOR SELECTION

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher $V_{I\,N}$ or $V_{O\,UT}$. Equation 4 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 5

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (4)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (5)$$

With:

f = Switching Frequency
L = Inductor Value
ΔI_L= Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e., quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS62730 converters.

Table 1. List of inductors

INDUCTANCE [µH]	DIMENSIONS [mm3]	INDUCTOR TYPE	SUPPLIER
2.2	2.0 × 1.2 × 1.0	LQM21PN2R2NGC	Murata
2.2	2.0 × 1.2 × 1.0	MIPSZ2012	FDK

DC/DC OUTPUT CAPACITOR SELECTION

The DCS-Control™ scheme of the TPS62730 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. At light load currents the converter operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current.

ADDITIONAL DECOUPLING CAPACITORS

In addition to the output capacitor there are further decoupling capacitors connected to the output of the TPS62730. These decoupling capacitor are placed closely at the RF transmitter or micro controller. The total capacitance of these decoupling capacitors should be kept to a minimum and should not exceed the values given in the reference designs, see Figure 31 and Figure 32. During mode transition from DC/DC operation to bypass mode the capacitors on the output VOUT are charged up to the battery voltage VIN via the internal bypass switch. During mode transition from bypass mode to DC/DC operation, these capacitors need to be discharged by the system supply current to the nominal output voltage threshold until the DC/DC will kick in. The charge change in the output and decoupling capacitors can be calculated according to Equation 6. The energy loss due to charge/discharge of the output and decoupling capacitors can be calculated according to Equation 7

$$dQ_{COUT\_CDEC} = C_{COUT\_CDEC} \times \left(V_{IN} - V_{OUT\_DC\_DC}\right) \quad (6)$$

$$E_{Charge\_Loss} = \tfrac{1}{2} \times C_{COUT\_CDEC} \times \left(V_{IN}^{\ 2} - V_{OUT\_DC\_DC}^{\ 2}\right) \quad (7)$$

with

dQ_{COUT_CDEC} : Charge change needed to charge up / discharge the output and decoupling capacitors from VOUT_DC_DC to V_{IN} and vice versa

C_{COUT_CDEC}: Total capacitance on the VOUT pin of the device, includes output and decoupling capacitors

V_{IN}: Input (battery) voltage

$V_{OUT\_DC\_DC}$: nominal DC/DC output voltage V_{OUT}

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to ensure proper function of the device and to minimize input voltage spikes. For most applications a 2.2µF to 4.7µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Table 2 shows a list of tested input/output capacitors.

INPUT BUFFER CAPACITOR SELECTION

In addition to the small ceramic input capacitor a larger buffer capacitor C_{Buf} is recommended to reduce voltage drops and ripple voltage. When using battery chemistries like Li-SOCl2, Li-SO2, Li-MnO2, the impedance of the battery has to be considered. These battery types tend to increase their impedance depending on discharge status and often can support output currents of only a few mA. Therefore a buffer capacitor is recommended to stabilize the battery voltage during DC/DC operations e.g. for a RF transmission. A voltage drop on the input of the TPS62730 during DC/DC operation impacts the advantage of the step down conversion for system power reduction. Furthermore the voltage drops can fall below the minimum recommended operating voltage of the device and leads to an early system cut off. Both impacts effects reduce the battery life time. To achieve best performance and to extract most energy out of the battery a good procedure is to design the select the buffer capacitor value for an voltage drop below 50mVpp during DC/DC operation. The capacitor value strongly depends on the used battery type, as well the current consumption during a RF transmission as well the duration of the transmission.

Table 2. List of Capacitor

CAPACITANCE [µF]	SIZE	CAPACITOR TYPE	SUPPLIER
2.2	0402	GRM155R60J225	Murata

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the High Side MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Especially RF designs demand careful attention to the PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems and interference with RF circuits. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The VOUT line should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line).

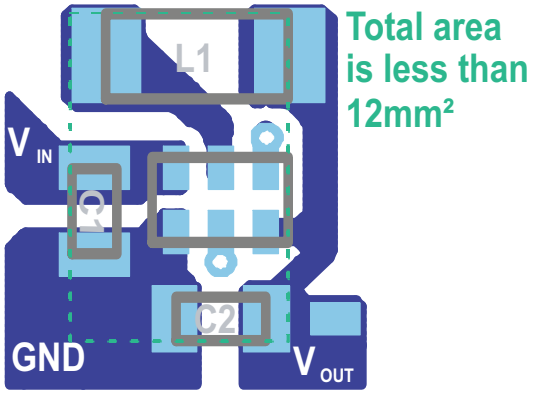


Figure 33. Recommended PCB Layout for TPS62730

PACKAGING INFORMATION

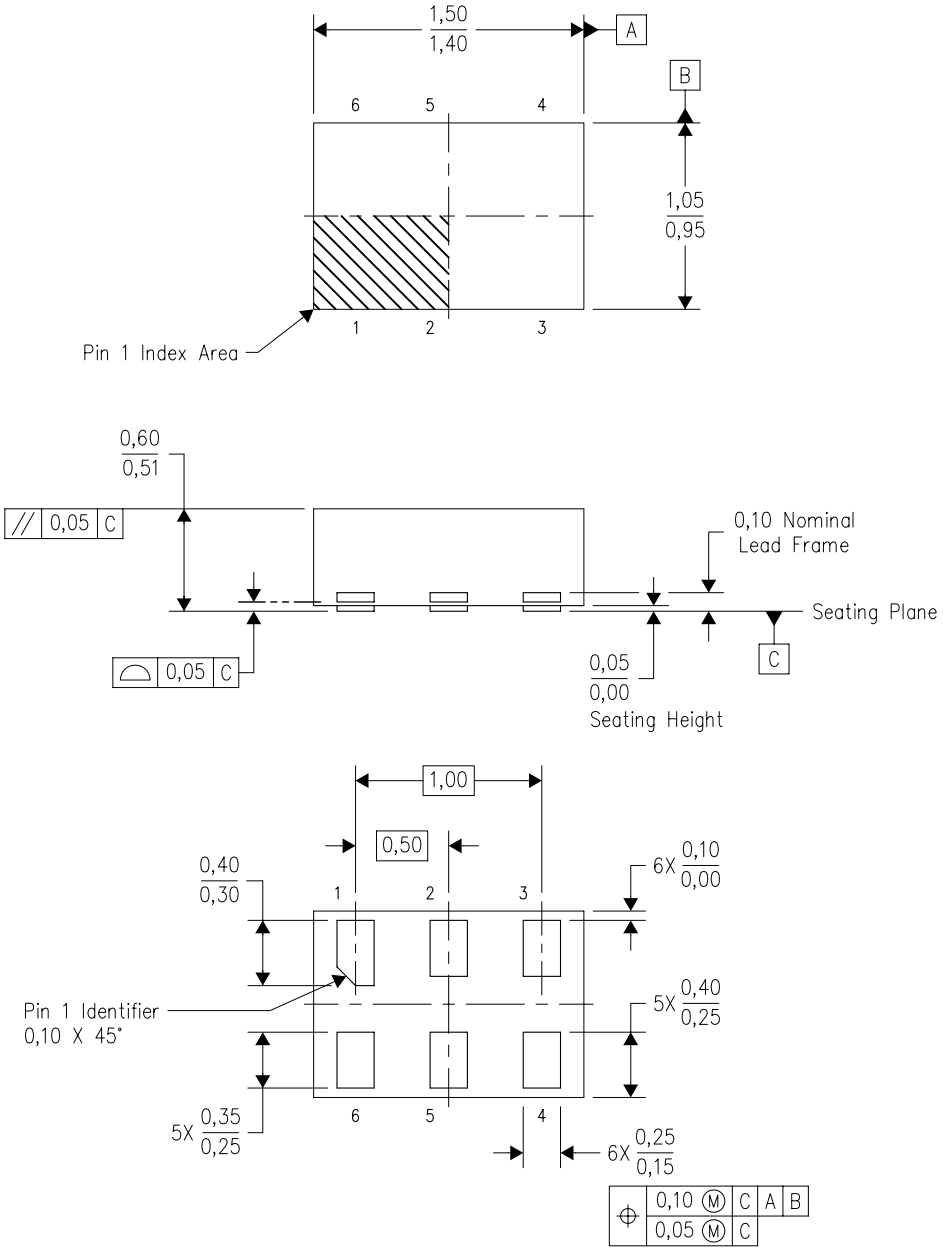
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS62730DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS62730DRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

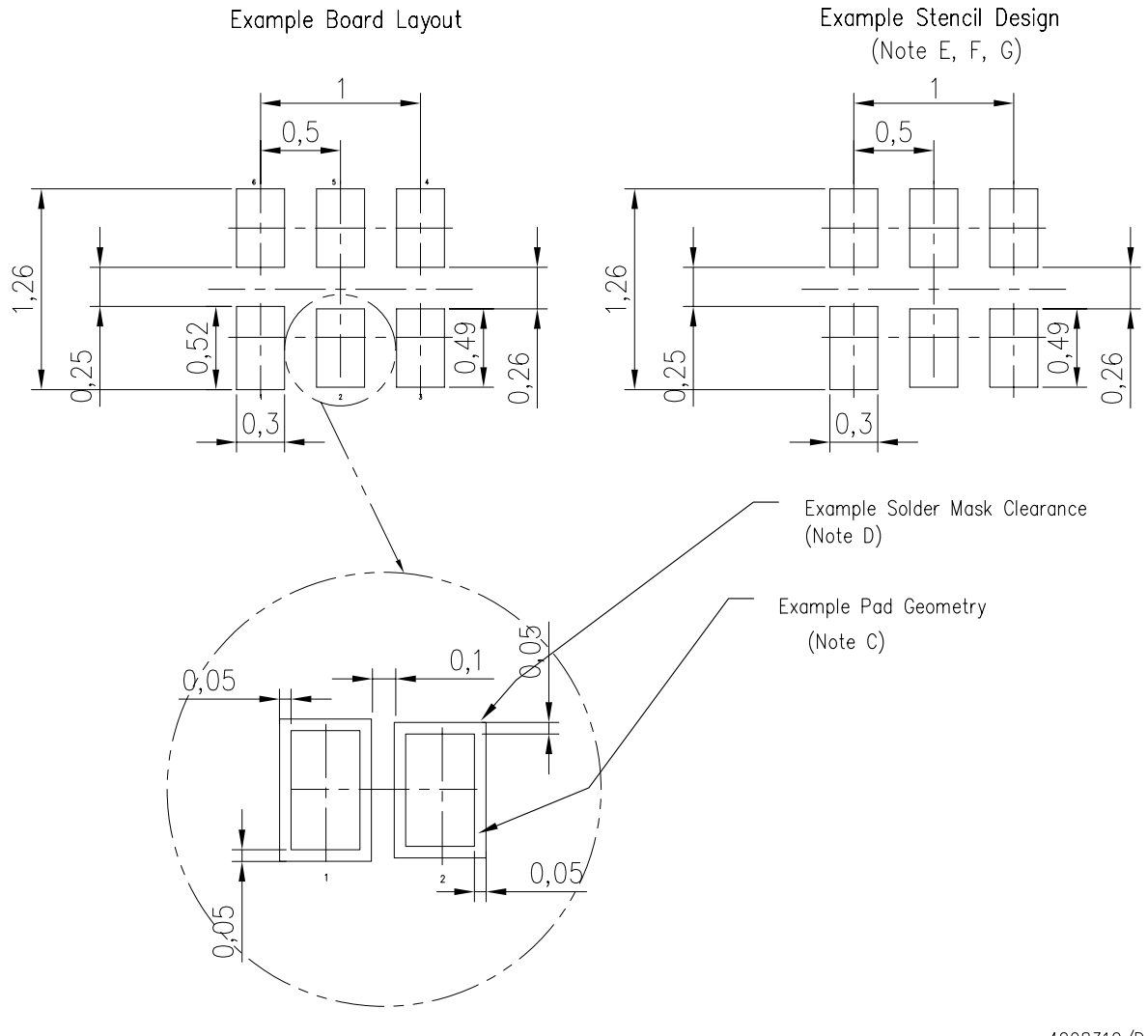
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/D 12/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation UFAD.

DRY (S–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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