

3A Processor Supply with I²C Compatible Interface and Remote Sense

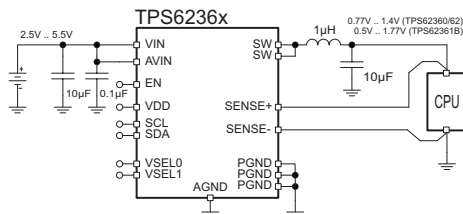
Check for Samples: [TPS62360](#), [TPS62361B](#), [TPS62362](#)

FEATURES

- **3A Peak Output Current**
- **Highest Efficiency:**
 - Low R_{DS,on} Switch and Active Rectifier
 - Power Save Mode for Light Loads
- **I²C High Speed Compatible Interface**
- **Programmable Output Voltage for Digital Voltage Scaling**
 - TPS62360/62: 0.77V to 1.4V, 10mV Steps
 - TPS62361B: 0.5V to 1.77V, 10mV Steps
- **Excellent DC/AC Output Voltage Regulation**
 - Differential Load Sensing
 - Precise DC Output Voltage Accuracy
 - DCS-Control™ Architecture for Fast and Precise Transient Regulation
- **Multiple Robust Operation/Protection Features:**
 - Soft Start
 - Programmable Slew Rate at Voltage Transition
 - Over Temperature Protection
 - Input Under Voltage Detection and Lockout
- **Available in 16-Bump, 2mm x 2mm NanoFree™ Package**
- **Low External Device Count: 27.5 mm² Solution Size**

APPLICATIONS

- **Dynamic Voltage Scale Compliant Processors and DSPs, Memory**
- **SmartReflex™ Compliant Power Supply**
- **Cell Phones, Smart Phones, Feature Phones**
- **Tablets, Netbooks, Clamshells**



DESCRIPTION

The TPS6236x are a family of high-frequency synchronous step down dc-dc converter optimized for battery-powered portable applications for a small solution size. With an input voltage range of 2.5V to 5.5V, common battery technologies are supported. The device provides up to 3A peak load current, operating at 2.5MHz typical switching frequency.

The devices convert to an output voltage range of 0.77V to 1.4V (TPS62360/62) and 0.5V to 1.77V (TPS62361B), programmable via I²C interface in 10mV steps. Dedicated inputs allow fast voltage transition to address processor performance operating points.

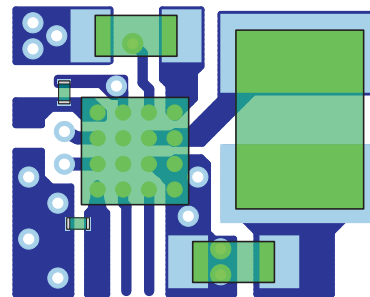
The TPS6236x supports low-voltage DSPs and processor cores in smart-phones and handheld computers including latest submicron processes. Dedicated hardware input pins allow simple transitions to performance operating points and retention modes of processors.

The devices focus on a high output voltage accuracy. The differential sensing and the DCS-Control™ architecture achieve precise static and dynamic, transient output voltage regulation.

The TPS6236x devices offer high efficiency step down conversion. The area of highest efficiency is extended towards low output currents to increase the efficiency while the processor is operating in retention mode, as well as towards highest output currents increasing the battery on-time.

The robust architecture and multiple safety features allow perfect system integration.

The 2mm x 2mm package and the low number of required external components lead to a tiny solution size of approximately 27.5 mm².



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DCS-Control, NanoFree, SmartReflex are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2011, Texas Instruments Incorporated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

| PART NUMBER | PACKAGE MARKING | PACKAGE | DEVICE SPECIFIC FEATURES ⁽¹⁾ |
|--------------------------|---|---------|--|
| TPS62360 ⁽²⁾ | See PACKAGE SUMMARY Section | CSP-16 | V _{OUT} = 0.77V to 1.4V, 10mV Steps |
| TPS62361B ⁽³⁾ | See PACKAGE SUMMARY Section | CSP-16 | V _{OUT} = 0.5V to 1.77V, 10mV Steps |
| TPS62362 ⁽⁴⁾ | See PACKAGE SUMMARY Section | CSP-16 | V _{OUT} = 0.77V to 1.4V, 10mV Steps |

- (1) Contact the factory to check availability of other output voltage or feature versions.
- (2) The YZH package is available in tape and reel. Add R suffix (TPS62360YZHR) to order quantities of 3000 parts per reel, T suffix for 250 parts per reel (TPS62360YZHT). For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.
- (3) The YZH package is available in tape and reel. Add R suffix (TPS62361BYZHR) to order quantities of 3000 parts per reel, T suffix for 250 parts per reel (TPS62361BYZHT). For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.
- (4) The YZH package is available in tape and reel. Add R suffix (TPS62362YZHR) to order quantities of 3000 parts per reel, T suffix for 250 parts per reel (TPS62362YZHT). For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | VALUE | | UNIT |
|--|--|-------|---------------------------|------|
| | | MIN | MAX | |
| Voltage range | VIN, AVIN, SW pin ⁽²⁾ | −0.3 | 7 | V |
| | EN, VSEL0, VSEL1, SENSE+ ⁽²⁾ | −0.3 | (V _{AVIN} +0.3V) | V |
| | SENSE− ⁽²⁾ | −0.3 | 0.3 | V |
| | SCL, SDA ⁽²⁾ | −0.3 | (V _{DD} +0.3V) | V |
| | VDD ⁽²⁾ | −0.3 | 3.6 | V |
| Continuous RMS VIN / SW current ⁽³⁾ | | | 1275 | mA |
| Temperature | Operating ambient temperature range, T _A ⁽⁴⁾ | −40 | 85 | °C |
| | Maximum operating junction temperature, T _J (MAX) | −40 | 150 | °C |
| | Storage temperature range, T _{stg} | −65 | 150 | °C |
| ESD rating ⁽⁵⁾ | Machine model | | 200 | V |
| | Charge device model | | 500 | V |
| | Human body model | | 2 | kV |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) In order to be consistent with the TI reliability requirement for the silicon chips (100K Power-On-Hours at 105°C junction temperature), the current should not continuously exceed 1275mA in the VIN pin and 2550mA in the SW pins so as to prevent electromigration failure in the solder. See [THERMAL AND DEVICE LIFE TIME INFORMATION](#).
- (4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(max)}] is dependent on the maximum operating junction temperature [T_{J(max)}], the maximum power dissipation of the device in the application [P_{D(max)}], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: T_{A(max)} = T_{J(max)} − (θ_{JA} × P_{D(max)})
- (5) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | TPS6236x | UNITS |
|-------------------------------|---|----------|-------|
| | | YZH | |
| | | 16 PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | 94.8 | °C/W |
| θ_{JCTop} | Junction-to-case (top) thermal resistance ⁽³⁾ | 25 | |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | 60 | |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 3.2 | |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 57 | |
| θ_{JCbott} | Junction-to-case (bottom) thermal resistance ⁽⁷⁾ | n/a | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

| | | | MIN | TYP | MAX | UNIT |
|------------------|---|-------------------------|-----|-----|-----|------|
| V _{IN} | Input voltage range, V _{IN} | I _{OUT} ≤ 2.5A | 2.5 | | 5.5 | V |
| | | I _{OUT} > 2.5A | 3 | | 5.5 | V |
| I _{OUT} | Max. continuous output current ⁽¹⁾ | | 2.5 | | | A |
| T _A | Operating ambient temperature | | −40 | | 85 | °C |
| T _J | Operating junction temperature | | −40 | | 125 | °C |

- (1) Drawing continuously more than 2.5A might impact the device life time. See [THERMAL AND DEVICE LIFE TIME INFORMATION](#) for details.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies for $V_{IN} = 3.6V$ over an operating ambient temp. $-40^{\circ}C \leq T_A \leq 85^{\circ}C$; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are for $T_A = 25^{\circ}C$.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------------------|---|--|-----------------------------|------|------|------|------|
| INPUT | | | | | | | |
| V _{IN} | Input voltage range at VIN, AVIN | | | 2.5 | | 5.5 | V |
| V _{DD} | I ² C and registers supply voltage range | | | 1.15 | | 3.6 | V |
| I _{SD(AVIN)} | Shutdown current into AVIN | EN = LOW, V _{DD} = 0V | | | 0.65 | 5 | μA |
| I _{SD(VIN)} | Shutdown current into VIN | EN = LOW, V _{DD} = 0V | T _A = 25°C | | 0.5 | 1 | μA |
| | | | T _A = 85°C | | 1 | 3 | μA |
| I _{SD(VDD)} | Shutdown current into VDD | EN = LOW, I ² C bus idle | | | 0.01 | | μA |
| I _Q | Operating quiescent current into (AVIN + VIN) | EN = HIGH, I _{OUT} = 0mA, not switching | PFM mode | | 56 | | μA |
| | | | Forced PWM mode (Test Mode) | | 180 | | μA |
| V _{UVLO} | Under voltage lock out at AVIN | Input voltage falling, EN = High | | | 2.3 | 2.45 | V |
| | | Input voltage rising, EN = Low | | | 1.3 | | V |
| V _{UVLO,HYST(AVIN)} | Under voltage lock out hysteresis at AVIN | Input voltage rising | | | 110 | | mV |
| V _{DD,UVLO} | Under voltage lock out at VDD | Input voltage falling | | 0.7 | 0.92 | 1.1 | V |

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted the specification applies for $V_{IN} = 3.6V$ over an operating ambient temp. $-40^{\circ}C \leq T_A \leq 85^{\circ}C$; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are for $T_A = 25^{\circ}C$.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|---|--|--|----------------------|-------|-------|-------|
| V _{UVLO,HYST} (V _D) | Under voltage lock out hysteresis at VDD | Input voltage rising | | 50 | | | mV |
| LOGIC INTERFACE | | | | | | | |
| V _{IH} | High-level input voltage at EN, VSEL0, VSEL1 | | | 1.2 | | | V |
| V _{IL} | Low-level input voltage at EN, VSEL0, VSEL1 | | | 0.4 | | | V |
| t _{rf} | Signal transition time at EN, VSEL0, VSEL1 | rising and falling edge | | 30 | | | mV/μs |
| V _{IH,I2C} | High-level input voltage at SCL, SDA | | | 0.7x V _{DD} | | | V |
| V _{IL,I2C} | Low-level input voltage at SCL, SDA | | | 0.3x V _{DD} | | | V |
| I _{LKG} | Logic input leakage current at EN, VSEL0, VSEL1, SDA, SCL | Internal pulldown resistors disabled | | 0.05 | | | μA |
| R _{PD} | Pull down resistance at EN, VSEL0, VSEL1 | Internal pulldown resistors enabled | | 300 | | | kΩ |
| I ² C clock frequency | | Fast mode | | 400 | | | kHz |
| | | High speed mode | | 3.4 | | | MHz |
| POWER SWITCH | | | | | | | |
| R _{DS(on)} | High side MOSFET switch | V _{IN} = 3.6V | | 25 | 44 | 75 | mΩ |
| | Low side MOSFET switch | V _{IN} = 3.6V | | 25 | 32 | 50 | mΩ |
| I _{LIMF} | High side MOSFET forward current limit | V _{IN} = 3.6V | | 3.0 | 3.6 | 4.3 | A |
| | Low side MOSFET forward current limit | V _{IN} = 3.6V | | 2.6 | 3 | 3.8 | A |
| | Low side MOSFET negative current limit | V _{IN} = 3.6V, PWM mode | | 2.2 | 2.5 | 2.9 | A |
| f _{SW} | Nominal switching frequency | PWM mode | | 2.5 | | | MHz |
| T _{JEW} | Die temperature early warning | | | 120 | | | °C |
| T _{JSD} | Thermal shutdown | | | 150 | | | °C |
| T _{JSD,HYST} | Thermal shutdown hysteresis | | | 20 | | | °C |
| t _{ON,min} | Minimum on time | | | 120 | | | ns |
| OUTPUT | | | | | | | |
| V _{OUT} | Output voltage range | 10mV increments | TPS62360/62 | 0.77 | 1.4 | | V |
| | | | TPS62361B | 0.5 | 1.77 | | |
| Output voltage accuracy | | TPS62360/62: V _{IN} = 2.5V .. 5.5V V _{OUT} = 0.77V .. 1.4V TPS62361B: V _{IN} = 2.7V .. 5.5V V _{OUT} = 0.5V .. 1.77V | No load, Forced PWM, V _{OUT} = [0.77V, 1.3V] T _J = 85°C | -0.5% | | +0.5% | |
| | | | No load, Forced PWM, T _J = -40 .. 150°C | -1% | ±0.5% | +1% | |
| Line regulation | | I _{OUT} = 1A, forced PWM | | < 0.1 | | | %/V |
| Load regulation | | V _{OUT} = 1.2V, forced PWM | | < 0.05 | | | %/A |
| t _{Start} | Start-up time | Time from active EN to V _{OUT} = 1.4V, C _{OUT} < 100μF, RMP[2:0] = 000, I _{OUT} = 0mA | | 1 | | | ms |
| R _{Sense} | Input resistance between Sense+, Sense– | | | 2.2 | | | MΩ |

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted the specification applies for VIN = 3.6V over an operating ambient temp. $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are for $T_A = 25^{\circ}\text{C}$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|-----------------|-----|------|-----|-------|
| Ramp timer | RMP[2:0] = 000 | | 32 | | mV/μs |
| | RMP[2:0] = 001 | | 16 | | |
| | RMP[2:0] = 010 | | 8 | | |
| | RMP[2:0] = 011 | | 4 | | |
| | RMP[2:0] = 100 | | 2 | | |
| | RMP[2:0] = 101 | | 1 | | |
| | RMP[2:0] = 110 | | 0.5 | | |
| | RMP[2:0] = 111 | | 0.25 | | |

I²C INTERFACE TIMING REQUIREMENTS⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-------------------|---|--|----------------|------|---------------|
| $f_{(SCL)}$ | SCL clock frequency | Standard mode | | 100 | kHz |
| | | Fast mode | | 400 | kHz |
| | | High-speed mode (write operation), $C_B - 100\text{ pF max}$ | | 3.4 | MHz |
| | | High-speed mode (read operation), $C_B - 100\text{ pF max}$ | | 3.4 | MHz |
| | | High-speed mode (write operation), $C_B - 400\text{ pF max}$ | | 1.7 | MHz |
| | | High-speed mode (read operation), $C_B - 400\text{ pF max}$ | | 1.7 | MHz |
| t_{BUF} | Bus free time between a STOP and START condition | Standard mode | 4.7 | | μs |
| | | Fast mode | 1.3 | | μs |
| t_{HD}, t_{STA} | Hold time (repeated) START condition | Standard mode | 4 | | μs |
| | | Fast mode | 600 | | ns |
| | | High-speed mode | 160 | | ns |
| t_{LOW} | Low period of the SCL clock | Standard mode | 4.7 | | μs |
| | | Fast mode | 1.3 | | μs |
| | | High-speed mode, $C_B - 100\text{ pF max}$ | 160 | | ns |
| | | High-speed mode, $C_B - 400\text{ pF max}$ | 320 | | ns |
| t_{HIGH} | High period of the SCL clock | Standard mode | 4 | | μs |
| | | Fast mode | 600 | | ns |
| | | High-speed mode, $C_B - 100\text{ pF max}$ | 60 | | ns |
| | | High-speed mode, $C_B - 400\text{ pF max}$ | 120 | | ns |
| t_{SU}, t_{STA} | Setup time for a repeated START condition | Standard mode | 4.7 | | μs |
| | | Fast mode | 600 | | ns |
| | | High-speed mode | 160 | | ns |
| t_{SU}, t_{DAT} | Data setup time | Standard mode | 250 | | ns |
| | | Fast mode | 100 | | ns |
| | | High-speed mode | 10 | | ns |
| t_{HD}, t_{DAT} | Data hold time | Standard mode | 0 | 3.45 | μs |
| | | Fast mode | 0 | 0.9 | μs |
| | | High-speed mode, $C_B - 100\text{ pF max}$ | 0 | 70 | ns |
| | | High-speed mode, $C_B - 400\text{ pF max}$ | 0 | 150 | ns |
| t_{RCL} | Rise time of SCL signal | Standard mode | $20 + 0.1 C_B$ | 1000 | ns |
| | | Fast mode | $20 + 0.1 C_B$ | 300 | ns |
| | | High-speed mode, $C_B - 100\text{ pF max}$ | 10 | 40 | ns |
| | | High-speed mode, $C_B - 400\text{ pF max}$ | 20 | 80 | ns |
| t_{RCL1} | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | Standard mode | $20 + 0.1 C_B$ | 1000 | ns |
| | | Fast mode | $20 + 0.1 C_B$ | 300 | ns |
| | | High-speed mode, $C_B - 100\text{ pF max}$ | 10 | 80 | ns |
| | | High-speed mode, $C_B - 400\text{ pF max}$ | 20 | 160 | ns |
| t_{FCL} | Fall time of SCL signal | Standard mode | $20 + 0.1 C_B$ | 300 | ns |
| | | Fast mode | $20 + 0.1 C_B$ | 300 | ns |
| | | High-speed mode, $C_B - 100\text{ pF max}$ | 10 | 40 | ns |
| | | High-speed mode, $C_B - 400\text{ pF max}$ | 20 | 80 | ns |

(1) S/M = standard mode; F/M = fast mode

(2) Specified by design. Not tested in production.

I²C INTERFACE TIMING REQUIREMENTS⁽¹⁾⁽²⁾ (continued)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------------------------|---------------------------------|--|-------------------------|------|------|
| t _{RDA} | Rise time of SDA signal | Standard mode | 20 + 0.1 C _B | 1000 | ns |
| | | Fast mode | 20 + 0.1 C _B | 300 | ns |
| | | High-speed mode, C _B – 100 pF max | 10 | 80 | ns |
| | | High-speed mode, C _B – 400 pF max | 20 | 160 | ns |
| t _{FDA} | Fall time of SDA signal | Standard mode | 20 + 0.1 C _B | 300 | ns |
| | | Fast mode | 20 + 0.1 C _B | 300 | ns |
| | | High-speed mode, C _B – 100 pF max | 10 | 80 | ns |
| | | High-speed mode, C _B – 400 pF max | 20 | 160 | ns |
| t _{SU} , t _{STO} | Setup time for STOP condition | Standard mode | 4 | | μs |
| | | Fast mode | 600 | | ns |
| | | High-speed mode | 160 | | ns |
| C _B | Capacitive load for SDA and SCL | | 400 | | pF |

I²C TIMING DIAGRAMS

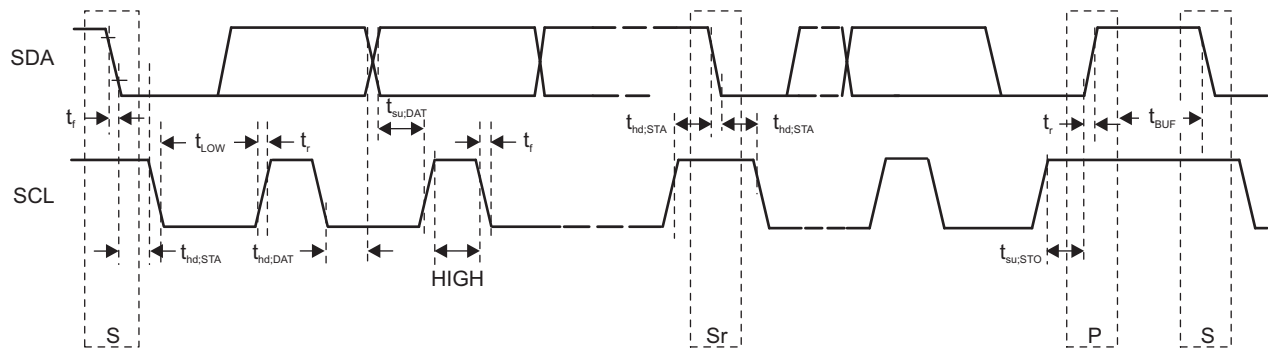
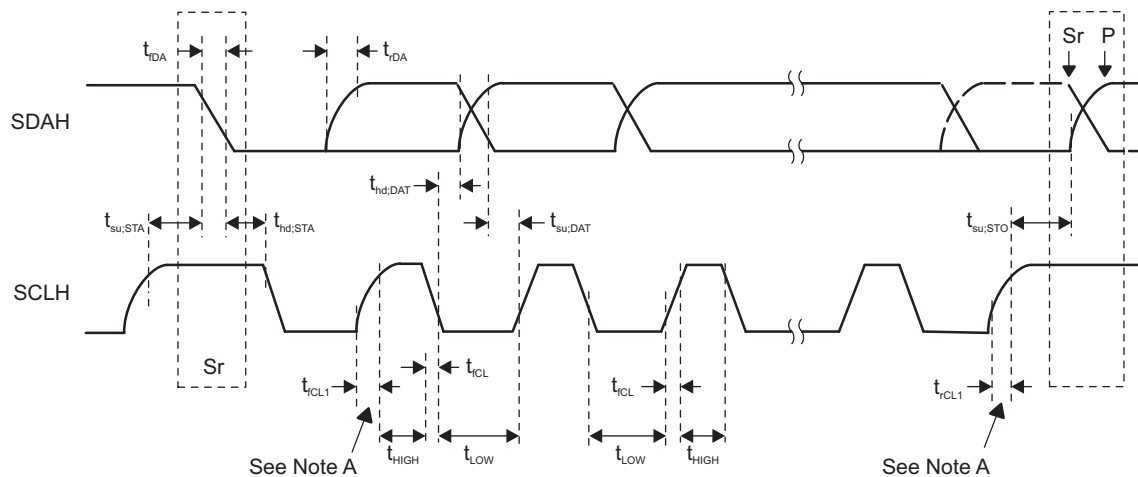



Figure 1. Serial Interface Timing for F/S Mode



 = MCS Current Source Pull-Up

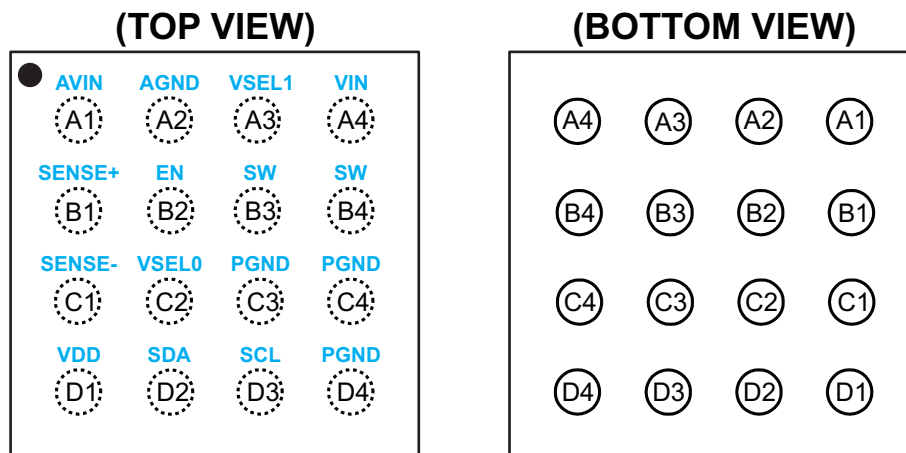
 = $R_{(P)}$ Resistor Pull-Up

Note A: First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 2. Serial Interface Timing for H/S Mode

DEVICE INFORMATION

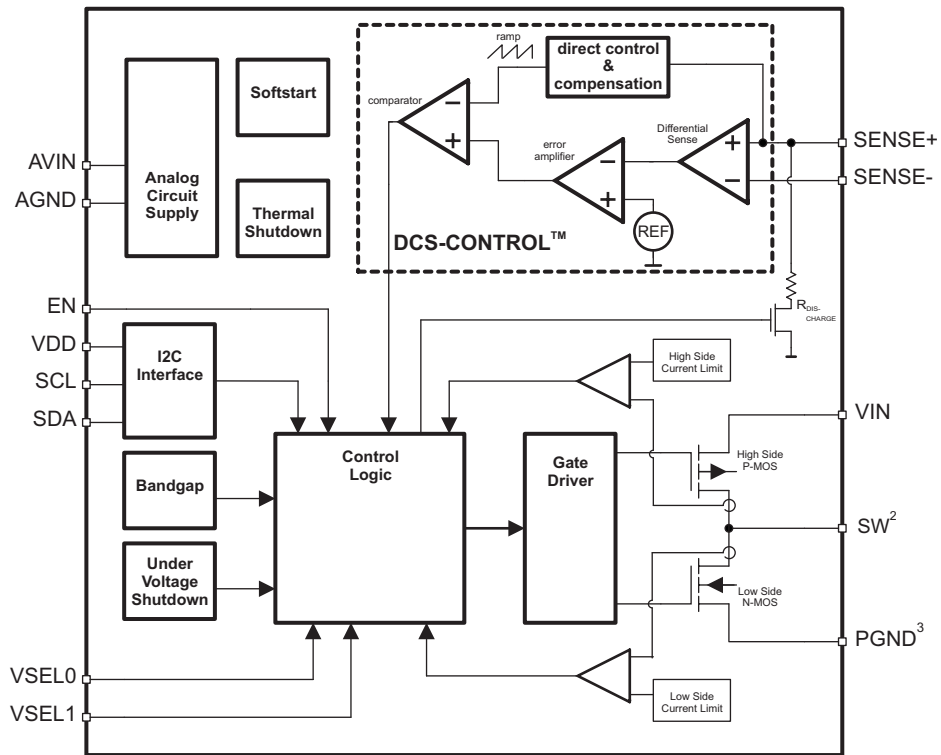
PIN ASSIGNMENTS



PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|--------|----------|-----|---|
| NAME | NO. | | |
| AVIN | A1 | I | Analog Supply Voltage Input. |
| AGND | A2 | – | Analog Ground Connection. |
| EN | B2 | I | Device Enable Logic Input. Logic HIGH enables the device, logic LOW disables the device and turns it into shutdown. The pin must be terminated to either HIGH or LOW if the internal pull down resistor is deactivated. |
| VDD | D1 | I | I ² C Logic and Registers supply voltage. For resetting the internal registers, this connection must be pulled below its UVLO level. |
| SCL | D3 | I/O | I ² C clock signal. |
| SDA | D2 | I/O | I ² C data signal. |
| VSEL0 | C2 | I | Output Settings Selection Logic Inputs. Predefined register settings can be chosen for setting output voltage and mode. The pins must be terminated to logic HIGH or LOW if the internal pull down resistors are deactivated. |
| VSEL1 | A3 | I | |
| SW | B3 B4 | – | |
| SENSE+ | B1 | I | Positive Output Voltage Remote Sense. Must be connected closest to the load supply node. |
| SENSE– | C1 | I | Negative Output Voltage Remote Sense. Must be connected closest to the load ground node. |
| VIN | A4 | I | Power Supply Voltage Input. |
| PGND | C3 | – | Power Ground Connection. |
| | C4 | | |
| | D4 | | |

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Table of Graphs

| | | | FIGURE |
|-----------------------------|--|---|--|
| η | Efficiency | vs. Output Current (Power Save and Forced PWM Mode) | $V_{OUT} = 1.5V$ Figure 3 |
| | | | $V_{OUT} = 1.4V$ Figure 4 |
| | | | $V_{OUT} = 1.2V$ Figure 5 |
| | | | $V_{OUT} = 1.1V$ Figure 6 |
| | | | $V_{OUT} = 1.0V$ Figure 7 |
| | | | $V_{OUT} = 0.9V$ Figure 8 |
| | | | $V_{OUT} = 0.6V$ Figure 9 |
| | vs. Input Voltage (Power Save and Forced PWM Mode) | | $I_{OUT} = 3000mA$ Figure 10 |
| | | | $I_{OUT} = 1000mA$ Figure 11 |
| | | | $I_{OUT} = 100mA$ Figure 12 |
| | | | $I_{OUT} = 10mA$ Figure 13 |
| V_O | DC Output Voltage | vs. Output Current (Power Save and Forced PWM Mode) | $V_{OUT} = 1.5V, T_A = 25^\circ C$ Figure 14 |
| | | | $V_{OUT} = 1.2V, T_A = 25^\circ C$ Figure 15 |
| | | | $V_{OUT} = 0.9V, T_A = 25^\circ C$ Figure 16 |
| | | | $V_{OUT} = 0.6V, T_A = 25^\circ C$ Figure 17 |
| | Startup | Into No Load | $V_{OUT} = 0.5V, I_{OUT} = 0mA$ Figure 18 |
| | | | $V_{OUT} = 1.5V, I_{OUT} = 0mA$ Figure 19 |
| | | Into Load | $V_{OUT} = 0.5V, I_{OUT} = 1000mA$ Figure 20 |
| | | | $V_{OUT} = 1.5V, I_{OUT} = 1000mA$ Figure 21 |
| | Switching Wave forms | | $I_{OUT} = 10mA$ Figure 22 |
| | | | $I_{OUT} = 200mA$ Figure 23 |
| | | | $I_{OUT} = 1000mA$ Figure 24 |
| | | | $I_{OUT} = 3000mA$ Figure 25 |
| | Output Voltage Ramp Control | Transition 0.6V .. 1.5V | $I_{OUT} = 0mA$ Figure 26 |
| | | | $I_{OUT} = 1000mA$ Figure 27 |
| | Load Transient Response | | $I_{OUT} = 5mA$ to 200mA Figure 28 |
| | | | $I_{OUT} = 5mA$ to 1000mA Figure 29 |
| | | | $I_{OUT} = 200mA$ to 1000mA Figure 30 |
| | | | $I_{OUT} = 1000mA$ to 3000mA Figure 31 |
| | Line Transient Response | | $V_{IN} = 3.2$ to 4.2V Figure 32 |
| $I_{SD(VIN)}, I_{SD(AVIN)}$ | Shutdown Current at AVIN and VIN | vs. Input Voltage | $T_A = [-40^\circ C, 25^\circ C, 125^\circ C]$ Figure 33 |
| I_Q | Quiescent Current | vs. Input Voltage | $T_A = [-40^\circ C, 25^\circ C, 125^\circ C]$, auto PFM/PWM Figure 34 |
| | | | $T_A = [-40^\circ C, 25^\circ C, 125^\circ C]$ forced PWM Figure 35 |
| f_{SW} | Switching Frequency | vs. Output Current | $V_{OUT} = 1.2V$ Figure 36 |
| I_{LIM} | Current Limit | vs. Input Voltage | Figure 37 |

TYPICAL CHARACTERISTICS (continued)

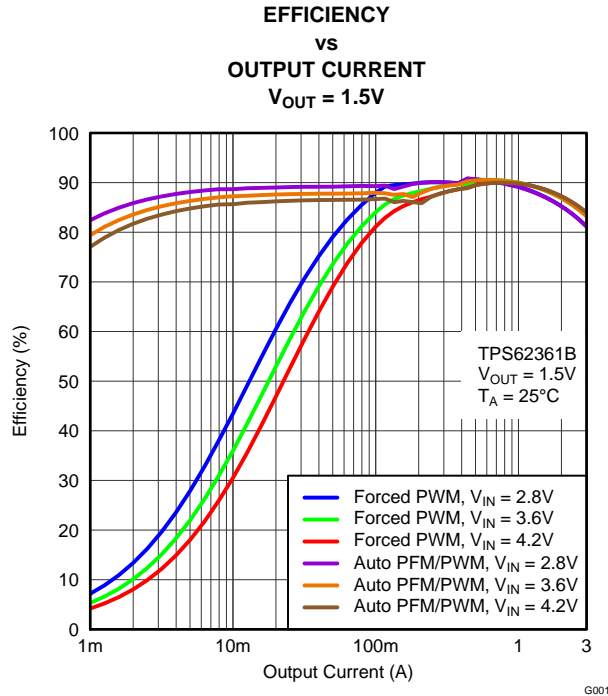


Figure 3.

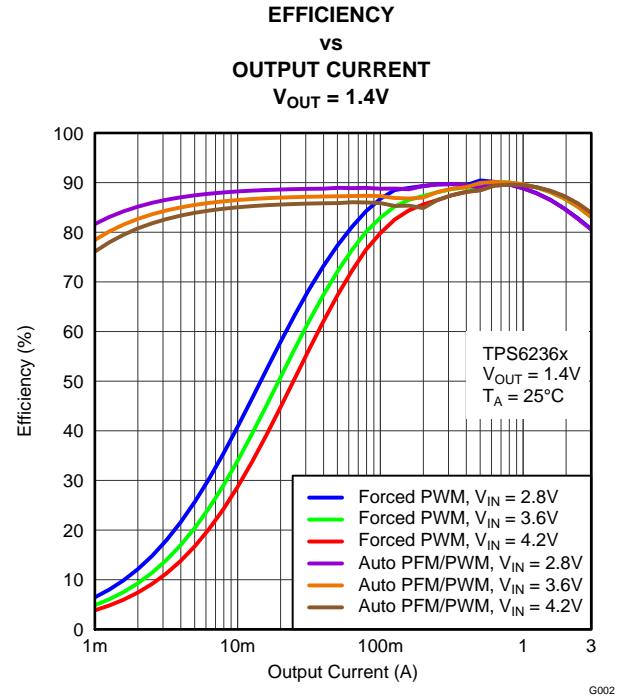


Figure 4.

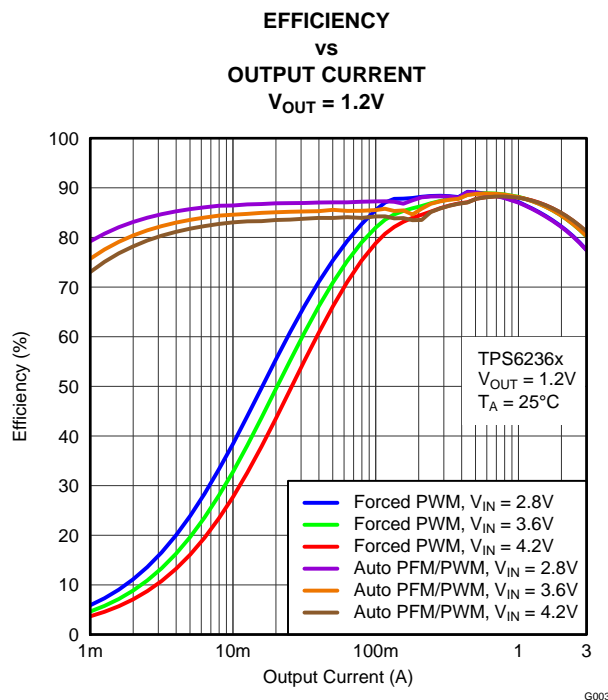


Figure 5.

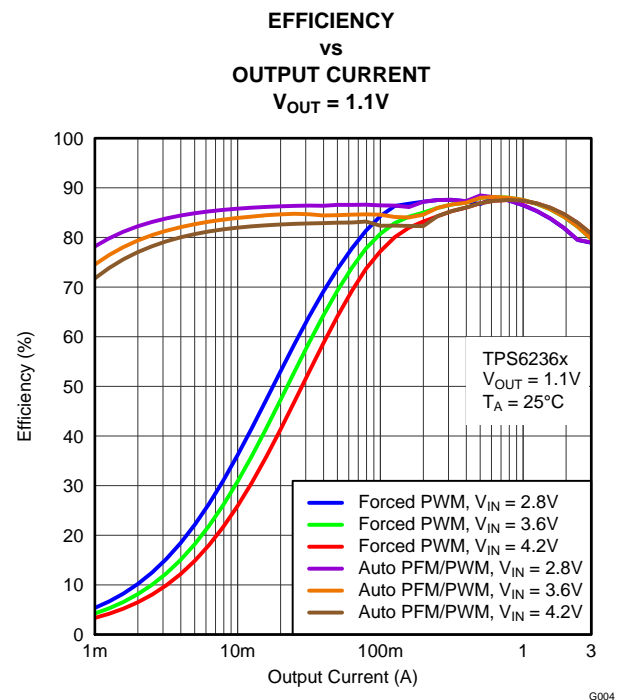


Figure 6.

TYPICAL CHARACTERISTICS (continued)

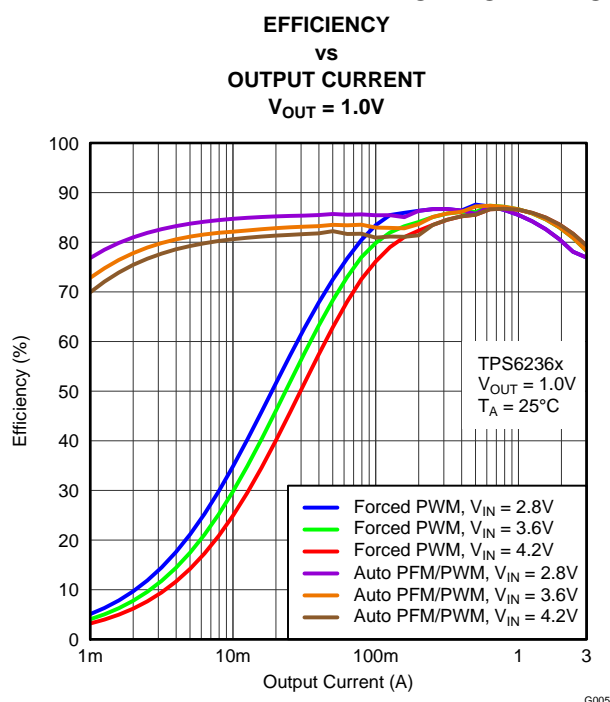


Figure 7.

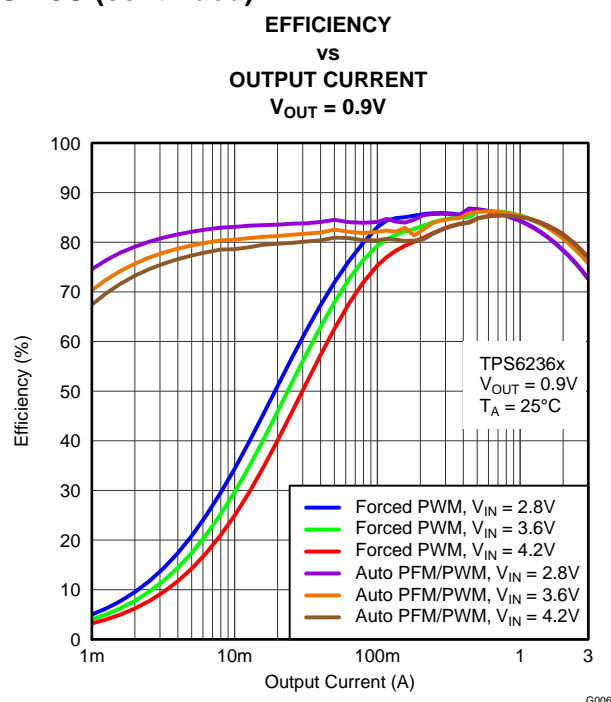


Figure 8.

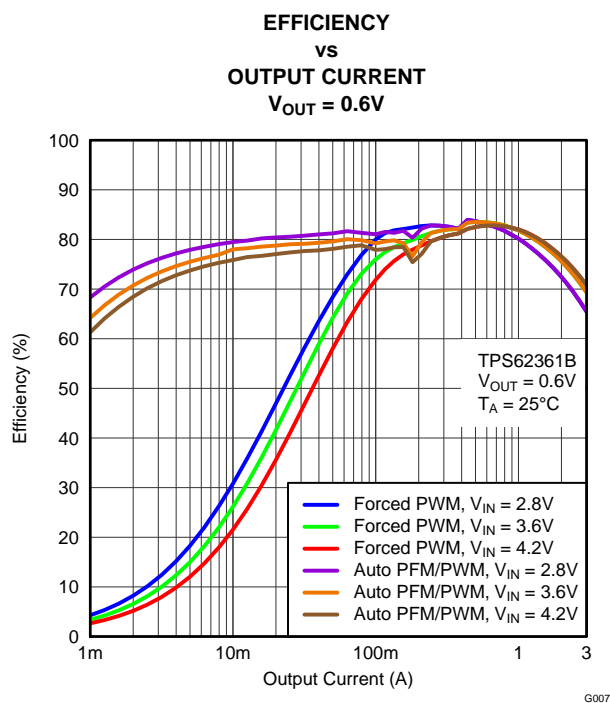


Figure 9.

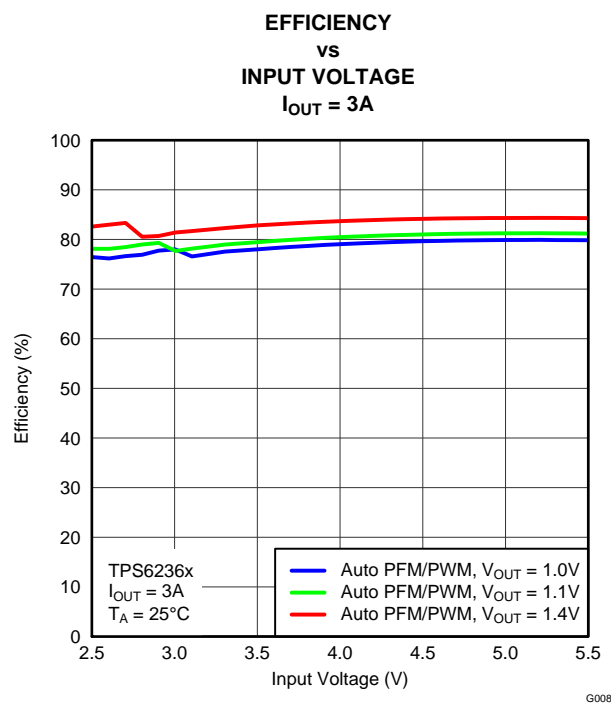


Figure 10.

TYPICAL CHARACTERISTICS (continued)

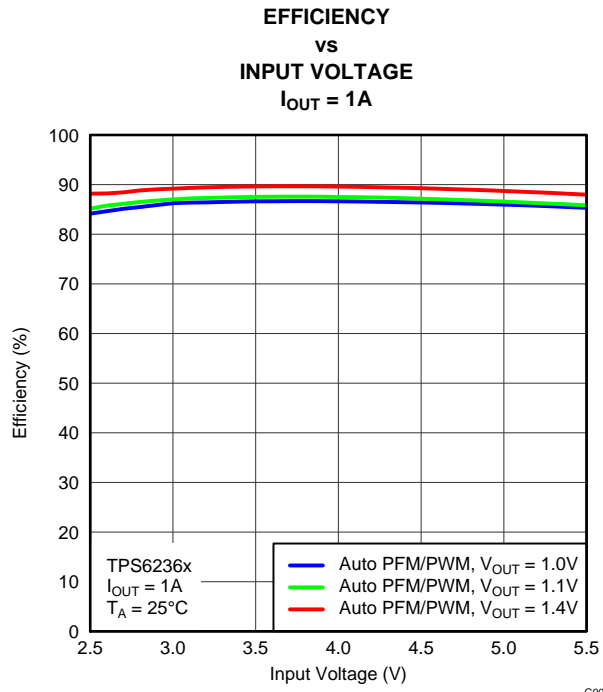


Figure 11.

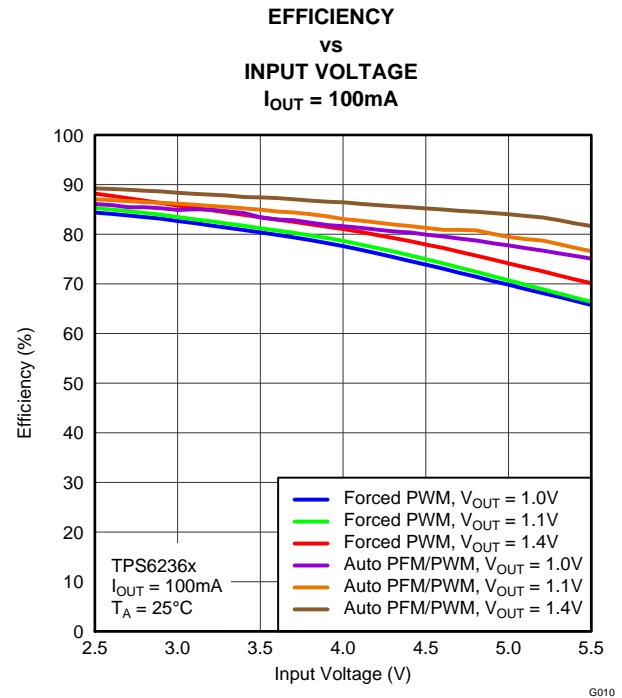


Figure 12.

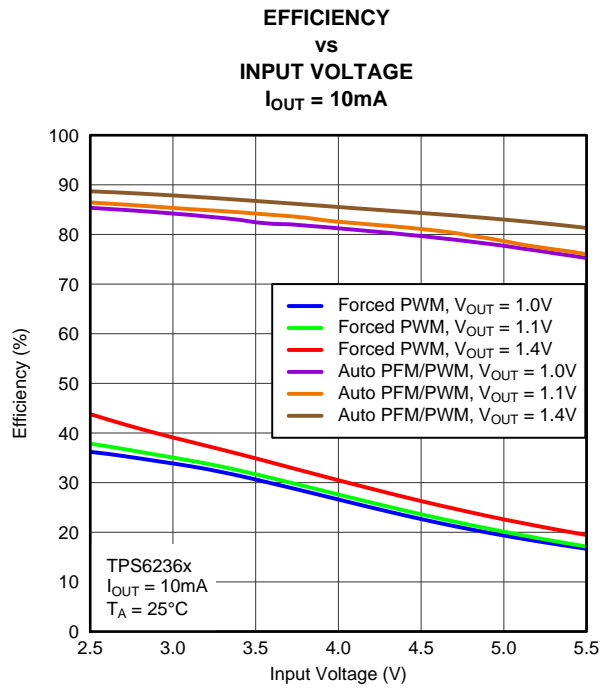


Figure 13.

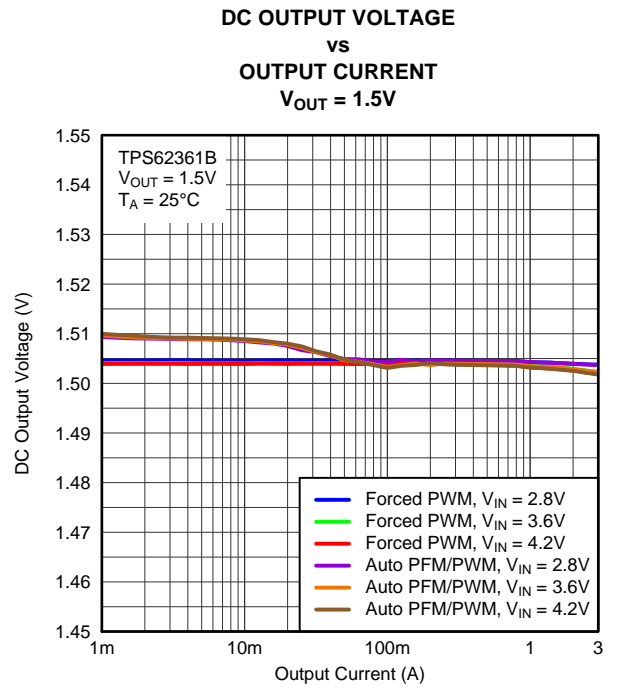


Figure 14.

TYPICAL CHARACTERISTICS (continued)

**DC OUTPUT VOLTAGE
vs
OUTPUT CURRENT
 $V_{OUT} = 1.2V$**

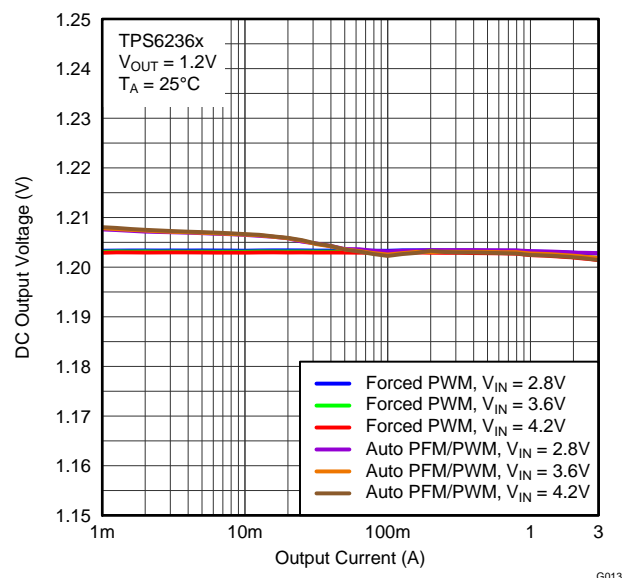


Figure 15.

**DC OUTPUT VOLTAGE
vs
OUTPUT CURRENT
 $V_{OUT} = 0.9V$**

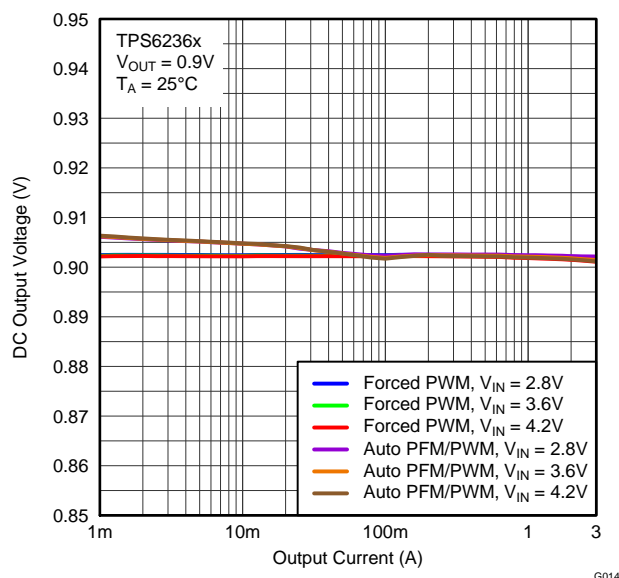


Figure 16.

**DC OUTPUT VOLTAGE
vs
OUTPUT CURRENT
 $V_{OUT} = 0.6V$**

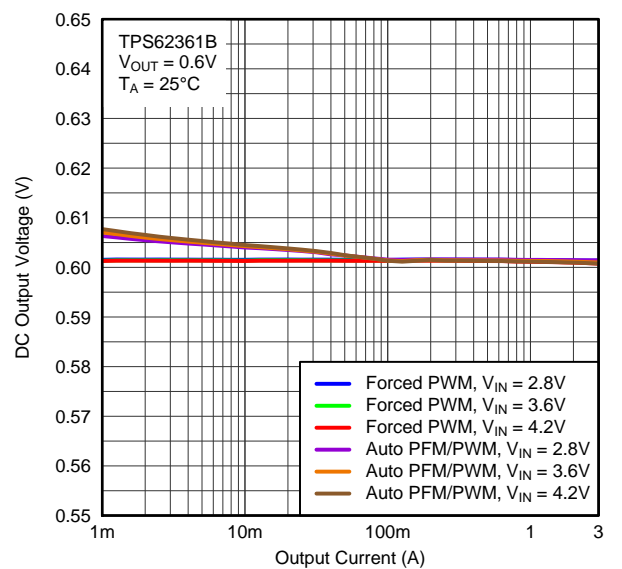


Figure 17.

**STARTUP INTO NO LOAD
 $V_{OUT} = 0.5V$**

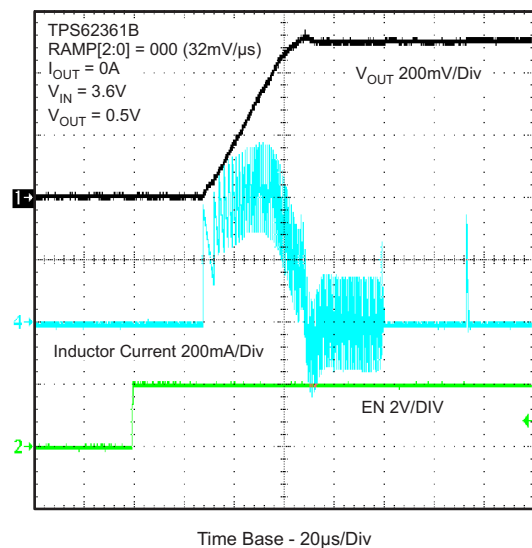


Figure 18.

TYPICAL CHARACTERISTICS (continued)

STARTUP INTO NO LOAD

$V_{OUT} = 1.5V$

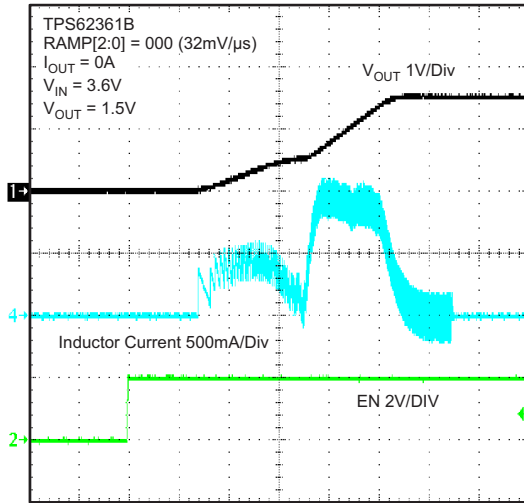


Figure 19.

STARTUP INTO LOAD

$V_{OUT} = 0.5V$

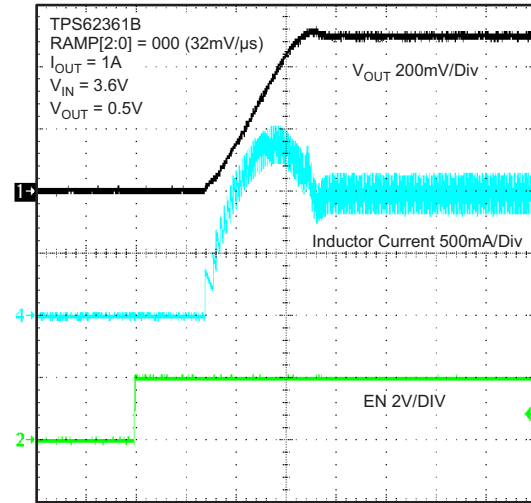


Figure 20.

STARTUP INTO LOAD

$V_{OUT} = 1.5V$

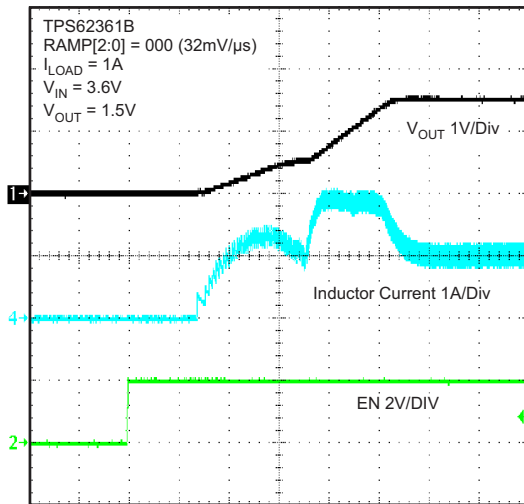


Figure 21.

SWITCHING WAVE FORMS

$I_{OUT} = 10mA$

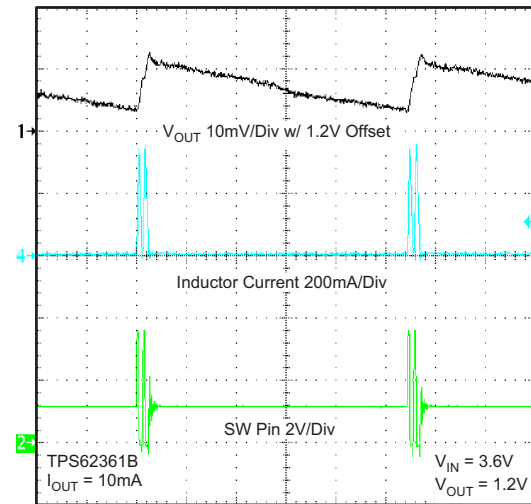
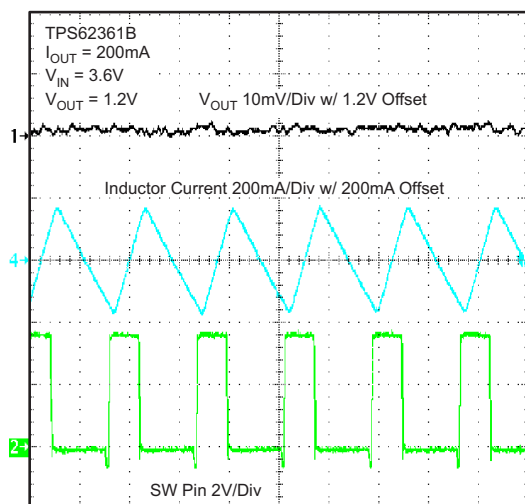


Figure 22.

TYPICAL CHARACTERISTICS (continued)

SWITCHING WAVE FORMS

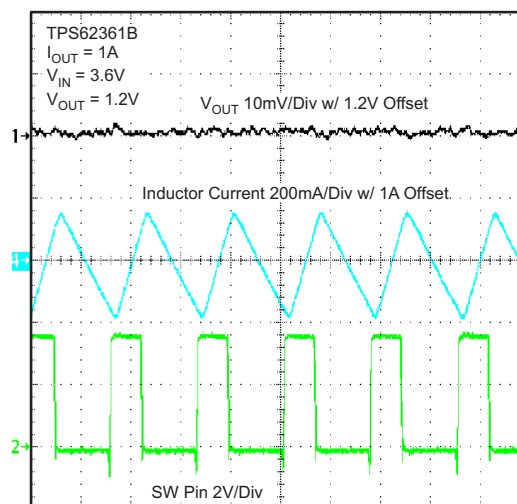
 $I_{OUT} = 200\text{mA}$


Time Base - 250ns/Div

G022

Figure 23.

SWITCHING WAVE FORMS

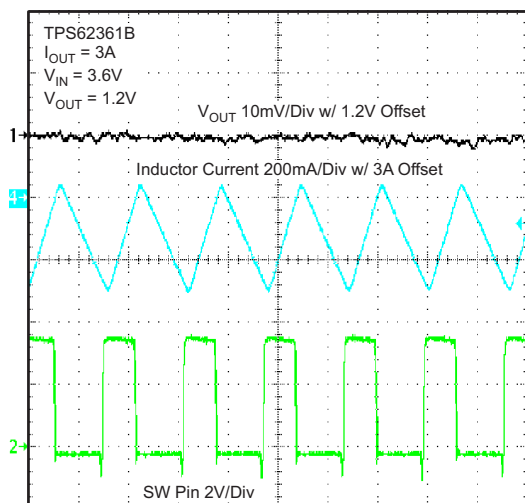
 $I_{OUT} = 1\text{A}$


Time Base - 250ns/Div

G023

Figure 24.

SWITCHING WAVE FORMS

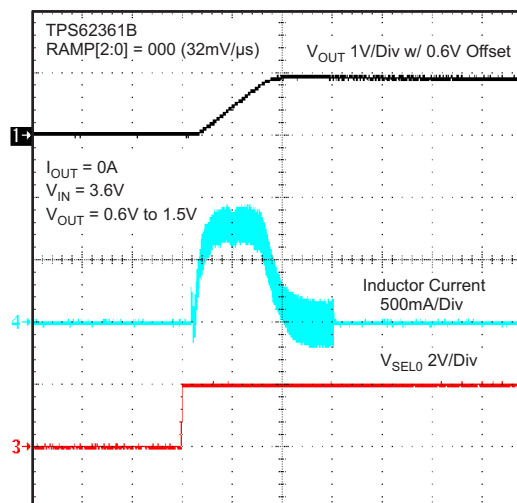
 $I_{OUT} = 3\text{A}$


Time Base - 250ns/Div

G024

Figure 25.

OUTPUT VOLTAGE RAMP CONTROL NO LOAD



Time Base - 20μs/Div

G025

Figure 26.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE RAMP CONTROL

$I_{OUT} = 1A$

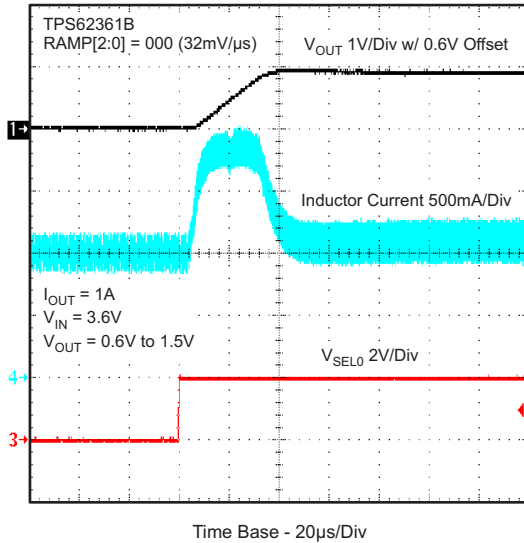


Figure 27.

LOAD TRANSIENT RESPONSE

I_{OUT} RANGE: 5mA to 200mA

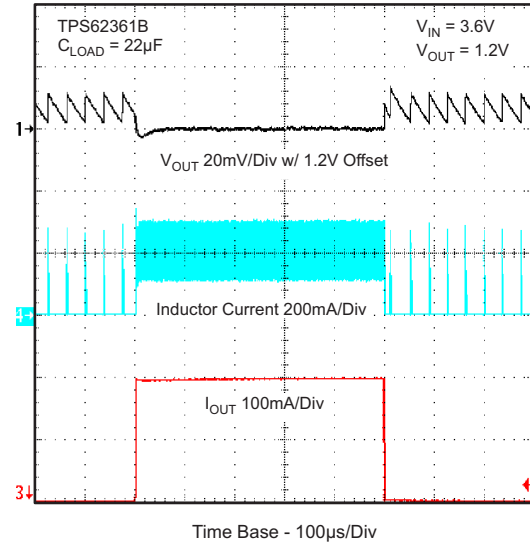


Figure 28.

LOAD TRANSIENT RESPONSE

I_{OUT} RANGE: 5mA to 1A

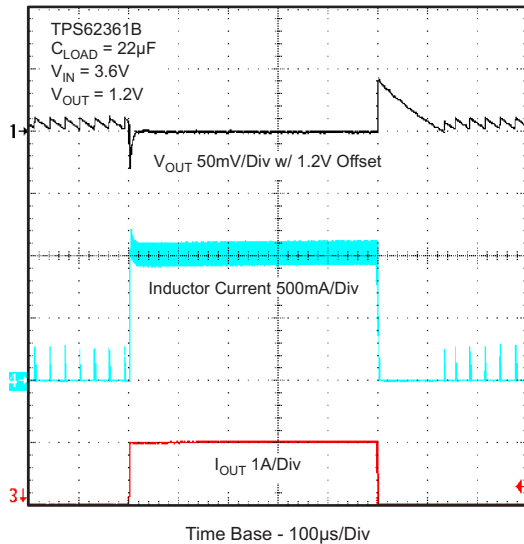


Figure 29.

LOAD TRANSIENT RESPONSE

I_{OUT} RANGE: 200mA to 1A

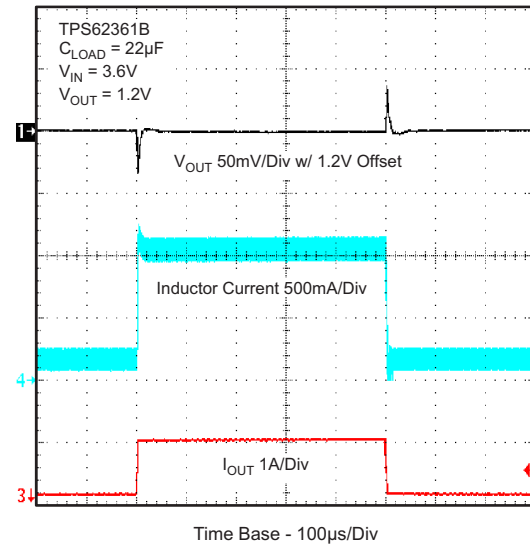
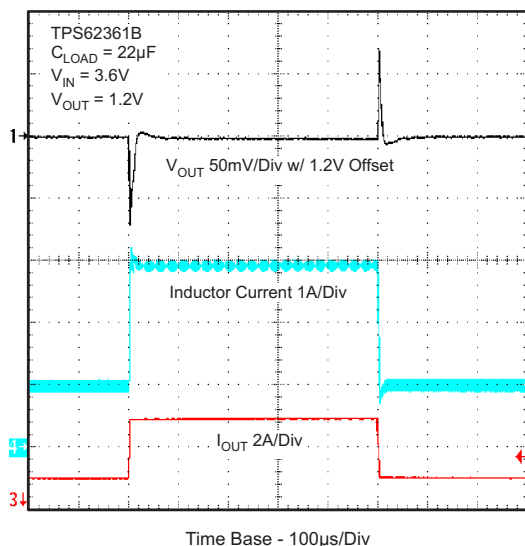
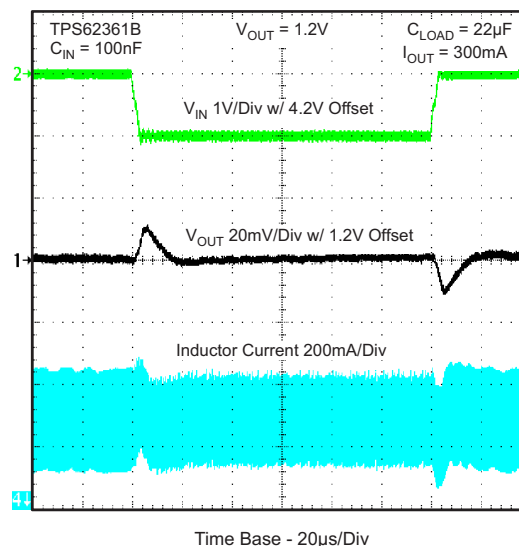
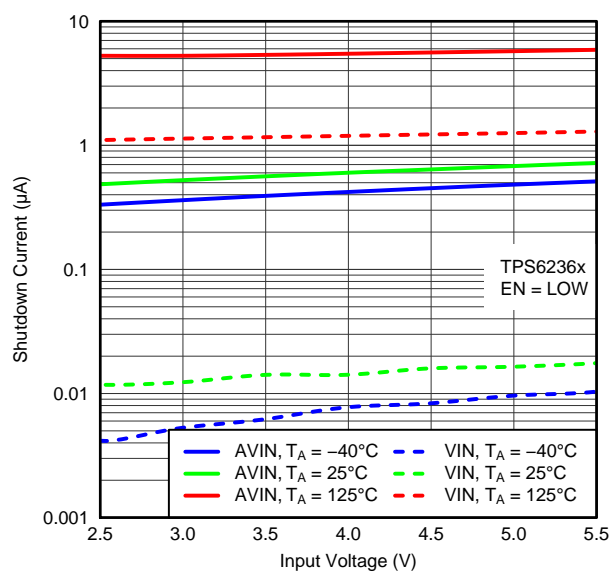
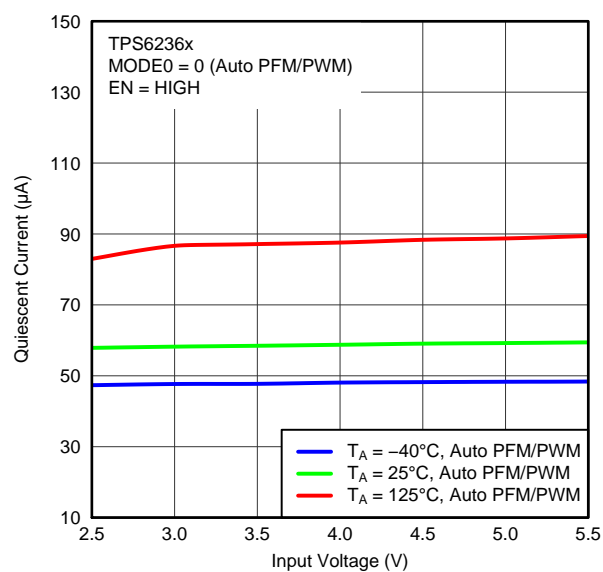


Figure 30.

TYPICAL CHARACTERISTICS (continued)**LOAD TRANSIENT RESPONSE**
I_{OUT} RANGE: 1A to 3A**Figure 31.****LINE TRANSIENT RESPONSE**
V_{IN} RANGE: 4.2V to 3.2V**Figure 32.****SHUTDOWN CURRENT**
vs
INPUT VOLTAGE**Figure 33.****QUIESCENT CURRENT**
vs
INPUT VOLTAGE**Figure 34.**

TYPICAL CHARACTERISTICS (continued)

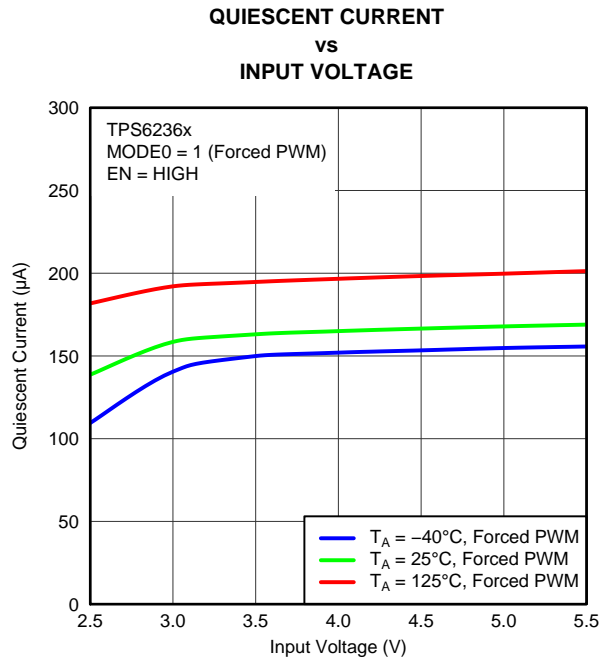


Figure 35.

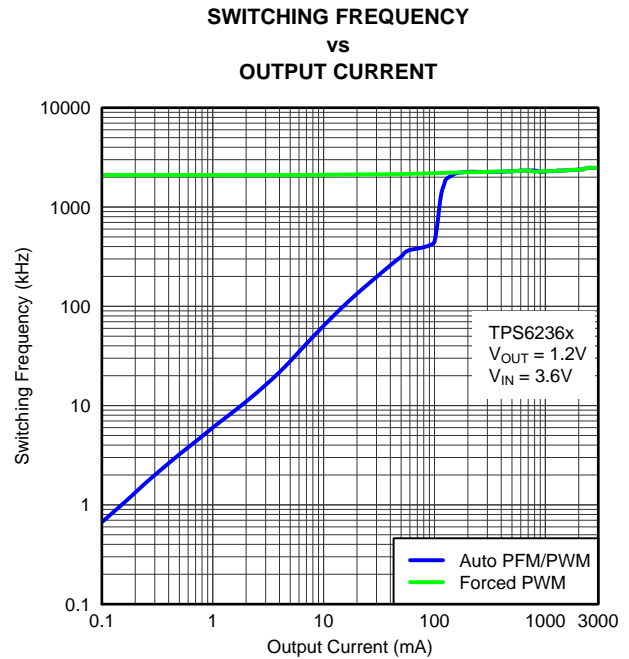


Figure 36.

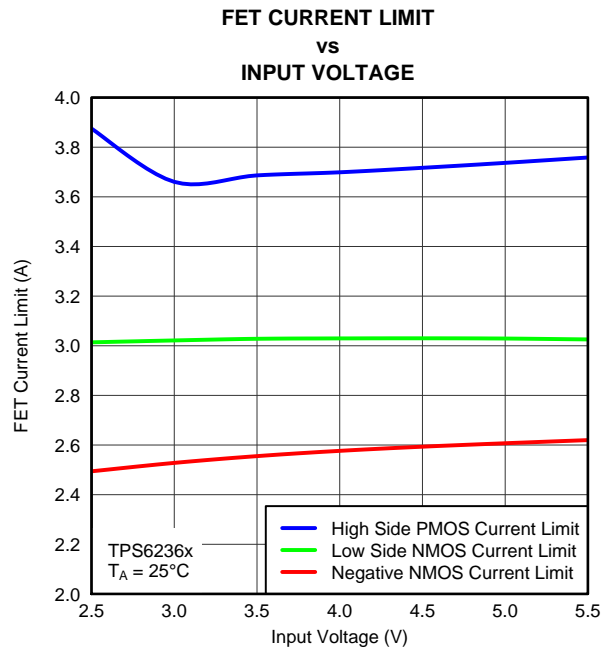


Figure 37.

PARAMETER MEASUREMENT INFORMATION

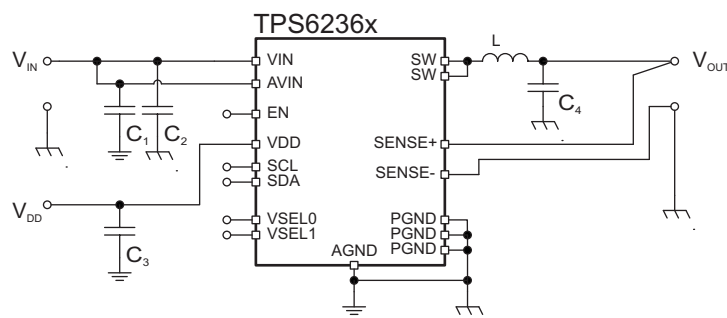


Table 1. List of Components

| REFERENCE | DESCRIPTION | MANUFACTURER |
|---------------------------------|---|------------------------------|
| TPS6236x | 3A Processor Supply with I ² C Compatible Interface and Remote Sense | Texas Instruments |
| L | 1 μ H, 4 mm x 4 mm x 2.1 mm | Coilcraft (XFL4020-102ME1.0) |
| C ₂ , C ₄ | 10 μ F, Ceramic, 6.3V, X5R | Murata (GRM188R60J106ME84D) |
| C ₁ , C ₃ | 0.1 μ F, Ceramic, 10V, X5R | Standard |

DETAILED DESCRIPTION

The TPS6236x are a family of high-frequency synchronous step down dc-dc converter optimized for battery-powered portable applications. With an input voltage range of 2.5V to 5.5V, common battery technologies are supported.

The device provides up to 3A peak load current, operating at 2.5MHz typical switching frequency.

The devices convert to an output voltage range of 0.77V to 1.4V (TPS62360 / TPS62362) and 0.5V to 1.77V (TPS62361B), programmable via I²C interface in 10mV steps.

The TPS6236x supports low-voltage DSPs and processor cores in smart-phones and handheld computers, including latest submicron processes and their retention modes and addresses digital voltage scaling technologies such as SmartReflex™.

Output Voltages and Modes can be fully programmed via I²C. To address different performance operating points and/or startup conditions, the device offers four output voltage / mode presets which can be chosen via dedicated hardware input pins allowing simple and zero latency output voltage transition.

The devices focus on a high output voltage accuracy. The fully differential sensing and the DCS-Control™ architecture achieve precise static and dynamic, transient output voltage regulation. This accounts for stable processor operation. Output voltage security margins can be kept small, resulting in an increased overall system efficiency.

The TPS6236x devices offer high efficiency step down conversion. The area of highest efficiency is extended towards low output currents to increase the efficiency while the processor is operating in retention mode, as well as towards highest output currents reducing the power loss. This addresses the power profile of processors. High efficiency conversion is required for low output currents to support the retention modes of processors, resulting in an increased battery on-time. To address the processor maximum performance operating points with highest output currents, high efficiency conversion is enabled as well to save the battery on-time and reduce input power.

The robust architecture and multiple safety features allow perfect system integration.

The 2mm x 2mm package and the low number of required external components lead to a tiny solution size of approximately 27.5 mm².

OPERATION

The TPS6236x synchronous switched mode power converters are based on DCS-Control™, an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control architectures.

While a comparator stage provides excellent load transient response, an additional voltage loop ensures high DC accuracy as well. The TPS6236x compensates ground shifts at the load by the differentially sensing the output voltage at the point of load.

The internal ramp generator adds information about the load current and fast output voltage changes. The internally compensated regulation network achieves fast and stable operation with low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5MHz with a controlled frequency variation depending on the input voltage. As the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to light loads. The transition from PWM to Power Save Mode is seamless and avoids output voltage transients.

An internal current limit supports nominal output currents of up to 3A. The TPS6236x family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

ENABLING AND DISABLING THE DEVICE

The device is enabled by setting the EN input to a logic high. Accordingly, a logic low disables the device. If the device is enabled, the internal power stage will start switching and regulate the output voltage to the programmed threshold. The EN input must be terminated unless the internal pull down resistor is activated.

The I²C interface is operable when VDD and AVIN are present, regardless of the state of the EN pin.

If the device is disabled by pulling the EN to a logic low, the output capacitor can actively be discharged. Per default, this feature is disabled. Programming the EN_DISC bit to a logic high will discharge the output capacitor via a typ. 300Ω path on the SENSE+ pin.

SOFT START

The device incorporates an internal soft start circuitry that controls the ramp up of the output voltage after enabling the device. This circuitry eliminates inrush current to avoid excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

During soft start, the output voltage is monotonically ramped up to the minimum programmable output voltage. After reaching this threshold, the output voltage is further increased following the slope as programmed in the ramp rate settings (see [RAMP RATE CONTROLLING](#)) until reaching the programmed output voltage. Once the nominal voltage is reached, regular operation as described above will continue.

The device is able to start into a pre biased output capacitor as well.

PROGRAMMING THE OUTPUT

The TPS6236x devices offer four similar registers to program the output. Two dedicated hardware input pins, VSEL0 and VSEL1, are implemented for choosing the active register. The logic state of VSEL0 and VSEL1 select the register whose settings are present at the output. The VSEL0 and VSEL1 pins must be terminated unless the internal pull-down resistors are activated.

The registers have a certain initial default value (see [Table 2](#)) and can be readjusted via I²C during operation.

This allows a simple transition between several output options by triggering the dedicated input pins. At the same time since the presets can be readjusted during operation, this offers highest flexibility.

Table 2. Output Presets

| INPUT PINS | | PRESET | I ² C REGISTER | DEFAULT OPERATION MODE | DEFAULT OUTPUT VOLTAGE [V] | | |
|------------|-------|--------|--|-------------------------------|----------------------------|-----------|----------|
| VSEL1 | VSEL0 | | | TPS62360, TPS62361B, TPS62362 | TPS62360 | TPS62361B | TPS62362 |
| 0 | 0 | SET0 | 0x00h – see Table 12 , Table 13 and Table 14 | Power Save Mode | 1.40 | 0.96 | 1.23 |
| 0 | 1 | SET1 | 0x01h – see Table 15 , Table 16 and Table 17 | Power Save Mode | 1.00 | 1.40 | 1.00 |
| 1 | 0 | SET2 | 0x02h – see Table 18 , Table 19 and Table 20 | Power Save Mode | 1.40 | 1.16 | 1.20 |
| 1 | 1 | SET3 | 0x03h – see Table 21 , Table 22 and Table 23 | Power Save Mode | 1.10 | 1.16 | 1.10 |

Via the I²C interface and/or the four preset options, the following output parameters can be changed:

- Output voltage from 0.77 V to 1.4 V (TPS62360/62) and 0.5V to 1.77V (TPS62361B) with 10 mV granularity
- Mode of operation: Power Save Mode or forced PWM mode

The slope for transition between different output voltages (Ramp Rate) can be changed via I²C as well. The slope applies for all presets globally. See [RAMP RATE CONTROLLING](#) for further details.

Since the output parameters can be changed by dedicated pins for selecting presets and by I²C, the following use scenarios are feasible:

- Control the device via dedicated pins only, after programming the presets, to choose and change within the programmed settings
- Program via I²C only. The dedicated input pins have fixed connections. Changes are conducted by changing the preset values of the active register.
- Dedicated input pins and I²C mixed operation. The non active presets might be changed. The dedicated input pins are used for the transition to the new output condition. Changes within an active preset via I²C are feasible as well.

DYNAMIC VOLTAGE SCALING

The output voltage can be adjusted dynamically. Each of the four output registers can be programmed individually by setting OV[5:0] (TPS62360/62) and OV[6:0] (TPS62361B) respectively in the SET0, SET1, SET2 and SET3 registers.

Table 3. TPS62360, TPS62362 Output Voltage Settings for Registers SET0, SET1, SET2 and SET3

| REGISTERS: SET0, SET1, SET2, SET3 | |
|-----------------------------------|----------------|
| OV[D5:D0] | OUTPUT VOLTAGE |
| 00 0000 | 770 mV |
| 00 0001 | 780 mV |
| 00 0010 | 790 mV |
| 00 0011 | 800 mV |
| ... | ... |
| 11 1101 | 1380 mV |
| 11 1110 | 1390 mV |
| 11 1111 | 1400 mV |

Table 4. TPS62361B Output Voltage Settings for Registers SET0, SET1, SET2 and SET3

| REGISTERS: SET0, SET1, SET2, SET3 | |
|-----------------------------------|----------------|
| OV[D6:D0] | OUTPUT VOLTAGE |
| 000 0000 | 500 mV |
| 000 0001 | 510 mV |
| 000 0010 | 520 mV |
| 000 0011 | 530 mV |
| ... | ... |
| 111 1101 | 1750 mV |
| 111 1110 | 1760 mV |
| 111 1111 | 1770 mV |

If the output voltage is changed at the active register (selected by VSEL0 and VSEL1), these changes will apply after the I²C command is sent.

POWER SAVE MODE AND FORCED PWM MODE

The TPS6236x devices feature a Power Save Mode to gain efficiency at light output current conditions. The device automatically transitions in both directions between pulse width modulation (PWM) operation at high load and pulse frequency modulation (PFM) operation at light load current. This maintains high efficiency at both light and heavy load currents. In PFM Mode, the device generates single switching pulses when required to maintain the programmed output voltage.

The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

The output current, at which the device transitions from PWM to PFM operation can be estimated as follows:

$$I_{OUT,TRANS} = \frac{V_{IN} - V_{OUT}}{2} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{(f \times L)} \quad (1)$$

With:

V_{IN} = Input voltage

V_{OUT} = Output Voltage

f = Switching frequency, typ. 2.5 MHz

L = Inductor value

The TPS6236x is optimized for low output voltage ripple. Therefore, the peak inductor current in PFM mode is kept small and can be calculated as follows:

$$I_{L,PFM,peak} = \frac{t_{ON}}{L} \times (V_{IN} - V_{OUT}) \quad (2)$$

And:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 350ns + 20ns \quad (3)$$

With:

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

t_{ON} = On-time of the High Side FET, from [Equation 3](#)

L = Inductor value

The TPS6236x offers a forced PWM mode as well. In this mode, the converter is forced in PWM mode even at light load currents. This comes with the benefit that the converter is operating with lower output voltage ripple. Compared to the PFM mode, the efficiency is lower during light load currents.

According to the output voltage, the Power Save Mode / forced PWM Mode can be programmed individually for each preset via I²C by setting the MODE0 – MODE3 bit D7. [Table 2](#) shows the factory presets after enabling the I²C. For additional flexibility, the Power Save Mode can be changed at a preset that is currently active.

RAMP RATE CONTROLLING

If the output voltage is changed, the TPS6236x can actively control the voltage ramp rate during the transition. An internal oscillator is embedded for high timing precision.

[Figure 38](#) and [Figure 39](#) show the operation principle. If the output voltage changes, the device will change the output voltage through discrete steps with a programmable ramp rate resulting in a corresponding transition time.

The ramp up/down slope can be programmed via I²C interface (see [Table 5](#)).

Table 5. Ramp Rates

| RMP [2:0] | RAMP RATE | |
|-----------|-----------|-----------|
| | [mV/μs] | [μs/10mV] |
| 000 | 32 | 0.3125 |
| 001 | 16 | 0.625 |
| 010 | 8 | 1.25 |
| 011 | 4 | 2.5 |
| 100 | 2 | 5 |
| 101 | 1 | 10 |
| 110 | 0.5 | 20 |
| 111 | 0.25 | 40 |

For a transition of the output voltage from $V_{OUT,A}$ to $V_{OUT,B}$ and vice versa, the resulting ramp up/down slope can be calculated as

$$\frac{\Delta V_{OUT}}{\Delta t} = 32 \frac{mV}{\mu s} \frac{1}{2^{(RMP[2:0])_2}} \quad (4)$$

If the device is operating in forced PWM Mode, the device actively controls both the ramp up and down slope.

If Power Save Mode is activated, the ramp up phase follows the programmed slope.

To force the output voltage to follow the ramp down slope in Power Save Mode, the RAMP_PFM bit needs to be set. This will force the converter to follow the ramp down slope during PFM operation as well.

If the RAMP_PFM bit is not set in Power Save Mode, the slope can be less at low output currents since the device does not actively source energy back from the output capacitor to the input or it might be sharper at high output currents since the output capacitor is discharged quickly.

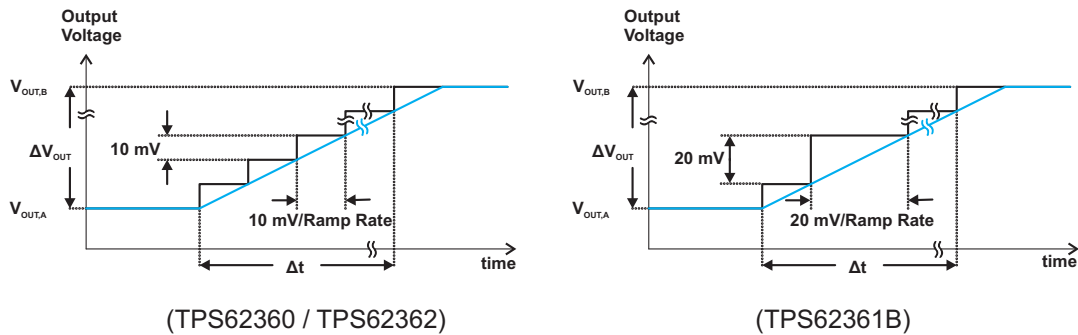


Figure 38. Ramp Up

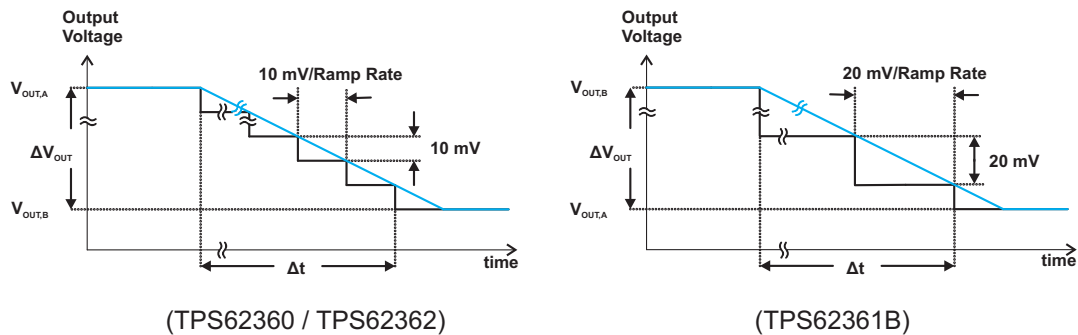


Figure 39. Ramp Down

The TPS62360 and TPS62362 ramp the output voltage taking 10mV steps, while the TPS62361B ramps taking 20mV steps with a final 10mV step if required. The resulting slope remains equal for both devices.

While the output voltage setpoint is changed in a digital stair step fashion, the connected output capacitor flattens the steps to create a linear change in the output voltage.

SAFE OPERATION AND PROTECTION FEATURES

Inductor Current Limit

The inductor current limiting prevents the device from drawing high inductor current and excessive current from the battery. Excessive current might occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition.

The incorporated inductor peak current limit measures the current while the high side power MOSFET is turned on. Once the current limit is tripped, the high side MOSFET is turned off and the low side MOSFET is turned on to ramp down the inductor current. This prevents high currents to be drawn from the battery.

Once the low side MOSFET is on, the low side forward current limit keeps the low side MOSFET on until the current through it decreases below the low side forward current limit threshold.

The negative current limit acts if current is flowing back to the battery from the output. It works differently in PWM and PFM operation. In PWM operation, the negative current limit prevents excessive current from flowing back through the inductor to the battery, preventing abnormal voltage conditions at the switching node. In PFM operation, a zero current limits any power flow back to the battery by preventing negative inductor current.

Die Temperature Monitoring and Over Temperature Protection

The TPS6236x offers two stages of die temperature monitoring and protection.

The Early Warning Monitoring Feature monitors the device temperature and provides the host an indication that the die temperature is in the higher range. If the device's junction temperature, T_J , exceeds 120°C typical, the TJEW bit is set high. To avoid the thermal shutdown being triggered, the current drawn from the TPS6236x should be reduced at this early stage.

The Over Temperature Protection feature disables the device if the temperature increases due to heavy load and/or high ambient temperature. It monitors the device die temperature and, if required, triggers the device into shutdown until the die temperature falls sufficiently.

If the junction temperature, T_J , exceeds 150°C typical, the device goes into thermal shutdown. In this mode, the power stage is turned off. During thermal shutdown, the I²C interface remains operable. All register values are kept.

For the thermal shutdown, a hysteresis of 20°C typical is implemented allowing the device to cool after the shutdown is triggered. Once the junction temperature T_J cools down to 130°C typical, the device resumes operation.

If a thermal shutdown has occurred, the TJTS bit is latched and remains a logic high as long as VDD and AVIN are present and until the bit is reset by the host.

Input Under Voltage Protection

The input under voltage protection is implemented in order to prevent operation of the device for low input voltage conditions. If the device is enabled, it prevents the device from switching if AVIN falls below the under voltage lockout threshold. If the AVIN under voltage protection threshold is tripped, the device will go into under voltage shutdown instantaneously, turning the power stage off and resetting all internal registers. The input under voltage protection is also implemented on the VDD input. If the VDD under voltage protection threshold is tripped, the device will reset all internal registers.

A under voltage lockout hysteresis of $V_{UVLO,HYST(AVIN)}$ at AVIN and $V_{UVLO,HYST(VDD)}$ at VDD is implemented.

The I²C compatible interface remains fully functional if AVIN and VDD are present. If the under voltage lockout of AVIN or VDD is triggered during operation, all internal registers are reset to their default values. Figure 40 shows the UVLO block diagram.

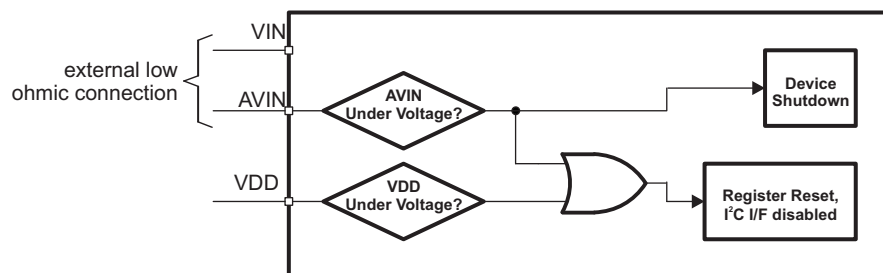


Figure 40. UVLO State Chart

By connecting VIN and AVIN to the same potential, VIN is included in the under voltage monitoring. If a low pass input filter is applied at AVIN (not mandatory for the TPS6236x), the delay and shift in the voltage level can be calculated by taking the typical quiescent current I_Q at AVIN. As an example, for I_Q and 10Ω series resistance, this results in a minimal static shift of approx. 560μV.

VIN and AVIN must be connected to the same source for proper device operation.

APPLICATION INFORMATION

I²C INTERFACE

Serial Interface Description

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a micro controller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device.

The TPS6236x device works as a *slave* and supports the following data transfer *modes*, as defined in the I²C-Bus Specification:

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- Fast mode plus (1Mbps)
- High-speed mode (3.4 Mbps)

The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as VDD and AVIN are present in the specified range. Tripping the under voltage lockout of AVIN or VDD deletes the registers and establishes the default values once the supply is present again.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as HS-mode. The TPS6236x device supports 7-bit addressing. 10-bit addressing and general call addressing are not supported.

Table 6 shows the TPS6236x devices and their assigned I²C addresses.

Table 6. I²C Address

| DEVICE OPTION | I ² C ADDRESS | |
|---------------|--------------------------|-------------------------|
| | HEXADECIMAL CODED | BINARY CODED |
| TPS62360 | (0x60) _{HEX} | (110 0000) ₂ |
| TPS62361B | (0x60) _{HEX} | (110 0000) ₂ |
| TPS62362 | (0x60) _{HEX} | (110 0000) ₂ |

F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 41. All I²C-compatible devices should recognize a start condition.

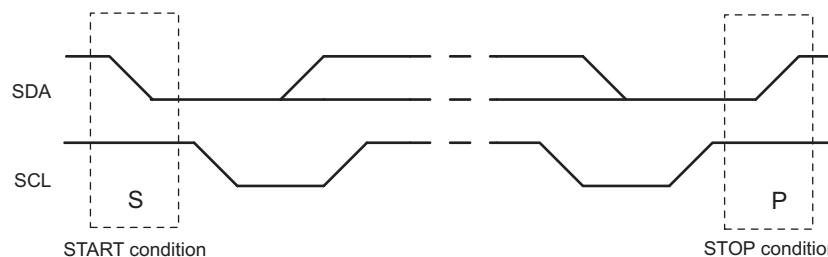


Figure 41. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires

the SDA line to be stable during the entire high period of the clock pulse (see [Figure 42](#)). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see [Figure 43](#)) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

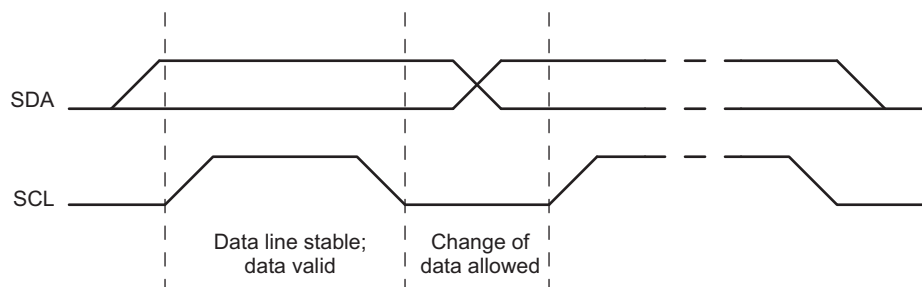


Figure 42. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see [Figure 41](#)). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

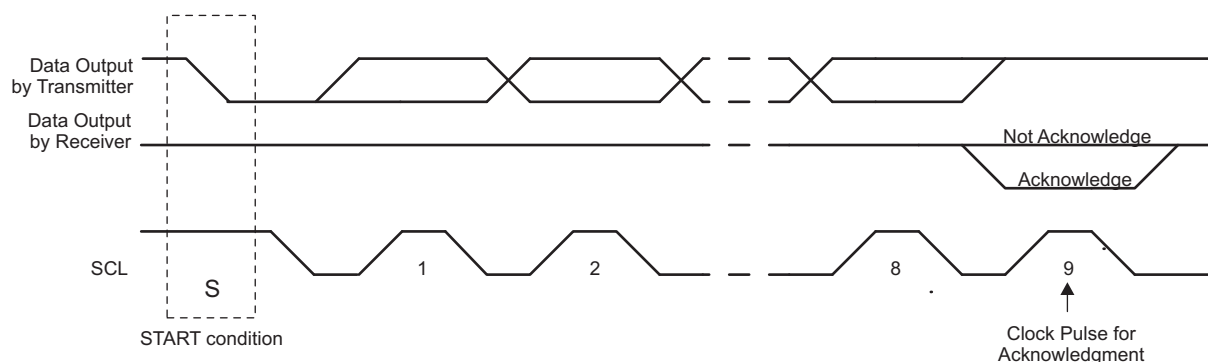
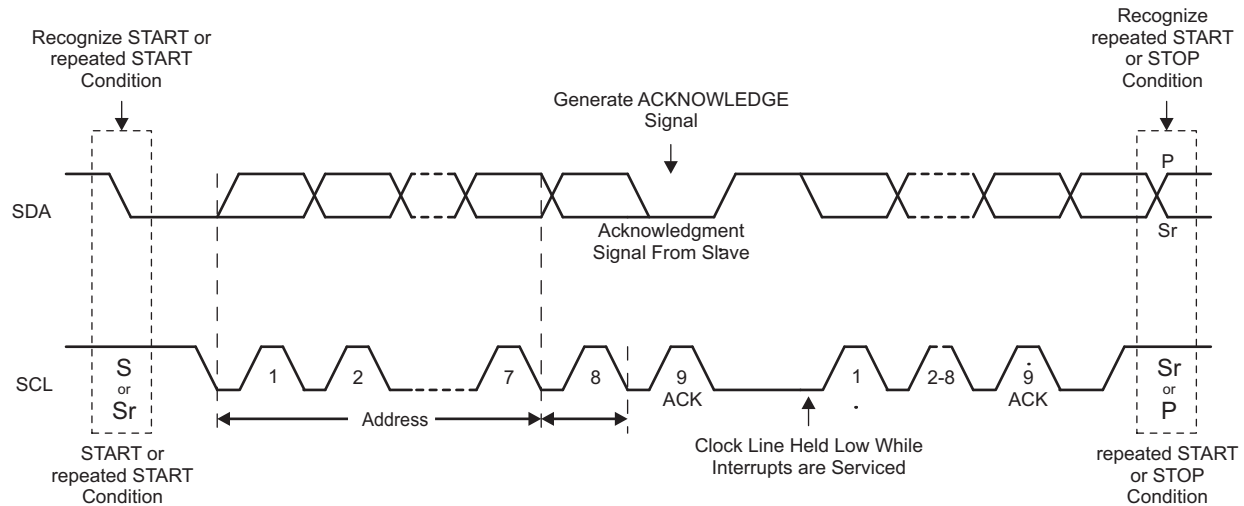


Figure 43. Acknowledge on the I²C Bus


Figure 44. Bus Protocol

HS-Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

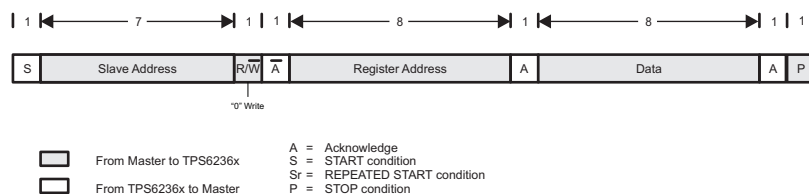
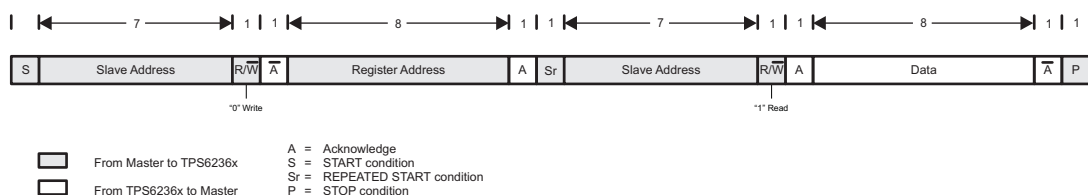
The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.

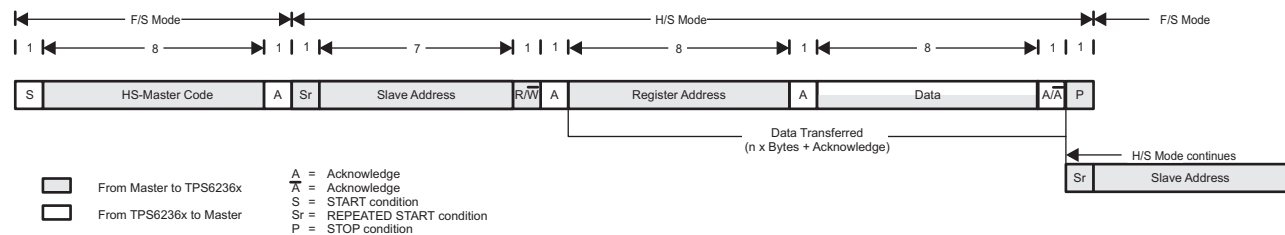
The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

I²C UPDATE SEQUENCE

The TPS6236x requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, the TPS6236x device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the TPS6236x. The TPS6236x performs an update on the falling edge of the acknowledge signal that follows the LSB byte.


Figure 45. Write Data Transfer Format in F/S-Mode

Figure 46. Read Data Transfer Format in F/S-Mode

**Figure 47. Data Transfer Format in H/S-Mode****Slave Address Byte**

| MSB | | | | | | | LSB |
|-----|---|---|---|---|---|----|-----|
| X | X | X | X | X | X | A1 | A0 |

The slave address byte is the first byte received following the START condition from the master device.

Register Address Byte

| MSB | | | | | | | LSB |
|-----|---|---|---|---|----|----|-----|
| 0 | 0 | 0 | 0 | 0 | D2 | D1 | D0 |

Following the successful acknowledgment of the slave address, the bus master will send a byte to the TPS6236x, which will contain the address of the register to be accessed.

I²C REGISTER RESET

The I²C registers can be reset by pulling VDD to GND. Refer to the [Input Under Voltage Protection](#) section for details.

PULL DOWN RESISTORS

The EN, VSEL0 and VSEL1 inputs feature internal pull down resistors to discharge the potential if one of the pins is not connected or is triggered by a high impedance source.

To achieve lowest possible quiescent current, the pull down resistors can be disabled individually at EN, VSEL0 and VSEL1 by I²C programming the registers PD_EN, PD_VSEL0 and PD_VSEL1.

By default, the pull down resistors are enabled.

INPUT CAPACITOR SELECTION

The input capacitor is required to buffer the pulsing current drawn by the device at VIN and reducing the input voltage ripple. The pulsing current is originated by the operation principles of a step down converter.

Low ESR input capacitors are required for best input voltage filtering and minimal interference with other system components. For best performance, ceramic capacitors with a low ESR at the switching frequency are recommended. X7R or X5R type capacitors should be used.

A ceramic input capacitor in the nominal range of $C_{IN} = 4.7\mu\text{F}$ to $22\mu\text{F}$ should be a good choice for most application scenarios. In general, there is no upper limit for increasing the input capacitor.

For typical operation, a $10\mu\text{F}$ X5R type capacitor is recommended. [Table 7](#) shows a list of recommended capacitors.

Table 7. List of Recommended Capacitors

| CAPACITANCE [μF] | TYPE | DIMENSIONS L x W x H [mm ³] | MANUFACTURER |
|---------------------|-----------------|--|--------------|
| 10 | GRM188R60J106M | 0603: 1.6 x 0.8 x 0.8 | Murata |
| 10 | CL10A106MQ8NRNC | 0603: 1.6 x 0.8 x 0.8 | Samsung |
| 22 | GRM188R60G226M | 0603: 1.6 x 0.8 x 0.8 | Murata |
| 22 | CL10A106MQ8NRNC | 0603: 1.6 x 0.8 x 0.8 | Samsung |

DECOUPLING CAPACITORS AT AVIN, VDD

Noise impacts can be reduced by buffering AVIN and VDD with a decoupling capacitor. It is recommended to buffer AVIN and VDD with a X5R or X7R ceramic capacitor of at least 0.1μF connected between AVIN, AGND and VDD, AGND respectively. The capacitor closest to the pin should be kept small (< 0.22μF) in order to keep a low impedance at high frequencies. In general, there is no upper limit for the total capacitance.

Adding a low pass input filter at AVIN (e.g. by adding a resistor in series) is not mandatory for the TPS6236x to filter out noise.

INDUCTOR SELECTION

The choice of the inductor type and value has an impact on the inductor ripple current, the transition point of PFM to PWM operation, the output voltage ripple and accuracy. The subsections below support for choosing the proper inductor.

Inductance Value

The TPS6236x is designed for best operation with a nominal inductance value of 1μH.

Choosing a smaller value than 1μH improves the load transient behavior, whereas choosing a higher value reduces the ripple current resulting in a smaller output voltage ripple and better DC output regulation. The inductor current ripple can be calculated as:

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (5)$$

With:

V_{IN} = Input Voltage

V_{OUT} = Output Voltage

f = Switching frequency, typ. 2.5 MHz

L = Inductor value

Inductor Saturation Current

The inductor needs to be selected for its current rating. To pick the proper saturation current rating, the maximum inductor current can be calculated as:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (6)$$

With:

ΔI_L = Inductor ripple current (see [Equation 5](#))

$I_{OUT,MAX}$ = Maximum output current

Since the inductance can be decreased by saturation effects and temperature impact, the inductor needs to be chosen to have an effective inductance of at least 0.6μH under temperature and saturation effects.

Table 8. List of Recommended Inductors

| INDUCTANCE [μH] | SATURATION CURRENT RATING (30% inductance drop, typ) [A] | DIMENSIONS L x W x H [mm ³] | DC RESISTANCE [mΩ typ] | TYPE | MANUFACTURER |
|--------------------|--|--|---------------------------|--|--------------|
| 1.0 | 3.4 | 3.2 x 2.5 x 1.2 | 51 | PST032251B-1R0MS-11 | Cyntec |
| 1.0 | 3.9 | 3.2 x 2.5 x 1.0 | 48 | DFE322510C1276AS-H-1R0N ⁽¹⁾ | Toko |
| 1.0 | 4.6 | 3.2 x 2.5 x 1.2 | 37 | DFE322512C1277AS-H-1R0N ⁽¹⁾ | Toko |
| 1.0 | 3.8 | 2.5 x 2.0 x 1.2 | 45 | DFE252012C1239AS-H-1R0N=P2 | Toko |
| 1.0 | 5.4 | 4 x 4 x 2.1 | 10 | XFL4020-102ME1.0 | Coilcraft |
| 1.0 | 5.4 | 3.2 x 3 x 1.2 | 57 | SPM3012T-1R0M | TDK |

(1) Release planned for Q4/2011. Contact manufacturer for details.

OUTPUT CAPACITOR SELECTION

The unique hysteretic control scheme allows the use of tiny ceramic capacitors. For best performance, ceramic capacitors with low ESR values are recommended to achieve high conversion efficiency and low output voltage ripple. For stable operation, X7R or X5R type capacitors are recommended.

The TPS6236x is designed to operate with an output capacitor of 10μF to 22μF, placed at the device's output. In addition a 0.1μF capacitor can be added to the output to reduce the high frequency content created by a very sudden load change.

At light loads, if the device is operating in PFM Mode, choosing a higher value will minimize the voltage ripple resulting in a better DC output accuracy.

Buffering the processor input by an additional ceramic capacitor in the range of 10μF to 22μF improves the voltage quality at the processor input and the dynamic load step behavior. This is especially true if the trace between the TPS6236x and the microprocessor is longer than the smallest possible. This additional capacitor needs to be taken into account for the recommended capacitance value. For stability, the sum of the VOUT capacitors should not exceed 75μF effective capacitance.

Table 7 shows a list of tested capacitors. The TPS6236x is not designed for use with polymer, tantalum, or electrolytic output capacitors.

OUTPUT FILTER DESIGN

The inductor and the output capacitor build the output filter. The load might be buffered with an input capacitor C_{LOAD} , which needs to be factored in. Based on the output capacitor and inductance recommendation sections and factoring in C_{LOAD} , these components should be in the range:

- $C_{OUT} + C_{LOAD} = 10\mu F$ to $75\mu F$
- $L = 1\mu H$

For further performance or specific demands, these values might be tweaked. In any case, the loop stability should be checked since the control loop stability might be affected.

THERMAL AND DEVICE LIFE TIME INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Thermal performance can be enhanced by proper PCB layout. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi layer PCB designs with vias to different layers.

Proper PCB layout with focus on thermal performance results in a reduced junction-to-ambient thermal resistance θ_{JA} and thereby reduces the device junction temperature, T_J .

The TI reliability requirement for the silicon chip's life time (100K Power-On-Hours at $T_J = 105^\circ\text{C}$) is affected by the junction temperature and the continuously drawn current at the VIN pin and the SW pins. In order to be consistent with the TI reliability requirement for the silicon chips (100000 Power-On-Hours at $T_J = 105^\circ\text{C}$), the VIN pin current should not continuously exceed 1275mA and the SW pins current should not continuously exceed 2550mA so as to prevent electromigration failure in the solder bump. Drawing 1150mA at VIN would, as an example, be the case for typically $I_{OUT} = 2350\text{mA}$, $V_{OUT} = 1.5\text{V}$ and $V_{IN} = 3.6\text{V}$.

Exceeding the VIN pin / SW pins current rating might affect the device reliability. As an example, drawing current peaks $I_{OUT} = 3000\text{mA}$ with up to 10% of the application time over a base continuous output current $I_{OUT} = 2000\text{mA}$ might reduce the Power-on-Hours to 90000 hours for conditions such as $V_{IN} = 2.7\text{V}$, $V_{OUT} = 1.5\text{V}$, $T_J = 105^\circ\text{C}$. In this example, exceeding $T_J = 105^\circ\text{C}$ in combination with a higher peak output current duty cycle clearly further affects the device life time.

For more details on how to use the thermal parameters, see the application notes: [Thermal Characteristics Application Note \(SZZA017\)](#), and [IC Package Thermal Metrics Application Note \(SPRA953\)](#).

PCB LAYOUT CONSIDERATIONS

The PCB layout is an important step to maintain the high performance of the TPS6236x. Both the high current and the fast switching nodes demands full attention to the PCB layout.

The input / output capacitors and the inductor should be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance. A common power GND should be used. The low side of the input and output capacitors must be connected to the power GND, as well as the PGND node. AGND and PGND should be connected close to the IC but at a single place.

The sense traces connected to SENSE+ and SENSE- are signal traces. Special care should be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. GND layers might be used for shielding if the parasitic capacitance can be kept small. Routing the SENSE+ and SENSE- close to each other minimizes inductive noise injection. Keep these traces away from switching nodes and swiftly alternating signal lines such as the I²C bus.

Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues or unsatisfying EMI behavior.

See [Figure 48](#) for the recommended layout.

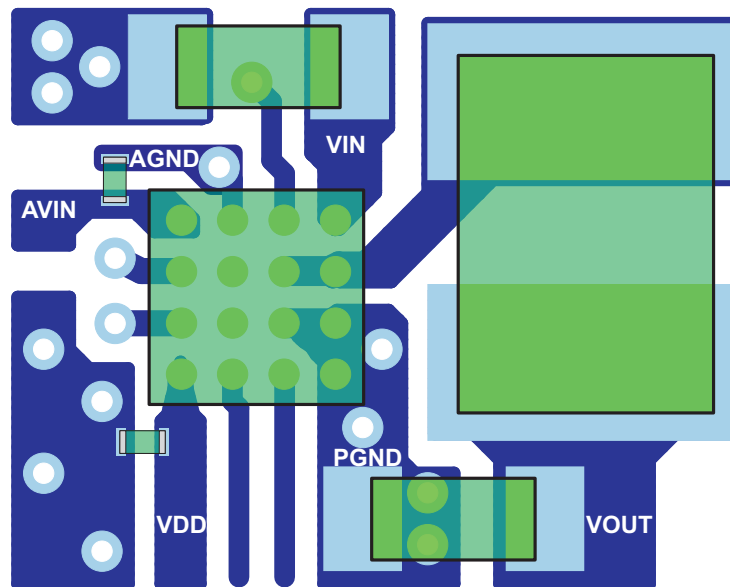


Figure 48. Layout Suggestion (top view). Overall Solution Size: 27.5mm²

REGISTER SETTINGS

Overview

Table 9. TPS62360 Register Settings Overview

| ADDRESS | REGISTER | RESET / DEFAULT STATE | READ / WRITE | REGISTER (default / reset values) | | | | | | | |
|---------|------------|-----------------------------|-----------------|-----------------------------------|----------|----------|----|----|---------|----------|----------|
| | | | | MSB | | | | | | | LSB |
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0x00h | SET0 | 0x111111 | R/W | MODE0 | | | | | | | OV0[5:0] |
| 0x01h | SET1 | 0x010111 | R/W | MODE1 | | | | | | | OV1[5:0] |
| 0x02h | SET2 | 0x111111 | R/W | MODE2 | | | | | | | OV2[5:0] |
| 0x03h | SET3 | 0x100001 | R/W | MODE3 | | | | | | | OV3[5:0] |
| 0x04h | Ctrl | 111xxxxx | R/W | PD_EN | PD_VSEL0 | PD_VSEL1 | | | | | |
| 0x05h | Temp | xxxxx000 | R/W | | | | | | DIS_TS | TJEW | TJTS |
| 0x06h | RmpCtrl | 000xx00x | R/W | | | | | | EN_DISC | RAMP_PFM | |
| 0x07h | (Reserved) | xxxxxxx | | | | | | | | | |
| 0x08h | Chip_ID | 100000xx | R | | | | | | | | |
| 0x09h | Chip_ID | | | | | | | | | | |

Table 10. TPS62361B Register Settings Overview

| ADDRESS | REGISTER | RESET / DEFAULT STATE | READ / WRITE | REGISTER (default / reset values) | | | | | | | |
|---------|------------|-----------------------------|-----------------|-----------------------------------|----------|----------|----|----|---------|----------|----------|
| | | | | MSB | | | | | | | LSB |
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0x00h | SET0 | 00101110 | R/W | MODE0 | | | | | | | OV0[6:0] |
| 0x01h | SET1 | 01011010 | R/W | MODE1 | | | | | | | OV1[6:0] |
| 0x02h | SET2 | 01000010 | R/W | MODE2 | | | | | | | OV2[6:0] |
| 0x03h | SET3 | 01000010 | R/W | MODE3 | | | | | | | OV3[6:0] |
| 0x04h | Ctrl | 111xxxxx | R/W | PD_EN | PD_VSEL0 | PD_VSEL1 | | | | | |
| 0x05h | Temp | xxxxx000 | R/W | | | | | | DIS_TS | TJEW | TJTS |
| 0x06h | RmpCtrl | 000xx00x | R/W | | | | | | EN_DISC | RAMP_PFM | |
| 0x07h | (Reserved) | xxxxxxx | | | | | | | | | |
| 0x08h | Chip_ID | 100001xx | R | | | | | | | | |
| 0x09h | Chip_ID | | | | | | | | | | |

Table 11. TPS62362 Register Settings Overview

| ADDRESS | REGISTER | RESET / DEFAULT STATE | READ / WRITE | REGISTER (default / reset values) | | | | | | | |
|---------|------------|-----------------------------|-----------------|-----------------------------------|----------|----------|----|----|---------|----------|----------|
| | | | | MSB | | | | | | | LSB |
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0x00h | SET0 | 0x101110 | R/W | MODE0 | | | | | | | OV0[5:0] |
| 0x01h | SET1 | 0x010111 | R/W | MODE1 | | | | | | | OV1[5:0] |
| 0x02h | SET2 | 0x101011 | R/W | MODE2 | | | | | | | OV2[5:0] |
| 0x03h | SET3 | 0x100001 | R/W | MODE3 | | | | | | | OV3[5:0] |
| 0x04h | Ctrl | 111xxxxx | R/W | PD_EN | PD_VSEL0 | PD_VSEL1 | | | | | |
| 0x05h | Temp | xxxxx000 | R/W | | | | | | DIS_TS | TJEW | TJTS |
| 0x06h | RmpCtrl | 000xx00x | R/W | | | | | | EN_DISC | RAMP_PFM | |
| 0x07h | (Reserved) | xxxxxxx | | | | | | | | | |
| 0x08h | Chip_ID | 100010xx | R | | | | | | | | |
| 0x09h | Chip_ID | | | | | | | | | | |

Register 0x00h Description: SET0

The register settings apply by choosing SET0 (VSEL1 = LOW, VSEL0 = LOW).

Table 12. TPS62360 Register 0x00h Description

| REGISTER ADDRESS: 0x00h Read/Write | | | | | |
|------------------------------------|----------|---------|---------|--|--|
| BIT | NAME | DEFAULT | | DESCRIPTION | |
| D7 | MODE0 | MSB | 0 | Operation mode for SET0 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | |
| D6 | | | x | Reserved for future use | |
| D5 | OV0[5:0] | | 1 | Output voltage for SET0 Default: (111111) ₂ = 1.4V | |
| D4 | | 1 | D5-D0 | Output voltage | |
| D3 | | 1 | 00 0000 | 770 mV | |
| D2 | | 1 | 00 0001 | 780 mV | |
| | | | 00 0010 | 790 mV | |
| D1 | | 1 | ... | ... | |
| | | | 11 1111 | 1400 mV | |
| D0 | | LSB | 1 | V _{OUT} = (xx xxxx) ₂ × 10mV + 770 mV | |

Table 13. TPS62361B Register 0x00h Description

| REGISTER ADDRESS: 0x00h Read/Write | | | | | |
|------------------------------------|----------|---------|---|--|----------------|
| BIT | NAME | DEFAULT | | DESCRIPTION | |
| D7 | MODE0 | MSB | 0 | Operation mode for SET0 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | |
| D6 | OV0[6:0] | | 0 | Output voltage for SET0 Default: (0101110) ₂ = 0.96V | |
| D5 | | | 1 | | |
| D4 | | | 0 | D6-D0 | Output voltage |
| D3 | | | 1 | 000 0000 | 500 mV |
| D2 | | | 1 | 000 0001 | 510 mV |
| | | | | 000 0010 | 520 mV |
| D1 | | | 1 | ... | ... |
| | | | | 111 1111 | 1770 mV |
| D0 | | | | LSB | 0 |

Table 14. TPS62362 Register 0x00h Description

| REGISTER ADDRESS: 0x00h Read/Write | | | | | |
|------------------------------------|----------|---------|-----|--|---|
| BIT | NAME | DEFAULT | | DESCRIPTION | |
| D7 | MODE0 | MSB | 0 | Operation mode for SET0 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | |
| D6 | | | x | Reserved for future use | |
| D5 | OV0[5:0] | | 1 | Output voltage for SET0 Default: (101110) ₂ = 1.23V | |
| D4 | | | 0 | D5-D0 | Output voltage |
| D3 | | | 1 | 00 0000 | 770 mV |
| D2 | | | 1 | 00 0001 | 780 mV |
| | | | | 00 0010 | 790 mV |
| D1 | | | 1 | ... | ... |
| | | | | 11 1111 | 1400 mV |
| D0 | | | LSB | 0 | V _{OUT} = (xx xxxx) ₂ × 10mV + 770 mV |

Register 0x01h Description: SET1

The register settings apply by choosing SET1 (VSEL1 = LOW, VSEL0 = HIGH).

Table 15. TPS62360 Register 0x01h Description

| REGISTER ADDRESS: 0x01h Read/Write | | | | | |
|--|----------|--|---|--|----------------|
| BIT | NAME | DEFAULT | | DESCRIPTION | |
| D7 | MODE1 | MSB | 0 | Operation mode for SET1 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | |
| D6 | | | x | Reserved for future use | |
| D5 | OV1[5:0] | | 0 | Output voltage for SET1 Default: (010111) ₂ = 1.0V | |
| D4 | | 1 | <table><tr><td>D5-D0</td><td>Output voltage</td></tr></table> | D5-D0 | Output voltage |
| D5-D0 | | Output voltage | | | |
| D3 | | 0 | <table><tr><td>00 0000</td><td>770 mV</td></tr></table> | 00 0000 | 770 mV |
| 00 0000 | | 770 mV | | | |
| D2 | | 1 | <table><tr><td>00 0001</td><td>780 mV</td></tr></table> | 00 0001 | 780 mV |
| | | | 00 0001 | 780 mV | |
| <table><tr><td>00 0010</td><td>790 mV</td></tr></table> | | 00 0010 | 790 mV | | |
| 00 0010 | 790 mV | | | | |
| D1 | 1 | <table><tr><td>...</td><td>...</td></tr></table> | ... | ... | |
| | | ... | ... | | |
| <table><tr><td>11 1111</td><td>1400 mV</td></tr></table> | 11 1111 | 1400 mV | | | |
| 11 1111 | 1400 mV | | | | |
| D0 | | LSB | 1 | V _{OUT} = (xx xxxx) ₂ × 10mV + 770 mV | |

Table 16. TPS62361B Register 0x01h Description

| REGISTER ADDRESS: 0x01h Read/Write | | | | | | | | |
|------------------------------------|----------|--|--|---|----------|----------------|----------|--------|
| BIT | NAME | DEFAULT | | DESCRIPTION | | | | |
| D7 | MODE1 | MSB | 0 | Operation mode for SET1 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | | | | |
| D6 | OV1[6:0] | | 1 | Output voltage for SET1 Default: (1011010) ₂ = 1.4V | | | | |
| D5 | | | 0 | | | | | |
| D4 | | | 1 | <table><tr><td>D6-D0</td><td>Output voltage</td></tr></table> | D6-D0 | Output voltage | | |
| D6-D0 | | | Output voltage | | | | | |
| D3 | | | 1 | <table><tr><td>000 0000</td><td>500 mV</td></tr></table> | 000 0000 | 500 mV | | |
| 000 0000 | | | 500 mV | | | | | |
| D2 | | | 0 | <table><tr><td>000 0001</td><td>510 mV</td></tr><tr><td>000 0010</td><td>520 mV</td></tr></table> | 000 0001 | 510 mV | 000 0010 | 520 mV |
| 000 0001 | | | 510 mV | | | | | |
| 000 0010 | 520 mV | | | | | | | |
| D1 | 1 | <table><tr><td>...</td><td>...</td></tr><tr><td>111 1111</td><td>1770 mV</td></tr></table> | ... | ... | 111 1111 | 1770 mV | | |
| ... | ... | | | | | | | |
| 111 1111 | 1770 mV | | | | | | | |
| D0 | LSB | 0 | V _{OUT} = (xxx xxxx) ₂ × 10mV + 500 mV | | | | | |

Table 17. TPS62362 Register 0x01h Description

| REGISTER ADDRESS: 0x01h Read/Write | | | | | | | |
|------------------------------------|----------|---|--|---|---------|----------------|---------|
| BIT | NAME | DEFAULT | | DESCRIPTION | | | |
| D7 | MODE1 | MSB | 0 | Operation mode for SET1 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | | | |
| D6 | | | x | Reserved for future use | | | |
| D5 | OV1[5:0] | | 0 | Output voltage for SET1 Default: $(010111)_2 = 1.0\text{V}$ | | | |
| D4 | | | 1 | <table><tr><td>D5-D0</td><td>Output voltage</td></tr></table> | D5-D0 | Output voltage | |
| D5-D0 | | | Output voltage | | | | |
| D3 | | | 0 | <table><tr><td>00 0000</td><td>770 mV</td></tr></table> | 00 0000 | 770 mV | |
| 00 0000 | | | 770 mV | | | | |
| D2 | | | 1 | <table><tr><td>00 0001</td><td>780 mV</td></tr><tr><td>00 0010</td><td>790 mV</td></tr></table> | 00 0001 | 780 mV | 00 0010 |
| | | 00 0001 | | 780 mV | | | |
| 00 0010 | 790 mV | | | | | | |
| D1 | 1 | <table><tr><td>...</td><td>...</td></tr><tr><td>11 1111</td><td>1400 mV</td></tr></table> | ... | ... | 11 1111 | 1400 mV | |
| | | ... | ... | | | | |
| 11 1111 | 1400 mV | | | | | | |
| D0 | LSB | 1 | $V_{\text{OUT}} = (\text{xx xxxx})_2 \times 10\text{mV} + 770\text{ mV}$ | | | | |

Register 0x02h Description: SET2

The register settings apply by choosing SET2 (VSEL1 = HIGH, VSEL0 = LOW).

Table 18. TPS62360 Register 0x02h Description

| REGISTER ADDRESS: 0x02h Read/Write | | | | | |
|------------------------------------|----------|---------|---------|--|--|
| BIT | NAME | DEFAULT | | DESCRIPTION | |
| D7 | MODE2 | MSB | 0 | Operation mode for SET2 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | |
| D6 | | | x | Reserved for future use | |
| D5 | OV2[5:0] | | 1 | Output voltage for SET2 Default: (111111) ₂ = 1.4V | |
| D4 | | 1 | D5-D0 | Output voltage | |
| D3 | | 1 | 00 0000 | 770 mV | |
| D2 | | 1 | 00 0001 | 780 mV | |
| | | | 00 0010 | 790 mV | |
| D1 | | 1 | ... | ... | |
| | | | 11 1111 | 1400 mV | |
| D0 | | LSB | 1 | V _{OUT} = (xx xxxx) ₂ × 10mV + 770 mV | |

Table 19. TPS62361B Register 0x02h Description

| REGISTER ADDRESS: 0x02h Read/Write | | | | | | | | |
|------------------------------------|----------|--|----------------|---|----------|----------------|----------|--------|
| BIT | NAME | DEFAULT | | DESCRIPTION | | | | |
| D7 | MODE2 | MSB | 0 | Operation mode for SET2 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | | | | |
| D6 | OV2[6:0] | | 1 | Output voltage for SET2 Default: (1000010) ₂ = 1.16V | | | | |
| D5 | | | 0 | | | | | |
| D4 | | | 0 | <table><tr><td>D6-D0</td><td>Output voltage</td></tr></table> | D6-D0 | Output voltage | | |
| D6-D0 | | | Output voltage | | | | | |
| D3 | | | 0 | <table><tr><td>000 0000</td><td>500 mV</td></tr></table> | 000 0000 | 500 mV | | |
| 000 0000 | | | 500 mV | | | | | |
| D2 | | | 0 | <table><tr><td>000 0001</td><td>510 mV</td></tr><tr><td>000 0010</td><td>520 mV</td></tr></table> | 000 0001 | 510 mV | 000 0010 | 520 mV |
| | | | | 000 0001 | 510 mV | | | |
| 000 0010 | | | 520 mV | | | | | |
| D1 | 1 | <table><tr><td>...</td><td>...</td></tr><tr><td>111 1111</td><td>1770 mV</td></tr></table> | ... | ... | 111 1111 | 1770 mV | | |
| | | ... | ... | | | | | |
| 111 1111 | 1770 mV | | | | | | | |
| D0 | | LSB | 0 | V _{OUT} = (xxx xxxx) ₂ × 10mV + 500 mV | | | | |

Table 20. TPS62362 Register 0x02h Description

| REGISTER ADDRESS: 0x02h Read/Write | | | | | | | | |
|------------------------------------|----------|---|----------------|---|---------|----------------|---------|--------|
| BIT | NAME | DEFAULT | | DESCRIPTION | | | | |
| D7 | MODE2 | MSB | 0 | Operation mode for SET2 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | | | | |
| D6 | | | x | Reserved for future use | | | | |
| D5 | OV2[5:0] | | 1 | Output voltage for SET2 Default: $(101011)_2 = 1.2\text{V}$ | | | | |
| D4 | | | 0 | <table><tr><td>D5-D0</td><td>Output voltage</td></tr></table> | D5-D0 | Output voltage | | |
| D5-D0 | | | Output voltage | | | | | |
| D3 | | | 1 | <table><tr><td>00 0000</td><td>770 mV</td></tr></table> | 00 0000 | 770 mV | | |
| 00 0000 | | | 770 mV | | | | | |
| D2 | | | 0 | <table><tr><td>00 0001</td><td>780 mV</td></tr><tr><td>00 0010</td><td>790 mV</td></tr></table> | 00 0001 | 780 mV | 00 0010 | 790 mV |
| | | | | 00 0001 | 780 mV | | | |
| 00 0010 | | | 790 mV | | | | | |
| D1 | 1 | <table><tr><td>...</td><td>...</td></tr><tr><td>11 1111</td><td>1400 mV</td></tr></table> | ... | ... | 11 1111 | 1400 mV | | |
| | | ... | ... | | | | | |
| 11 1111 | 1400 mV | | | | | | | |
| D0 | | LSB | 1 | $V_{\text{OUT}} = (\text{xx xxxx})_2 \times 10\text{mV} + 770\text{ mV}$ | | | | |
| | | | | | | | | |

Register 0x03h Description: SET3

The register settings apply by choosing SET3 (VSEL1 = HIGH, VSEL0 = HIGH).

Table 21. TPS62360 Register 0x03h Description

| REGISTER ADDRESS: 0x03h Read/Write | | | | | |
|------------------------------------|----------|---------|---------|--|--|
| BIT | NAME | DEFAULT | | DESCRIPTION | |
| D7 | MODE3 | MSB | 0 | Operation mode for SET3 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | |
| D6 | | | x | Reserved for future use | |
| D5 | OV3[5:0] | | 1 | Output voltage for SET3 Default: $(100001)_2 = 1.1V$ | |
| D4 | | 0 | D5-D0 | Output voltage | |
| D3 | | 0 | 00 0000 | 770 mV | |
| D2 | | 0 | 00 0001 | 780 mV | |
| | | | 00 0010 | 790 mV | |
| D1 | | 0 | ... | ... | |
| | | | 11 1111 | 1400 mV | |
| D0 | | LSB | 1 | $V_{OUT} = (xx\ xxxx)_2 \times 10mV + 770\ mV$ | |

Table 22. TPS62361B Register 0x03h Description

| REGISTER ADDRESS: 0x03h Read/Write | | | | | | | | |
|------------------------------------|----------|--|--|---|----------|----------------|----------|--------|
| BIT | NAME | DEFAULT | | DESCRIPTION | | | | |
| D7 | MODE3 | MSB | 0 | Operation mode for SET3 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | | | | |
| D6 | OV3[6:0] | | 1 | Output voltage for SET3 Default: (1000010) ₂ = 1.16V | | | | |
| D5 | | | 0 | | | | | |
| D4 | | | 0 | <table><tr><td>D6-D0</td><td>Output voltage</td></tr></table> | D6-D0 | Output voltage | | |
| D6-D0 | | | Output voltage | | | | | |
| D3 | | | 0 | <table><tr><td>000 0000</td><td>500 mV</td></tr></table> | 000 0000 | 500 mV | | |
| 000 0000 | | | 500 mV | | | | | |
| D2 | | | 0 | <table><tr><td>000 0001</td><td>510 mV</td></tr><tr><td>000 0010</td><td>520 mV</td></tr></table> | 000 0001 | 510 mV | 000 0010 | 520 mV |
| 000 0001 | | | 510 mV | | | | | |
| 000 0010 | 520 mV | | | | | | | |
| D1 | 1 | <table><tr><td>...</td><td>...</td></tr><tr><td>111 1111</td><td>1770 mV</td></tr></table> | ... | ... | 111 1111 | 1770 mV | | |
| ... | ... | | | | | | | |
| 111 1111 | 1770 mV | | | | | | | |
| D0 | LSB | 0 | V _{OUT} = (xxx xxxx) ₂ × 10mV + 500 mV | | | | | |

Table 23. TPS62362 Register 0x03h Description

| REGISTER ADDRESS: 0x03h Read/Write | | | | | |
|------------------------------------|----------|---------|---------|--|----------------|
| BIT | NAME | DEFAULT | | DESCRIPTION | |
| D7 | MODE3 | MSB | 0 | Operation mode for SET3 0 = PFM / PWM mode operation 1 = Forced PWM mode operation | |
| D6 | | | x | Reserved for future use | |
| D5 | OV3[5:0] | | 1 | Output voltage for SET3 Default: (100001) ₂ = 1.1V | |
| D4 | | | 0 | D5-D0 | Output voltage |
| D3 | | | 0 | 00 0000 | 770 mV |
| D2 | | | 0 | 00 0001 | 780 mV |
| | | | | 00 0010 | 790 mV |
| D1 | | | 0 | ... | ... |
| | | 11 1111 | 1400 mV | | |
| D0 | | LSB | 1 | V _{OUT} = (xx xxxx) ₂ × 10mV + 770 mV | |

Register 0x04h Description: Ctrl

Table 24. TPS6236x Register 0x04h Description

| REGISTER ADDRESS: 0x04h Read / Write | | | | |
|--------------------------------------|----------|---------|---|--|
| BIT | NAME | DEFAULT | | DESCRIPTION |
| D7 | PD_EN | MSB | 1 | EN internal pull down resistor 0 = disabled 1 = enabled |
| D6 | PD_VSEL0 | | 1 | VSEL0 internal pull down resistor 0 = disabled 1 = enabled |
| D5 | PD_VSEL1 | | 1 | VSEL1 internal pull down resistor 0 = disabled 1 = enabled |
| D4 | | | x | Reserved for future use |
| D3 | | | x | Reserved for future use |
| D2 | | | x | Reserved for future use |
| D1 | | | x | Reserved for future use |
| D0 | | LSB | x | Reserved for future use |

Register 0x05h Description: Temp

Table 25. TPS6236x Register 0x05h Description

| REGISTER ADDRESS: 0x05h Read/Write | | | | |
|------------------------------------|--------|---------|---|---|
| BIT | NAME | DEFAULT | | DESCRIPTION |
| D7 | | MSB | x | Reserved for future use |
| D6 | | | x | Reserved for future use |
| D5 | | | x | Reserved for future use |
| D4 | | | x | Reserved for future use |
| D3 | | | x | Reserved for future use |
| D2 | DIS_TS | | 0 | Disable temperature shutdown feature 0 = Temperature shutdown enabled 1 = Temperature shutdown disabled |
| D1 | TJEW | LSB | 0 | T _J early warning bit 0 = T _J < 120°C (typ) 1 = T _J ≥ 120°C (typ) |
| D0 | TJTS | | 0 | T _J temperature shutdown bit 0 = die temperature within the valid range 1 = temperature shutdown was triggered Bit needs to be reset after it has been latched. |

Register 0x06h Description: RmpCtrl**Table 26. TPS6236x Register 0x06h Description**

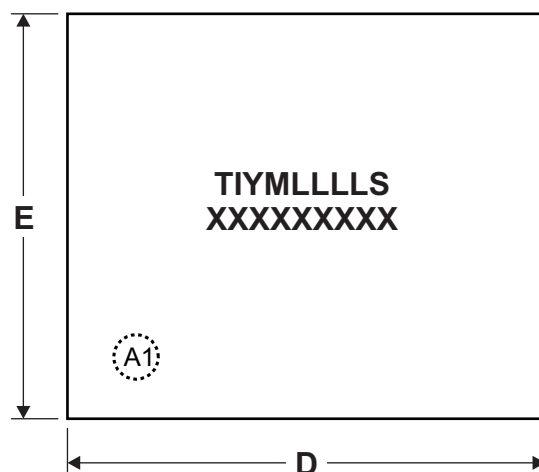
| REGISTER ADDRESS: 0x06h Read/Write | | | | |
|------------------------------------|----------|---------|---|---|
| BIT | NAME | DEFAULT | | DESCRIPTION |
| D7 | RMP[2:0] | MSB | 0 | Output voltage ramp timing |
| | | | | D7-D5 Slope |
| | | | | 000 32 mV / μ s |
| | | | | 001 16 mV / μ s |
| | | | | 010 8 mV / μ s |
| | | | | |
| | | | | 110 0.5 mV / μ s |
| | | | | 111 0.25 mV / μ s |
| D6 | | | 0 | |
| D5 | | | 0 | $\frac{\Delta V_{OUT}}{\Delta t} = 32 \frac{\text{mV}}{\mu\text{s}} \frac{1}{2^{(RMP[2-0])_2}}$ |
| D4 | | | x | Reserved for future use |
| D3 | | | x | Reserved for future use |
| D2 | EN_DISC | | 0 | Active output capacitor discharge at shutdown 0 = disabled 1 = enabled |
| D1 | RAMP_PFM | | 0 | Defines the ramp behavior if the device is in Power Save (PFM) mode 0 = output cap will be discharged by the load 1 = output voltage will be forced to follow the ramp down slope |
| D0 | | LSB | x | Reserved for future use |

Register 0x07h Description: (Reserved)**Table 27. TPS6236x Register 0x07h Description**

| REGISTER ADDRESS: 0x07h | | | | |
|-------------------------|------|---------|---|-------------------------|
| BIT | NAME | DEFAULT | | DESCRIPTION |
| D7 | | MSB | x | Reserved for future use |
| D6 | | | x | Reserved for future use |
| D5 | | | x | Reserved for future use |
| D4 | | | x | Reserved for future use |
| D3 | | | x | Reserved for future use |
| D2 | | | x | Reserved for future use |
| D1 | | | x | Reserved for future use |
| D0 | | LSB | x | Reserved for future use |

Register 0x08h, 0x09h Description Chip_ID:
Table 28. TPS6236x Register 0x08h and 0x09h Description

| REGISTER ADDRESS: 0x08h, 0x09 Read | | | | | |
|------------------------------------|------|---------|---|-------------|------------------|
| BIT | NAME | DEFAULT | | DESCRIPTION | |
| D7 | | MSB | 1 | Vendor ID | |
| D6 | | | 0 | | |
| D5 | | | 0 | | |
| D4 | | | 0 | | |
| D3 | | | x | D3-D2 | Part number ID |
| D2 | | | x | 00 | TPS62360 |
| | | | | 01 | TPS62361B |
| | | | | 10 | TPS62362 |
| D1 | | | x | D1-D0 | Chip revision ID |
| D0 | | | x | 00 | Rev. 1 |
| | | | | 01 | Rev. 2 |
| | | | | 10 | Rev. 3 |
| | | LSB | | 11 | Rev. 4 |

PACKAGE SUMMARY**CHIP SCALE PACKAGE
(TOP VIEW)****Code:**

- TI — Texas Instruments
- YM — Year Month date code
- LLLL — Lot trace code
- S — Assembly site code
- XXXXXXXX — Part number
 - TPS62360 = TPS62360
 - TPB62361 = TPS62361B
 - TPS62362 = TPS62362

Figure 49. Package Marking and Dimensions**CHIP SCALE PACKAGE DIMENSIONS**

The TPS6236x device is available in a 16-bump chip scale package (YZH, NanoFree™). The package dimensions are given as:

- D = 2.076mm (+/- 0.03mm)
- E = 2.076mm (+/- 0.03mm)

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| TPS62360YZHR | ACTIVE | DSBGA | YZH | 16 | 3000 | Green (RoHS & no Sb/Br) | Call TI | Level-1-260C-UNLIM | |
| TPS62360YZHT | ACTIVE | DSBGA | YZH | 16 | 250 | Green (RoHS & no Sb/Br) | Call TI | Level-1-260C-UNLIM | |
| TPS62361BYZHR | ACTIVE | DSBGA | YZH | 16 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |
| TPS62361BYZHT | ACTIVE | DSBGA | YZH | 16 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |
| TPS62362YZHR | ACTIVE | DSBGA | YZH | 16 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |
| TPS62362YZHT | ACTIVE | DSBGA | YZH | 16 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



www.ti.com

PACKAGE OPTION ADDENDUM

20-Aug-2011

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS62361BYZHR | DSBGA | YZH | 16 | 3000 | 180.0 | 8.4 | 2.18 | 2.18 | 0.81 | 4.0 | 8.0 | Q1 |
| TPS62362YZHR | DSBGA | YZH | 16 | 3000 | 180.0 | 8.4 | 2.18 | 2.18 | 0.81 | 4.0 | 8.0 | Q1 |
| TPS62362YZHT | DSBGA | YZH | 16 | 250 | 180.0 | 8.4 | 2.18 | 2.18 | 0.81 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

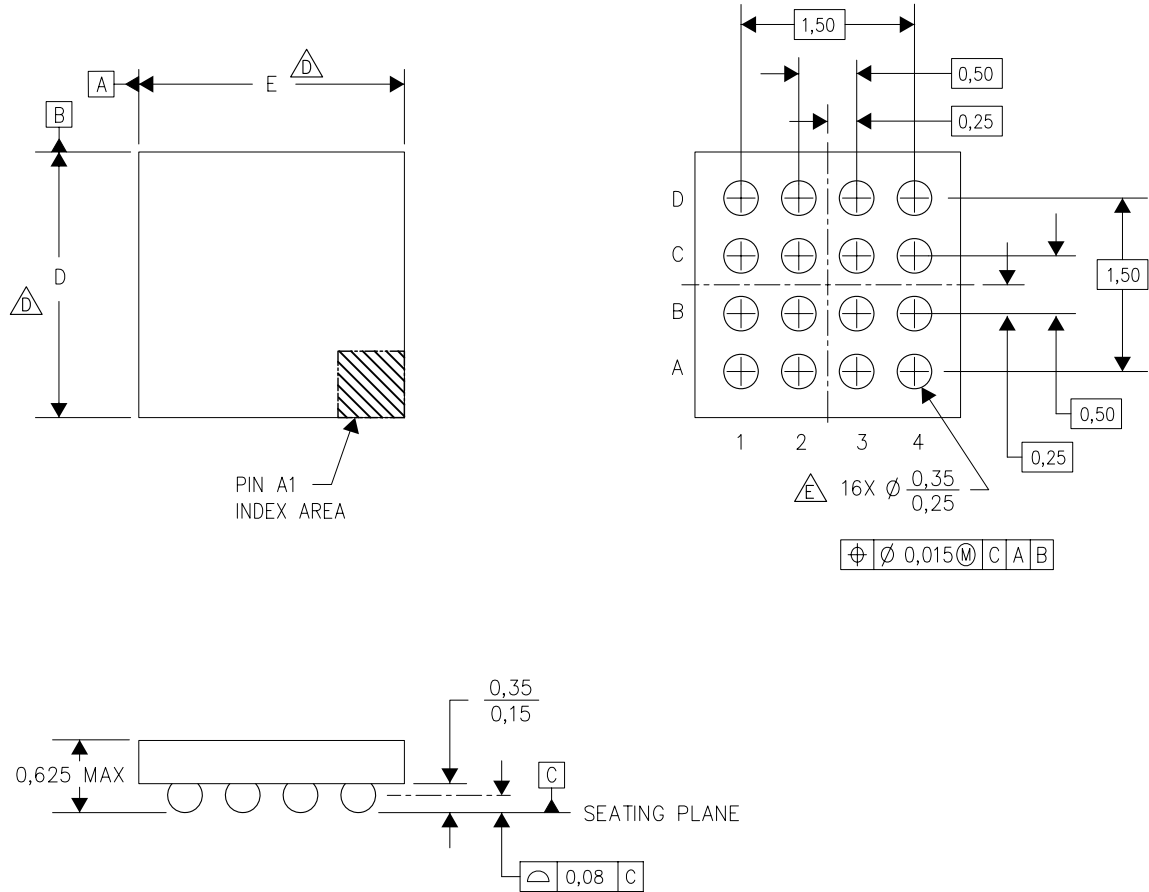


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS62361BYZHR | DSBGA | YZH | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS62362YZHR | DSBGA | YZH | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS62362YZHT | DSBGA | YZH | 16 | 250 | 210.0 | 185.0 | 35.0 |

YZH (S-XBGA-N16)

DIE-SIZE BALL GRID ARRAY



4205060/D 06/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. Devices in YZH package can have dimension D ranging from 1.94 to 2.65 mm and dimension E ranging from 1.94 to 2.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
4 x 4 matrix pattern is shown for illustration only.
 - F. This package contains lead-free balls.
Refer to YEH (Drawing #4204183) for tin-lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

| | |
|------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Mobile Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|--|
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Transportation and Automotive | www.ti.com/automotive |
| Video and Imaging | www.ti.com/video |

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated