# SN74CBT16233
## 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS010K – MAY 1995 – REVISED NOVEMBER 2001

- **Member of the Texas Instruments Widebus™ Family**
- **5-$\Omega$ Switch Connection Between Two Ports**
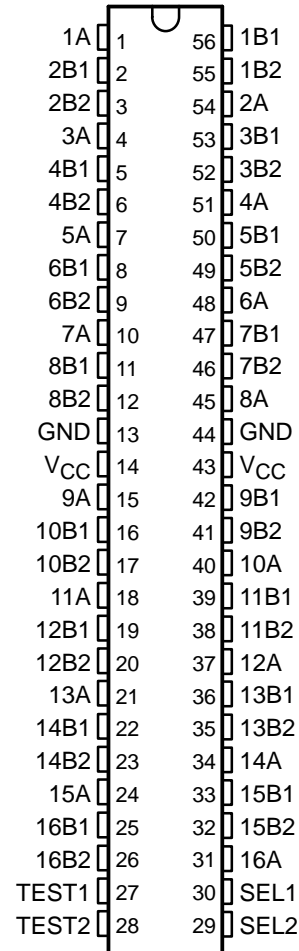- **TTL-Compatible Input Levels**

### description

The SN74CBT16233 is a 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The device can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select (SEL1 and SEL2) inputs control the data flow. When the TEST inputs are asserted, the A port is connected to both the B1 and the B2 ports. SEL1, SEL2, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.

This device is designed so it does not have through current when switching directions.

**DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| 1A | 1 | 56 | 1B1 |
| 2B1 | 2 | 55 | 1B2 |
| 2B2 | 3 | 54 | 2A |
| 3A | 4 | 53 | 3B1 |
| 4B1 | 5 | 52 | 3B2 |
| 4B2 | 6 | 51 | 4A |
| 5A | 7 | 50 | 5B1 |
| 6B1 | 8 | 49 | 5B2 |
| 6B2 | 9 | 48 | 6A |
| 7A | 10 | 47 | 7B1 |
| 8B1 | 11 | 46 | 7B2 |
| 8B2 | 12 | 45 | 8A |
| GND | 13 | 44 | GND |
| $V_{CC}$ | 14 | 43 | $V_{CC}$ |
| 9A | 15 | 42 | 9B1 |
| 10B1 | 16 | 41 | 9B2 |
| 10B2 | 17 | 40 | 10A |
| 11A | 18 | 39 | 11B1 |
| 12B1 | 19 | 38 | 11B2 |
| 12B2 | 20 | 37 | 12A |
| 13A | 21 | 36 | 13B1 |
| 14B1 | 22 | 35 | 13B2 |
| 14B2 | 23 | 34 | 14A |
| 15A | 24 | 33 | 15B1 |
| 16B1 | 25 | 32 | 15B2 |
| 16B2 | 26 | 31 | 16A |
| TEST1 | 27 | 30 | SEL1 |
| TEST2 | 28 | 29 | SEL2 |

### ORDERING INFORMATION

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SSOP – DL | Tube | SN74CBT16233DL | CBT16233 |
| | | Tape and reel | SN74CBT16233DLR | |
| | TSSOP – DGG | Tape and reel | SN74CBT16233DGGR | CBT16233 |
| | TVSOP – DGV | Tape and reel | SN74CBT16233DGVR | CY233 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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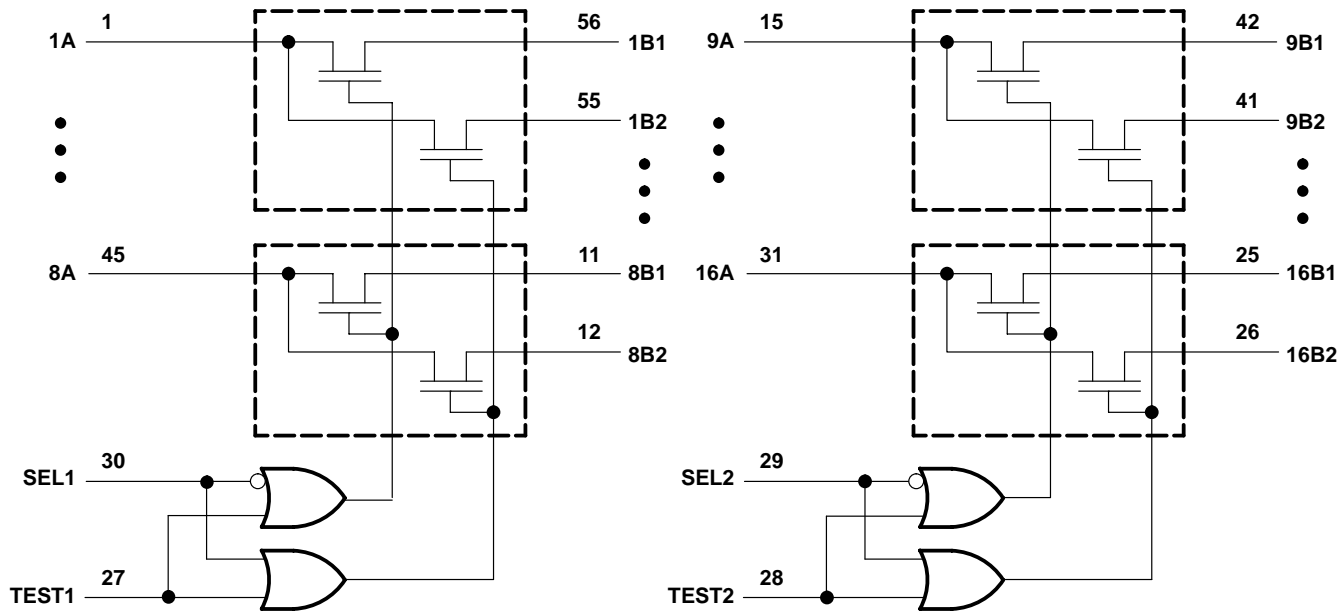POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

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# 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

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**FUNCTION TABLE**
**(each multiplexer/demultiplexer)**

| INPUTS | | FUNCTION |
|---|---|---|
| SEL | TEST | |
| L | L | A = B1 |
| H | L | A = B2 |
| X | H | A = B1 and A = B2 |

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ......................................................... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ........................................ −0.5 V to $V_{CC}$ + 0.5 V
Continuous channel current ....................................................... 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) ............................................... −50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package ........................... 64°C/W
               DGV package ........................... 48°C/W
               DL package ........................... 56°C/W
Storage temperature range, $T_{stg}$ ............................................ −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
    2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.75 | 5.25 | V |
| $V_{IH}$ | High-level control input voltage | 2 | | V |
| $V_{IL}$ | Low-level control input voltage | | 0.8 | V |
| $T_A$ | Operating free-air temperature | −40 | 85 | °C |

NOTE 3: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP[†] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.75 V, | $I_I$ = −18 mA | | | | −1.2 | V |
| $I_I$ | | $V_{CC}$ = 0, | $V_I$ = 5.25 V | | | | 10 | µA |
| | | $V_{CC}$ = 5.25 V, | $V_I$ = 5.25 V or GND | | | | ±1 | µA |
| $I_{CC}$ | | $V_{CC}$ = 5.25 V, | $I_O$ = 0, | $V_I$ = $V_{CC}$ or GND | | | 3 | µA |
| $\Delta I_{CC}$[‡] | Control inputs | $V_{CC}$ = 5.25 V, | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 2.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 3 V or 0 | | | | 4.5 | | pF |
| $C_{io(OFF)}$ | | $V_O$ = 3 V or 0 | | | | 4 | | pF |
| $r_{on}$[§] | | $V_{CC}$ = 4.75 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 7 | Ω |
| | | | | $I_I$ = 30 mA | | 5 | 7 | |
| | | | $V_I$ = 2.4 V, | $I_I$ = 15 mA | | 7 | 12 | |

[†] All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
[§] Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

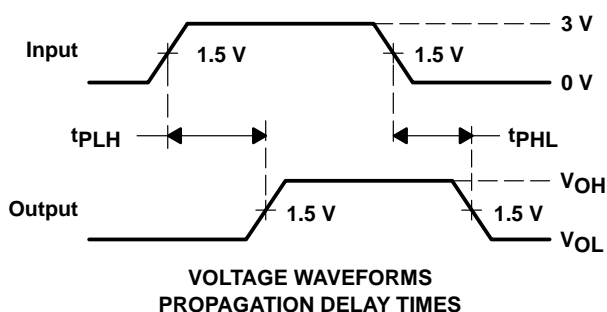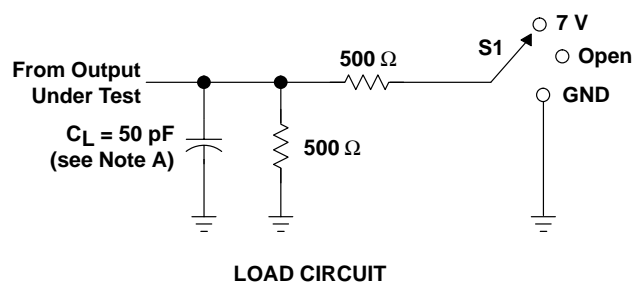| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{pd}$[¶] | A or B | B or A | | 0.25 | ns |
| $t_{pd}$ | SEL | A | 1.6 | 5.3 | ns |
| $t_{en}$ | TEST or SEL | B | 1.3 | 5.2 | ns |
| $t_{dis}$ | TEST or SEL | B | 1 | 5.3 | ns |

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
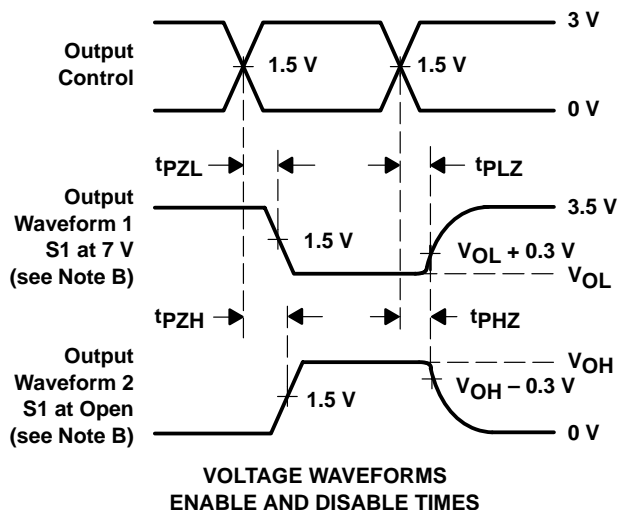
## PARAMETER MEASUREMENT INFORMATION

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

**LOAD CIRCUIT**

**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O$ = 50 $\Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

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## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| 74CBT16233DGGRE4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74CBT16233DGVRE4 | ACTIVE | TVSOP | DGV | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74CBT16233DGVRG4 | ACTIVE | TVSOP | DGV | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBT16233DGGR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBT16233DGVR | ACTIVE | TVSOP | DGV | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBT16233DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBT16233DLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBT16233DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBT16233DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
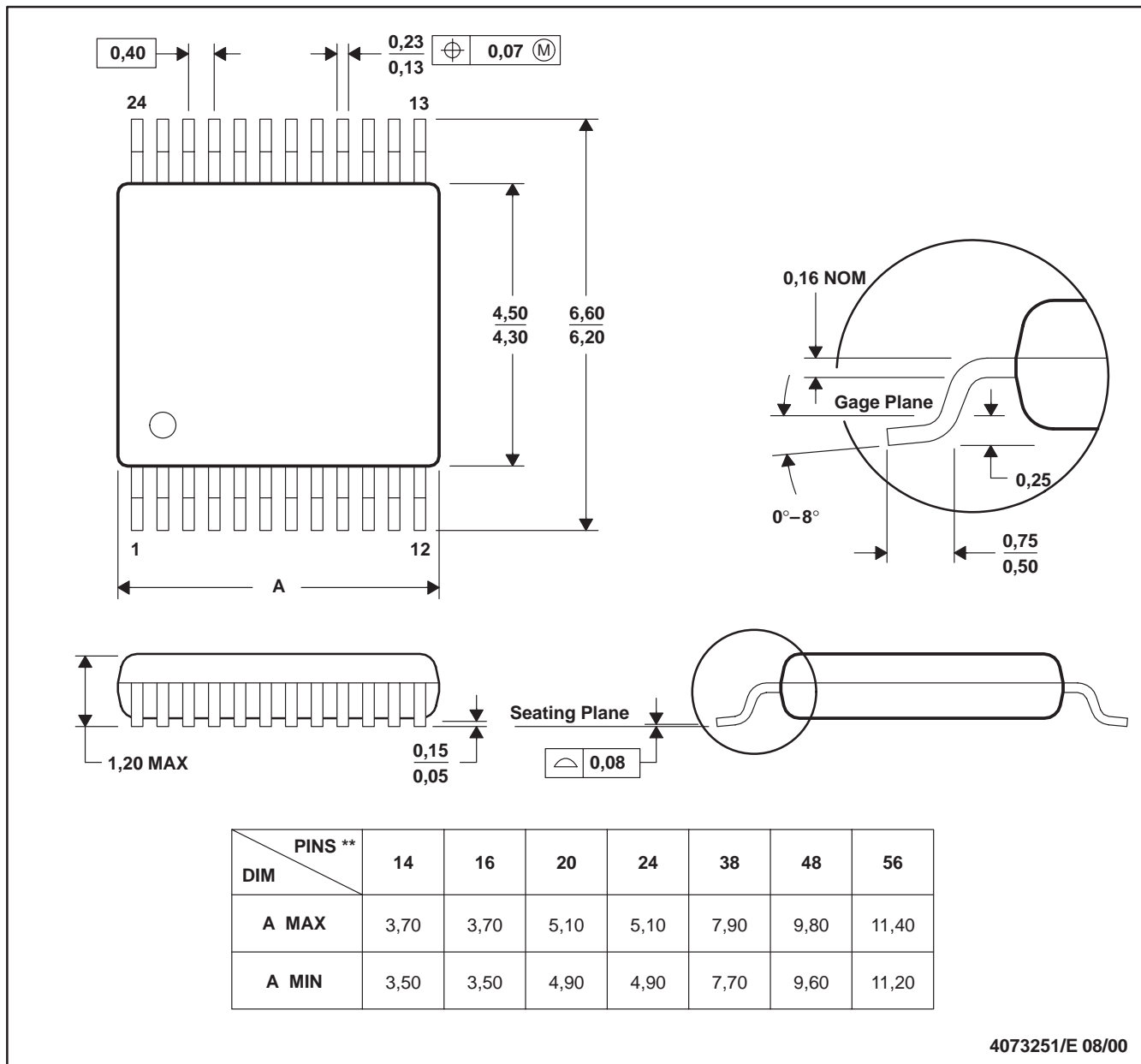
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**DGV (R-PDSO-G\*\*)**　　　　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**



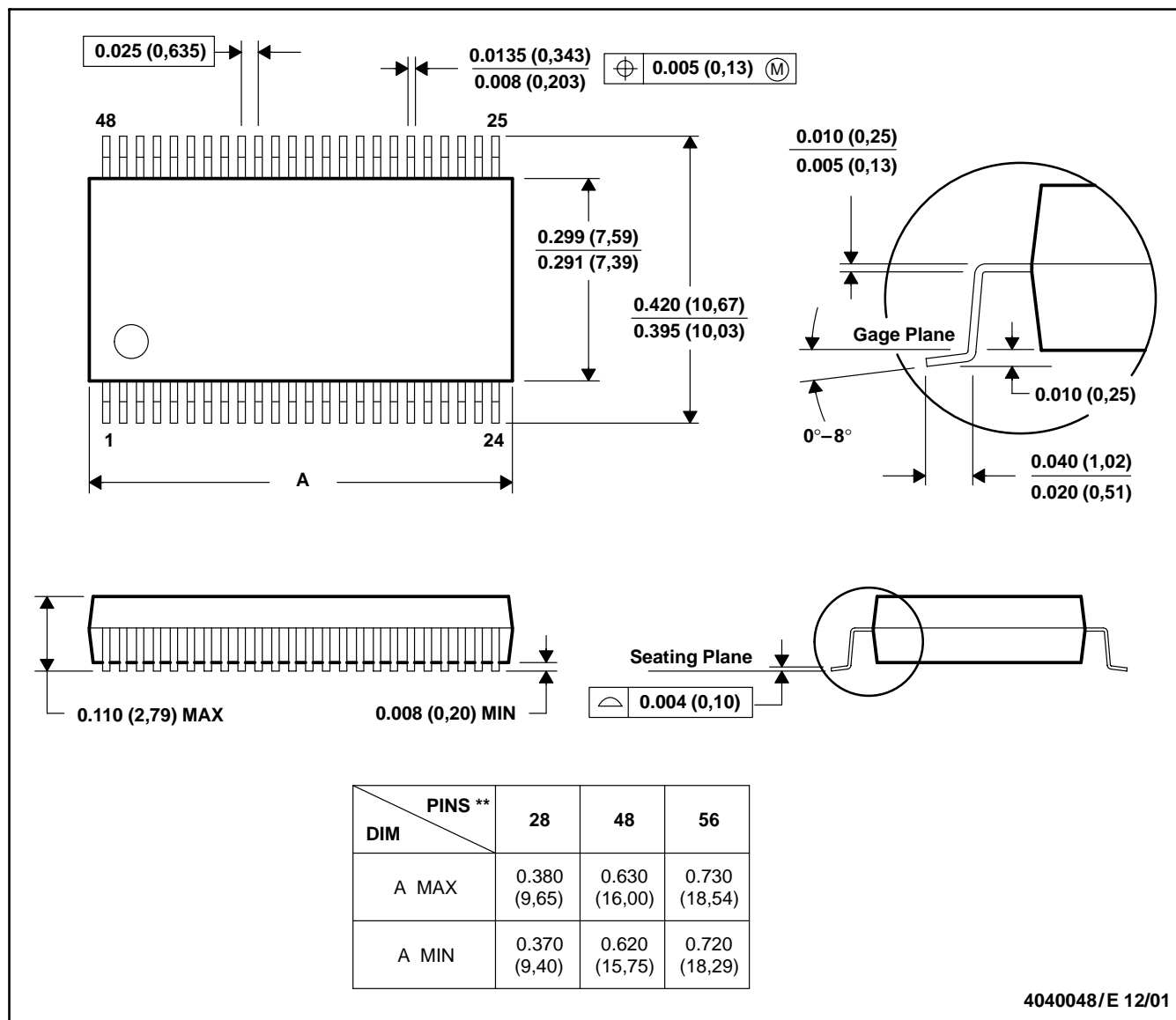| DIM \ PINS \*\* | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

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**DL (R-PDSO-G**\*\***)**                                      **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

48                                          25

0.299 (7,59)
0.291 (7,39)

0.420 (10,67)
0.395 (10,03)

0.010 (0,25)
0.005 (0,13)

**Gage Plane**

0°–8°

0.010 (0,25)

0.040 (1,02)
0.020 (0,51)

1                                           24

**A**

0.110 (2,79) MAX                   0.008 (0,20) MIN

**Seating Plane**

⌒ 0.004 (0,10)

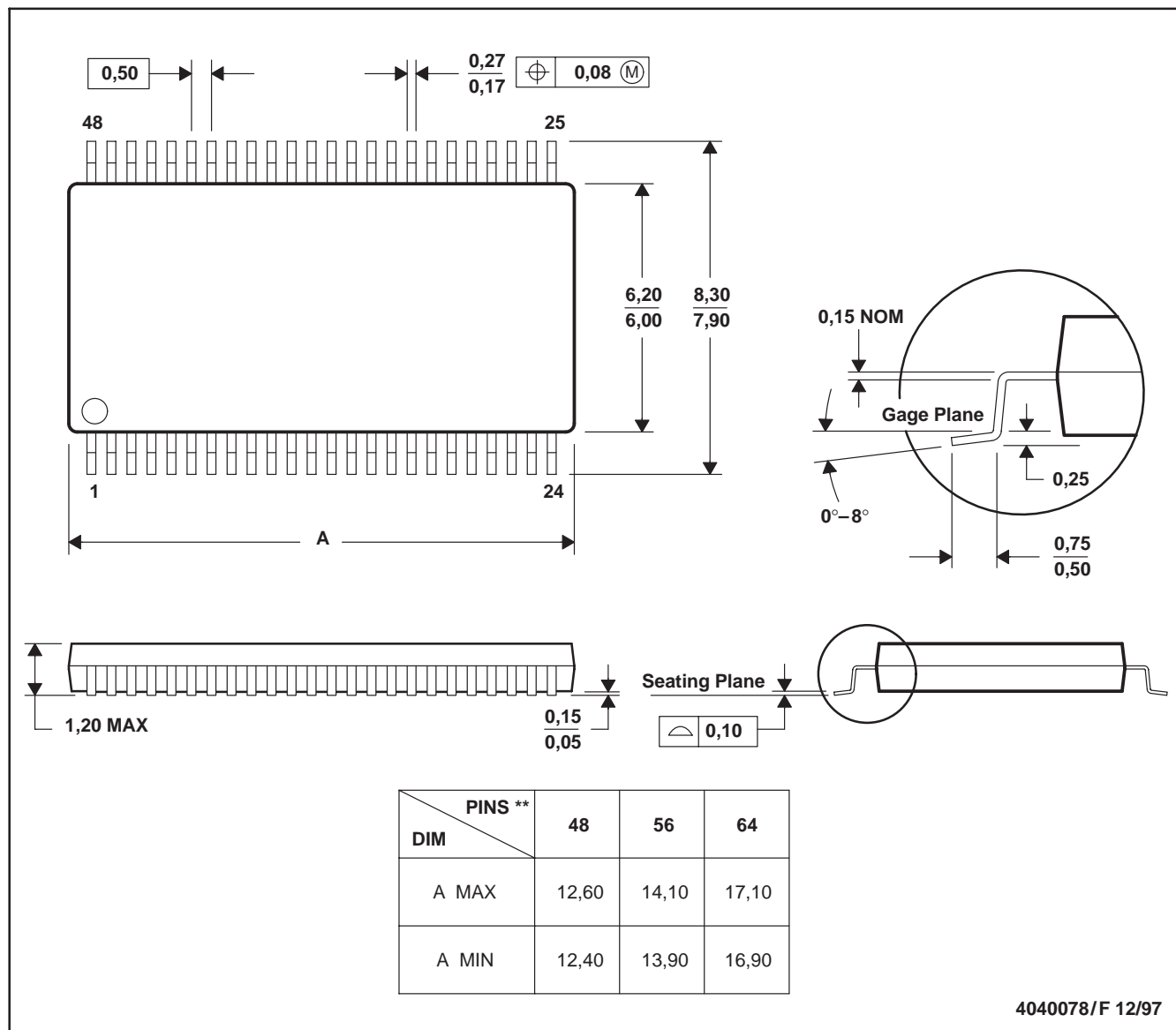| PINS ** DIM | 28 | 48 | 56 |
|---|---|---|---|
| A MAX | 0.380 (9,65) | 0.630 (16,00) | 0.730 (18,54) |
| A MIN | 0.370 (9,40) | 0.620 (15,75) | 0.720 (18,29) |

**4040048/E 12/01**

NOTES:  A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

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**DGG (R-PDSO-G\*\*)**                                        **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**

0,50

0,27
0,17

⊕  0,08  Ⓜ

48                                    25

6,20
6,00

8,30
7,90

0,15 NOM

**Gage Plane**

0°–8°

0,25

0,75
0,50

1                                     24

**A**

1,20 MAX

0,15
0,05

**Seating Plane**

△ 0,10

| PINS \*\* DIM | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

**4040078 / F 12/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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