

## 4.5-V to 14-V Input High-Current Synchronous Buck Converter

Check for Samples: [TPS56121](#)

### FEATURES

- 4.5-V to 14-V Input Voltage Range
- Incorporates Power Block Technology
- Up to 15-A Output Current
- Fixed Frequency Options of 300 kHz, 500 kHz and 1 MHz
- High-Side and Low-Side MOSFET  $R_{DS(on)}$  Sensing
- Programmable Soft-Start
- 600-mV Reference Voltage with 1% Accuracy
- Voltage Mode Control with Feed-Forward
- Supports Pre-Biased Output
- Thermal Shutdown
- 22-Pin 5 mm x 6 mm PQFN PowerPAD™ Package

### APPLICATIONS

- Point-of-Load (POL) Power Modules
- High Density DC-DC Converters for Telecom and Networking Applications

### DESCRIPTION

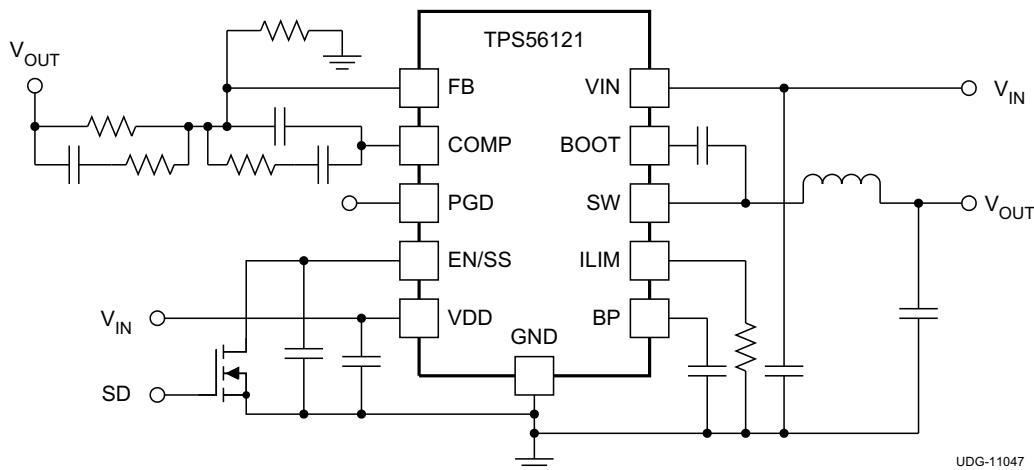
TPS56121 is a high-efficiency and high-current synchronous buck converter designed to operate from a supply between 4.5 V and 14 V. The device is capable of producing an output voltage as low as 0.6 V at loads up to 15 A. Integrated NexFET™ Power MOSFETs provide a small foot print and ease of use.

The device implements a voltage-mode control with voltage feed-forward compensation that responds instantly to input voltage change.

TPS56121 is available in a thermally enhanced 22-pin PQFN (DQP) PowerPAD™ package.

The device offers design flexibility with a variety of user programmable functions, including soft-start, overcurrent protection (OCP) levels, and loop compensation. OCP levels are programmed by a single external resistor connected from the ILIM pin to the circuit ground. During the initial power-on sequence, the device enters a calibration cycle, measures the voltage at the ILIM pin, and sets an internal OCP voltage level. During operation, the programmed OCP voltage level is compared to the voltage drop across the low-side FET when it is on to determine whether there is an overcurrent condition. It then enters a shutdown/restart cycle until the fault is removed.

### SIMPLIFIED APPLICATION



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE	PINS	TRANSPORT MEDIA	MINIMUM QUANTITY	ORDERABLE NUMBER
-40°C to 150°C	Plastic QFN (DQP)	22	Tape-and-reel	250	TPS56121DQPT
				2500	TPS56121DQPR

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		VALUE		UNIT
		MIN	TYP	
Voltage Range	VDD, VIN	-0.3	16.5	V
	SW	-3	25	
	SW (< 100 ns pulse width, 10 $\mu$ J)	-5		
	BOOT	-0.3	30	
	BOOT-SW (differential from BOOT to SW)	-0.3	7	
	COMP, PGOOD, FB, BP, EN/SS, ILIM	-0.3	7	
Electrostatic discharge	(HBM) QSS 009-105 (JESD22-A114A)		2	kV
	(CBM) QSS 009-147 (JESD22-C101B.01)		1.5	
Temperature	Junction, T <sub>J</sub>	-40	150	°C
	Storage, T <sub>stg</sub>	-55	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS56121	UNITS
		PQFN	
		22 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	34.6	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	22.9	
$\Psi_{JT}$	Junction-to-top characterization parameter	0.6	
$\Psi_{JB}$	Junction-to-board characterization parameter	5.0	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	0.3	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
V <sub>DD</sub> VIN Input voltage	4.5		14	V
T <sub>J</sub> Operating junction temperature	-40		125	°C

**ELECTRICAL CHARACTERISTICS**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE						
V <sub>FB</sub>	FB input voltage	T <sub>J</sub> = 25°C, 4.5 V ≤ V <sub>VDD</sub> ≤ 14 V	597	600	603	mV
		–40°C ≤ T <sub>J</sub> ≤ 125°C, 4.5 V ≤ V <sub>VDD</sub> ≤ 14 V	594	600	606	
INPUT SUPPLY						
V <sub>VDD</sub>	Input supply voltage range		4.5		14	V
IVDDSD	Shutdown supply current	V <sub>EN/SS</sub> = 0.2 V		80	120	μA
IVDDQ	Quiescent, non-switching	Let EN/SS float, V <sub>FB</sub> = 1 V		2.5	5.0	mA
V <sub>UVLO</sub>	UVLO ON Voltage		4.0		4.3	V
V <sub>UVLO(HYS)</sub>	UVLO hysteresis		500		700	mV
ENABLE/SOFT-START						
V <sub>IH</sub>	High-level input voltage, EN/SS		0.55	0.70	1.00	V
V <sub>IL</sub>	Low-level input voltage, EN/SS		0.27	0.30	0.33	V
I <sub>SS</sub>	Soft-start source current		8	10	12	μA
V <sub>SS</sub>	Soft-start voltage level – Start of ramp		0.4	0.8	1.3	V
BP REGULATOR						
V <sub>BP</sub>	Output voltage	I <sub>BP</sub> = 10 mA	6.2	6.5	6.8	V
V <sub>DO</sub>	Regulator dropout voltage, V <sub>VDD</sub> – V <sub>BP</sub>	I <sub>BP</sub> = 25 mA, V <sub>VDD</sub> = 4.5 V		70	125	mV
OSCILLATOR						
f <sub>SW</sub>	Switching Frequency	R <sub>COMP</sub> = 40.2 kΩ, 4.5 V ≤ V <sub>VDD</sub> ≤ 14 V	270	300	330	kHz
		R <sub>COMP</sub> = open, 4.5 V ≤ V <sub>VDD</sub> ≤ 14 V	450	500	550	kHz
		R <sub>COMP</sub> = 13.3 kΩ, 4.5 V ≤ V <sub>VDD</sub> ≤ 14 V	0.8	0.95	1.1	MHz
V <sub>RAMP</sub> <sup>(1)</sup>	Ramp amplitude		V <sub>VDD</sub> /6.6	V <sub>VDD</sub> /6	V <sub>VDD</sub> /5.4	V
PWM						
D <sub>MAX</sub> <sup>(1)</sup>	Maximum duty cycle	f <sub>SW</sub> = 300 kHz, V <sub>FB</sub> = 0 V, 4.5 V ≤ V <sub>VDD</sub> ≤ 14 V	93%			
		f <sub>SW</sub> = 500 kHz, V <sub>FB</sub> = 0 V, 4.5 V ≤ V <sub>VDD</sub> ≤ 14 V	90%			
		f <sub>SW</sub> = 1 MHz, V <sub>FB</sub> = 0 V, 4.5 V ≤ V <sub>VDD</sub> ≤ 14 V	85%			
t <sub>ON(min)</sub> <sup>(1)</sup>	Minimum controllable pulse width				100	ns
ERROR AMPLIFIER						
GBWP <sup>(1)</sup>	Gain bandwidth product		10	24		MHz
A <sub>OL</sub> <sup>(1)</sup>	Open loop gain		60			dB
I <sub>IB</sub>	Input bias current (current out of FB pin)	V <sub>FB</sub> = 0.6 V			75	nA
I <sub>EAOP</sub>	Output source current	V <sub>FB</sub> = 0 V	1.5			mA
I <sub>EAOM</sub>	Output sink current	V <sub>FB</sub> = 1 V	1.5			mA
POWER GOOD						
V <sub>OV</sub>	Feedback upper voltage limit for PGOOD		655	675	700	mV
V <sub>UV</sub>	Feedback lower voltage limit for PGOOD		500	525	550	
V <sub>PGD-HYST</sub>	PGOOD hysteresis voltage at FB			30	45	
R <sub>PGD</sub>	PGOOD pull down resistance	V <sub>FB</sub> = 0 V, I <sub>FB</sub> = 5 mA		30	70	Ω
I <sub>PGDLK</sub>	PGOOD leakage current	550 mV < V <sub>FB</sub> < 655 mV, V <sub>PGOOD</sub> = 5 V		10	20	μA

(1) Ensured by design. Not production tested

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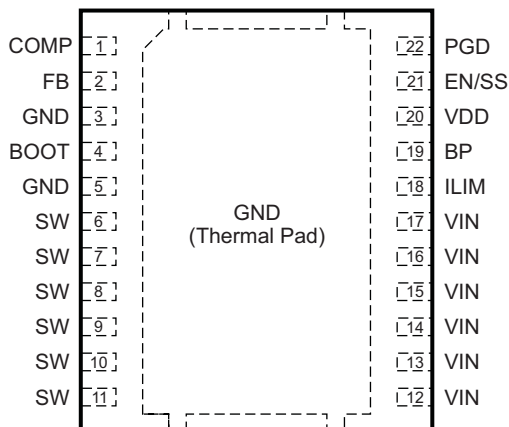
## ELECTRICAL CHARACTERISTICS (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>OUTPUT STAGE</b>						
R <sub>HI</sub>	High-side device resistance	T <sub>J</sub> = 25°C, (V <sub>BOOT</sub> – V <sub>SW</sub> ) = 5.5 V		4.5	6.5	mΩ
R <sub>LO</sub>	Low side device resistance	T <sub>J</sub> = 25°C		1.9	2.7	
<b>OVERCURRENT PROTECTION (OCP)</b>						
t <sub>PSSC(min)</sub> <sup>(2)</sup>	Minimum pulse time during short circuit			250		ns
t <sub>BLNKH</sub> <sup>(2)</sup>	Switch leading-edge blanking pulse time (high-side detection)			150		
I <sub>OCH</sub>	OC threshold for high-side FET	T <sub>J</sub> = 25°C, (V <sub>BOOT</sub> – V <sub>SW</sub> ) = 5.5 V	27	34	39	A
I <sub>LIM</sub>	ILIM current source	T <sub>J</sub> = 25°C		10.0		μA
V <sub>OCLPRO</sub> <sup>(2)</sup>	Programmable OC range for low side FET	T <sub>J</sub> = 25°C	12		100	mV
t <sub>OFF</sub>	OC retry cycles on EN/SS pin			4		Cycle
<b>BOOT DIODE</b>						
V <sub>DFWD</sub>	Bootstrap diode forward voltage	I <sub>BOOT</sub> = 5 mA		0.8		V
<b>THERMAL SHUTDOWN</b>						
T <sub>JSD</sub> <sup>(2)</sup>	Junction shutdown temperature			145		°C
T <sub>JSDH</sub> <sup>(2)</sup>	Hysteresis			20		°C

(2) Ensured by design. Not production tested

## DEVICE INFORMATION

### DQP PACKAGE PQFN-22 (TOP VIEW)



Note: The thermal pad is also an electrical ground connection.

## PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	4	O	Gate drive voltage for the high-side FET. A 100-nF capacitor (typical) must be connected between this pin and the SW pin. To reduce a voltage spike at SW, a BOOT resistance between 5 $\Omega$ to 10 $\Omega$ may be placed in series with the BOOT capacitor to slow down start-up of the high-side FET.
BP	19	O	Output bypass for the internal regulator. Connect a low-ESR bypass ceramic capacitor of 1 $\mu$ F or greater from this pin to GND.
COMP	1	O	Output of the error amplifier and connection node for loop feedback components. Optionally, a 40.2 k $\Omega$ resistor from this pin to GND sets switching frequency to 300KHz instead of the default value of 500KHz; while a 13.3 k $\Omega$ resistor from this pin to GND sets switching frequency to 1 MHz.
EN/SS	21	I	Logic-level input starts or stops the controller via an external user command. Allowing this pin to float turns the controller on. Pulling this pin low disables the controller. This is also the soft-start programming pin. A capacitor connected from this pin to GND programs the soft-start time. The capacitor is charged with an internal current source of 10 $\mu$ A. The resulting voltage ramp of this pin is also used as a second non-inverting input to the error amplifier after a 0.8 V (typical) level shift downwards. Output regulation is controlled by the internal level shifted voltage ramp until that voltage reaches the internal reference voltage of 600 mV. The voltage ramp of this pin reaches 1.4 V (typical).
FB	2	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage.
GND	3	–	Ground reference for the device
	5		
GND	Thermal Pad	–	Ground reference for the device. This is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first is to provide an electrical ground connection for the device. The second is to provide a low thermal impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.
ILIM	18	I	A resistor connected from this pin to GND sets the overcurrent threshold for the device (the low-side FET).
PGD	22	O	Open drain power good output.
SW	6	I	Sense line for the adaptive anti-cross conduction circuitry. Acts as the common connection for the flying high-side FET driver.
	7		
	8		
	9		
	10		
	11		
VDD	20	I	Power input to the controller. A low-ESR bypass ceramic capacitor of 1 $\mu$ F should be connected from this pin close to GND.

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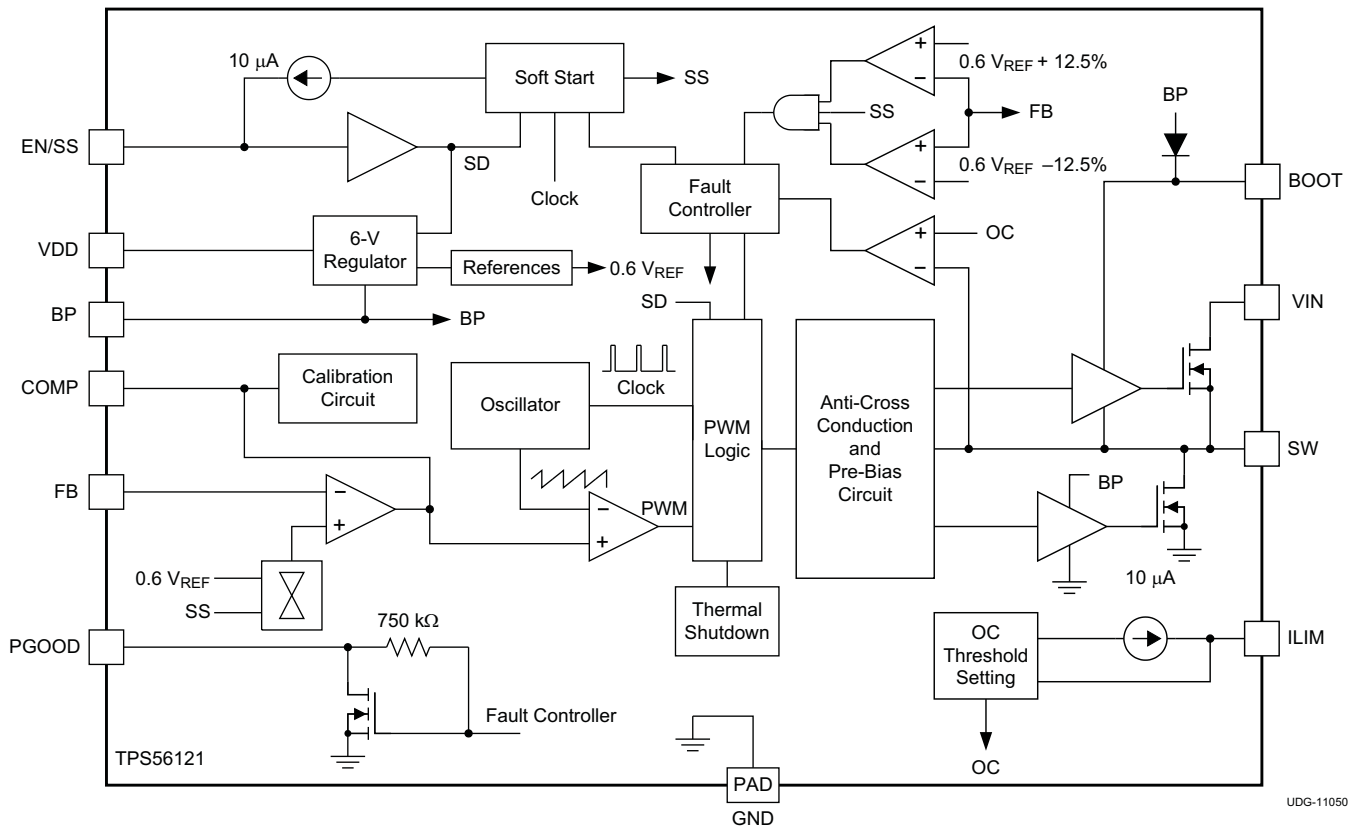
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## PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	12	I	Power input to the high-side FET.
	13		
	14		
	15		
	16		
	17		

## FUNCTIONAL BLOCK DIAGRAM



UDG-11050

## TYPICAL CHARACTERISTICS

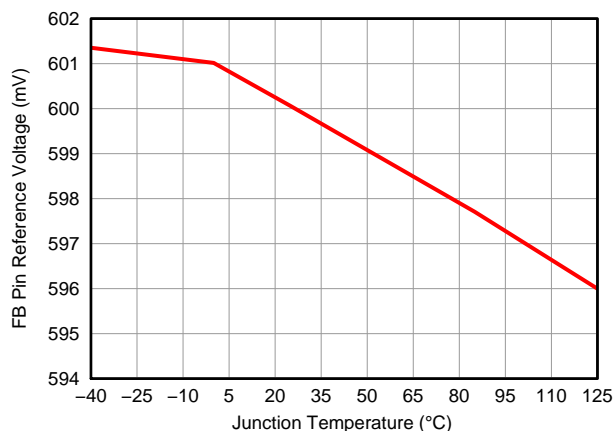


Figure 1. Reference Voltage vs. Junction Temperature

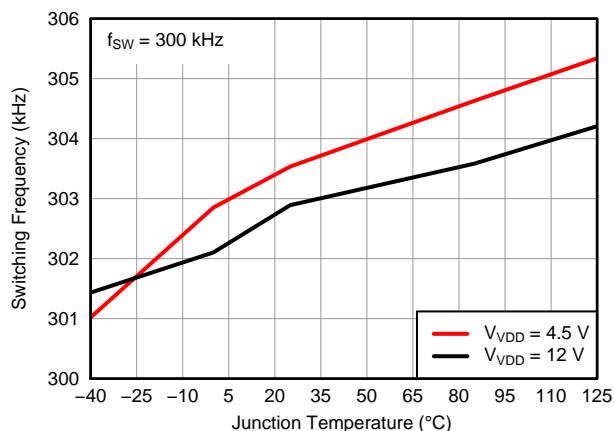


Figure 2. Switching Frequency vs. Junction Temperature (300 kHz)

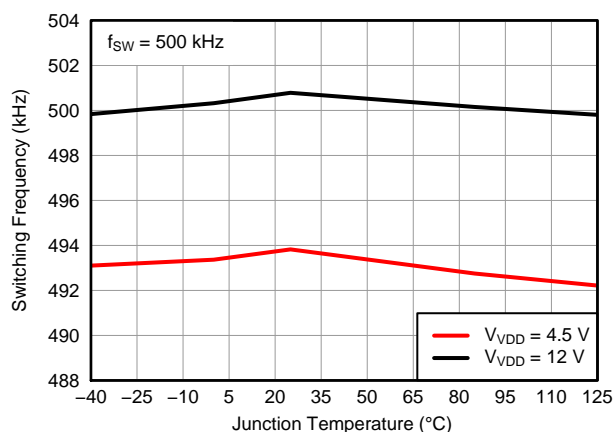


Figure 3. Switching Frequency vs. Junction Temperature (500 kHz)

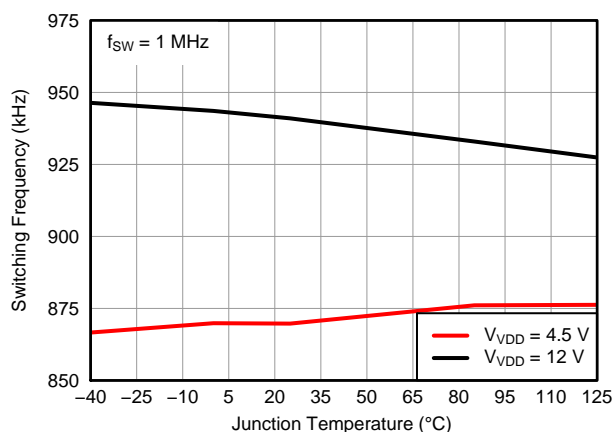


Figure 4. Switching Frequency vs. Junction Temperature (1 MHz)

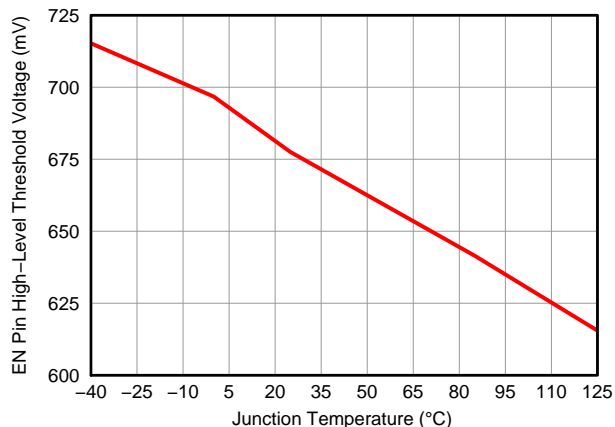


Figure 5. EN Pin High-Level Threshold Voltage vs. Junction Temperature

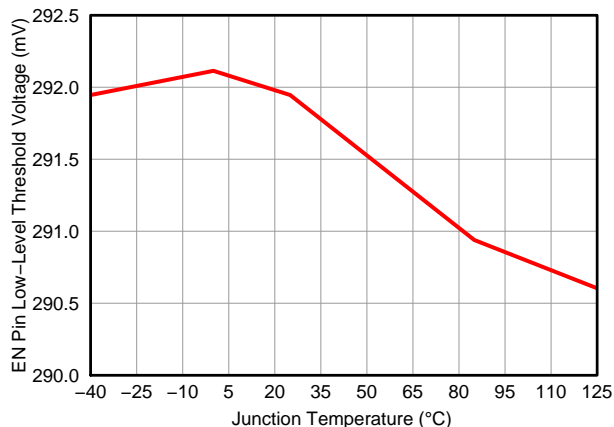
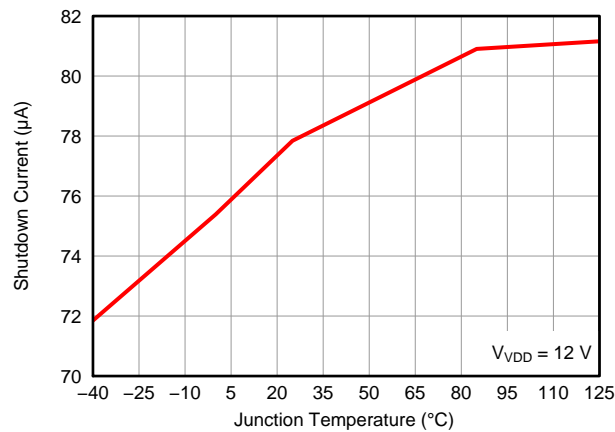
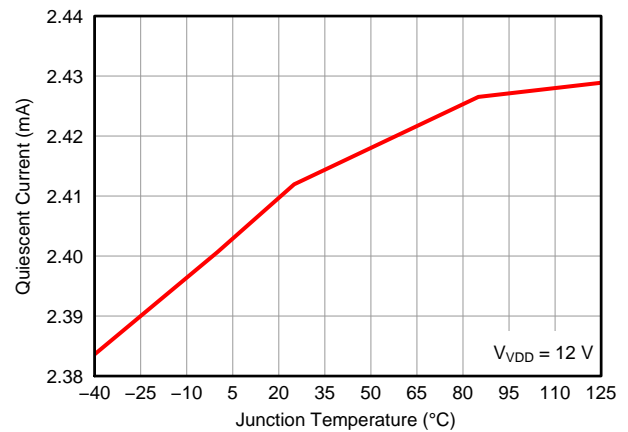


Figure 6. EN Pin Low-Level Threshold Voltage vs. Junction Temperature

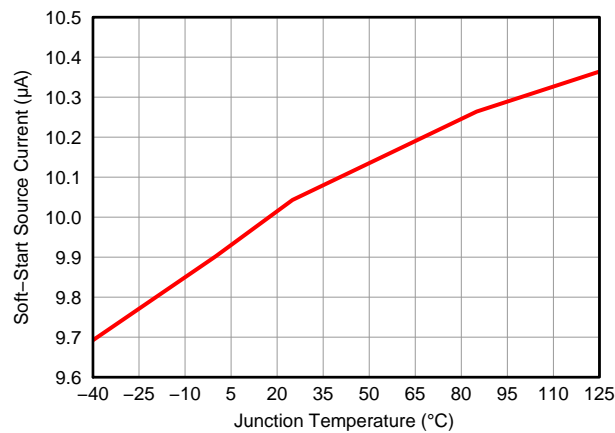
# **TYPICAL CHARACTERISTICS (continued)**



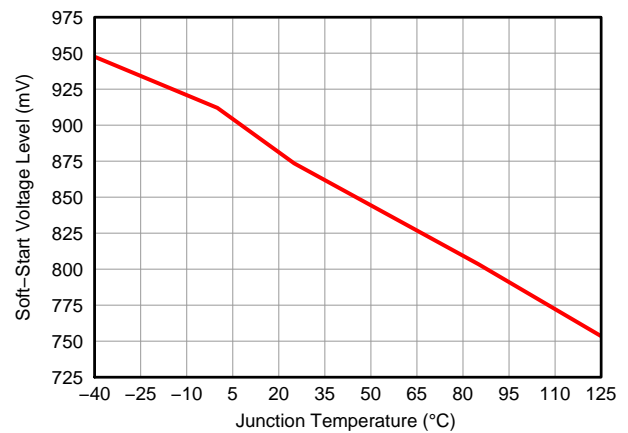
**Figure 7. Shutdown Current vs. Junction Temperature**



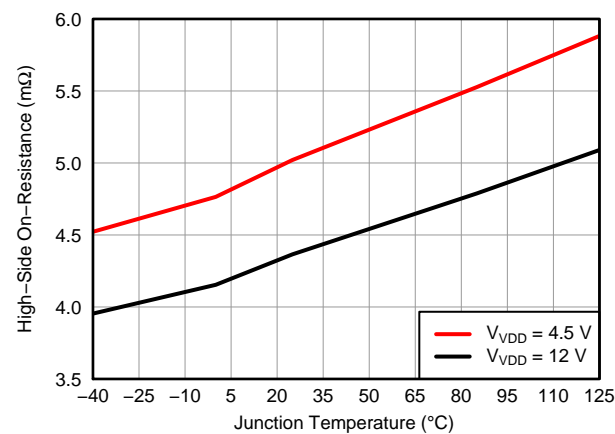
**Figure 8. Quiescent Current vs. Junction Temperature**



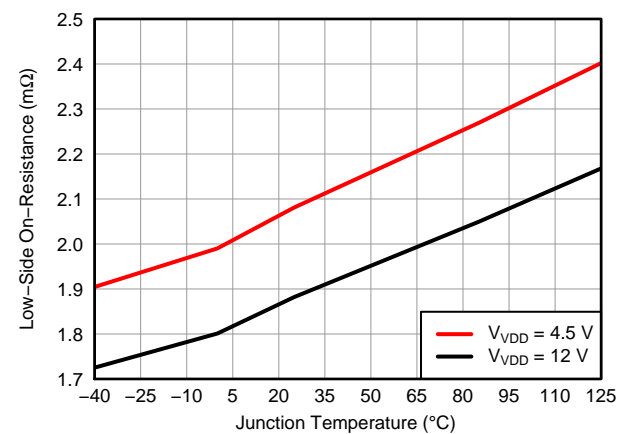
**Figure 9. Soft-Start Source vs. Junction Temperature**



**Figure 10. Soft-Start Voltage Level vs. Junction Temperature**



**Figure 11. High-Side On Resistance vs. Junction Temperature**



**Figure 12. Low-Side On Resistance vs. Junction Temperature**



## TYPICAL CHARACTERISTICS

The efficiency curve shown in Figure 15 is measured with a 0.5- $\mu$ H output inductor and a maximum DCR of 0.75 m $\Omega$ . The efficiency curve shown in Figure 16 is measured with a 0.3- $\mu$ H output inductor and a maximum DCR of 0.54 m $\Omega$ . The power derating curves shown in Figure 17 and Figure 18 are measured on a 4"  $\times$  3.25", 0.062" thick FR4 board with 6 layers and 1 oz. copper.

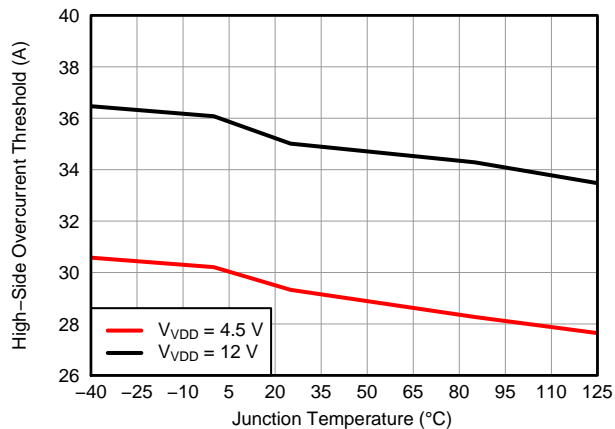


Figure 13. High-Side Overcurrent Threshold vs. Junction Temperature

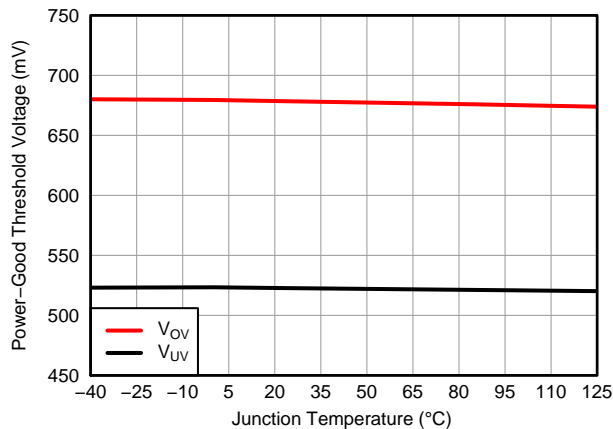


Figure 14. Power Good Threshold Voltage vs. Junction Temperature

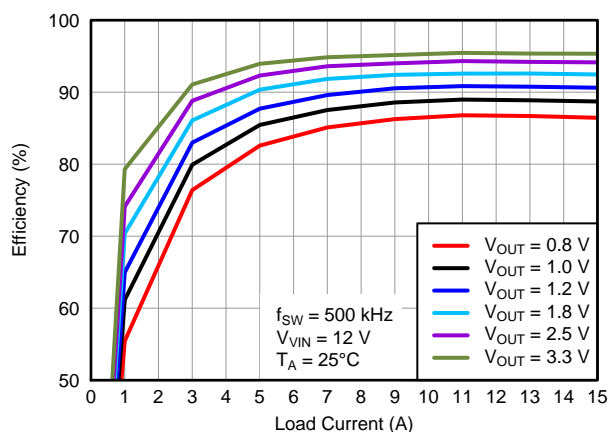


Figure 15. Efficiency vs. Load Current ( $V_{IN} = 12$  V)

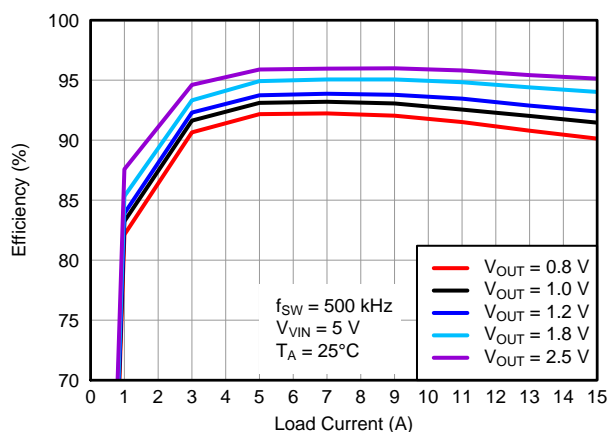


Figure 16. Efficiency vs. Load Current ( $V_{IN} = 5$  V)

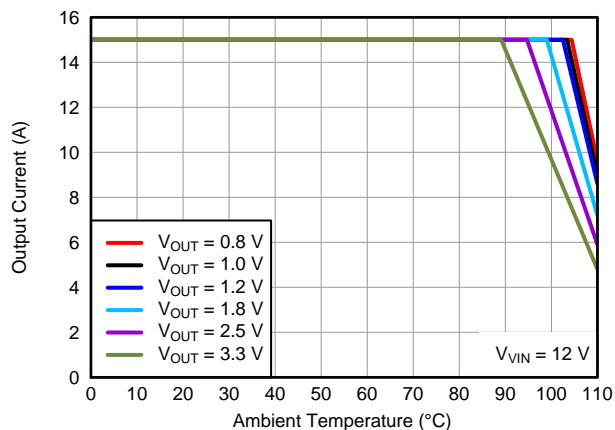


Figure 17. Output Current vs. Ambient Temperature ( $V_{IN} = 12$  V)

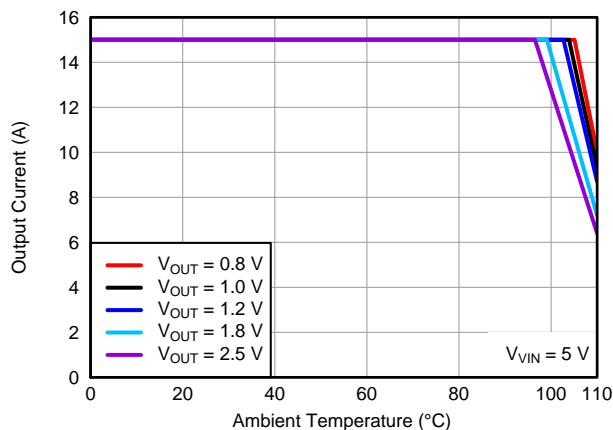


Figure 18. Output Current vs. Ambient Temperature ( $V_{IN} = 5$  V)

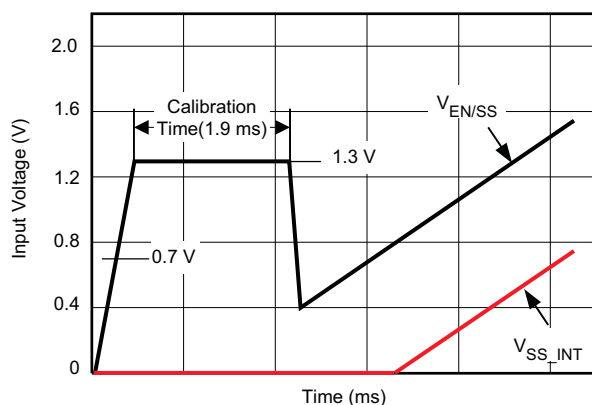
## APPLICATION INFORMATION

### Introduction

The TPS56121 is a 15-A high performance synchronous buck converter with two integrated N-channel NexFET™ power MOSFETs. The device implements a voltage-mode control with voltage feed-forward compensation that responds instantly to input voltage change. Pre-bias capability eliminates concerns about damaging sensitive loads.

### Voltage Reference

The 600-mV bandgap cell is internally connected to the non-inverting input of the error amplifier. The reference voltage is trimmed with the error amplifier in a unity gain configuration to remove amplifier offset from the final regulation voltage. The 1% tolerance on the reference voltage allows the user to design a very accurate power supply.



**Figure 19. Startup Sequence and Timing**

### Enable Functionality, Startup Sequence and Timing

After input power is applied, an internal 40- $\mu$ A current source begins to charge the soft-start capacitor connected from EN/SS to GND. When the voltage across that capacitor increases to 0.7 V, it enables the internal BP regulator followed by a calibration. Total calibration time is approximately 1.9 ms. See Figure 19. During the calibration, the device performs the following two functions.

#### COMP Pin Impedance Sensing

The device samples the impedance at the COMP pin and determines the appropriate operating switching frequency. If there is no resistor connected from the COMP pin to GND, the switching frequency is set to the default value of 500 kHz. If a resistor of 40.2 k $\Omega$   $\pm$  10% is connected from the COMP pin to GND, the switching frequency is set to 300 kHz. Alternatively, if a resistor of 13.3 K  $\pm$  10% is connected from the COMP pin to GND, the switching frequency is set to 1 MHz.

After a 1.1-ms time period, the COMP pin is then brought low for 0.8 ms. This ensures that the feedback loop is preconditioned at startup and no sudden output rise occurs at the output of the converter when it is allowed to start switching.

#### Overcurrent Protection (OCP) setting

The device sources 10  $\mu$ A (typical) to the resistor connected from the ILIM pin to GND. The voltage developed across that resistor multiplied by a factor of 2 is then sampled and latched off internally as the OCP trip level for the low-side FET until one cycles the input or toggles the EN/SS.

The voltage at EN/SS is internally clamped to 1.3 V before and/or during calibration to minimize the discharging

time once calibration is complete. The discharging current is from an internal current source of 140  $\mu\text{A}$  and it pulls the voltage down to 0.4 V. It then initiates the soft-start by charging up the capacitor using an internal current source of 10  $\mu\text{A}$ . The resulting voltage ramp on this pin is used as a second non-inverting input to the error amplifier after an 800 mV (typical) downward level-shift; therefore, the actual soft-start does not take place until the voltage at this pin reaches 800 mV.

If the EN/SS pin is left floating, the controller starts automatically. EN/SS must be pulled down to less than 270 mV to ensure that the chip is in shutdown mode.

### Soft-Start Time

The soft-start time of the TPS56121 is user programmable by selecting a single capacitor. The EN/SS pin sources 10  $\mu\text{A}$  to charge this capacitor. The actual output ramp-up time is the amount of time that it takes for the 10  $\mu\text{A}$  to charge the capacitor through a 600 mV range. There is some initial lag due to calibration and an offset (800 mV) from the actual EN/SS pin voltage to the voltage applied to the error amplifier.

The soft-start is accomplished in a closed-loop, meaning that the error amplifier controls the output voltage at all times during the soft-start period and the feedback loop is never open as occurs in duty cycle limit soft-start schemes. The error amplifier has two non-inverting inputs, one connected to the 600-mV reference voltage, and the other connected to the offset EN/SS pin voltage. The lower of these two voltages is what the error amplifier controls the FB pin to. As the voltage on the EN/SS pin ramps up past approximately 1.4 V (800 mV offset voltage plus the 600 mV reference voltage), the 600-mV reference voltage becomes the dominant input and the converter has reached its final regulation voltage.

The capacitance required for a given soft-start ramp time for the output voltage is calculated in [Equation 1](#).

$$C_{SS} = \left( \frac{I_{SS}}{V_{FB}} \right) \times t_{SS}$$

where

- $C_{SS}$  is the required capacitance on the EN/SS pin (nF)
  - $I_{SS}$  is the soft-start source current (10  $\mu\text{A}$ )
  - $V_{FB}$  is the feedback reference voltage (0.6 V)
  - $t_{SS}$  is the desired soft-start ramp time (ms)
- (1)

### Oscillator

The oscillator frequency is internally fixed at 500 KHz if there is no resistor connected from COMP pin to GND. Optionally, a 40.2-k $\Omega$  resistor from the COMP pin to GND sets the frequency to 300 KHz. Alternatively, a 13.3-k $\Omega$  resistor from COMP pin GND sets the frequency to 1 MHz.

### Overcurrent Protection (OCP)

Programmable OCP level at ILIM is from 6 mV to 50 mV. With a scale factor of 2, the actual OC trip point across the low-side FET is in the range of 12 mV to 100 mV.

If the voltage drop across  $R_{OCSET}$  reaches 300 mV during calibration (No  $R_{OCSET}$  resistor included), it disables OC protection. Once disabled, there is no low-side or high-side current sensing.

OCP level for the high-side FET is fixed at 34 A (typical). The high-side OCP provides pulse-by-pulse current limiting.

OCP sensing for the low-side FET is a true inductor valley current detection, using sample and hold. [Equation 2](#) can be used to calculate  $R_{OCSET}$ .

$$R_{OCSET} = \left( I_{OUT(max)} - \left( \frac{I_{P-P}}{2} \right) \right) \times 95 + 500$$

where

- $I_{P-P}$  is the peak-to-peak inductor current (A)
  - $I_{OUT(max)}$  is the trip point for OCP (A)
  - $R_{OC(set)}$  is the resistor used for setting the OCP level ( $\Omega$ )
- (2)

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An overcurrent (OC) condition is detected by sensing voltage drop across the low-side FET and across the high-side FET. If the voltage drop across either FET exceeds OC threshold, a count increments one count. If no OC condition is detected on either FET, the fault counter decrements by one counter. If three OC pulses are summed, a fault condition is declared which cycles the soft-start function in a hiccup mode. Hiccup mode is defined as four dummy soft-start timeouts followed by a real one if overcurrent condition is encountered during normal operation; or five dummy soft-start timeouts followed by a real one if overcurrent condition occurs from the beginning during start. This cycle continues indefinitely until the fault condition is removed.

### Input Undervoltage Lockout (UVLO)

The TPS56121 has fixed input under-voltage lockout (UVLO). In order for the device to turn on, the following conditions must be met:

- the EN/SS pin voltage must be greater than  $V_{IH}$
- the input voltage must exceed UVLO on voltage  $V_{UVLO}$

The UVLO has a minimum of 500 mV hysteresis built-in.

### Pre-Bias Startup

The TPS56121 contains a unique circuit to prevent current from being pulled from the output during startup in the condition the output is pre-biased. There are no PWM pulses until the internal soft-start voltage rises above the error amplifier input (FB pin), if the output is pre-biased. Once the soft-start voltage exceeds the error amplifier input, the controller slowly initiates synchronous rectification by starting the synchronous rectifier with a narrow on time. It then increments the on-time on a cycle-by-cycle basis until it coincides with the time dictated by  $(1-D)$ , where D is the duty cycle of the converter.

This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage startup and ramp to regulation is smooth and controlled.

### Power Good

The TPS56121 provides an indication that output is good for the converter. This is an open drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- $V_{FB}$  is more than  $\pm 12.5\%$  from nominal
- soft-start is active
- a short circuit condition has been detected

---

#### NOTE

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built in resistor connected from drain to gate on the PGOOD pull down device makes the PGOOD pin look approximately like a diode to GND.

---

### Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 145°C, the PWM and the oscillator are turned off. Both high-side FET and low-side FET are kept off. When the junction cools to the required level (125°C typical), the PWM initiates soft start as during a normal power-up cycle.

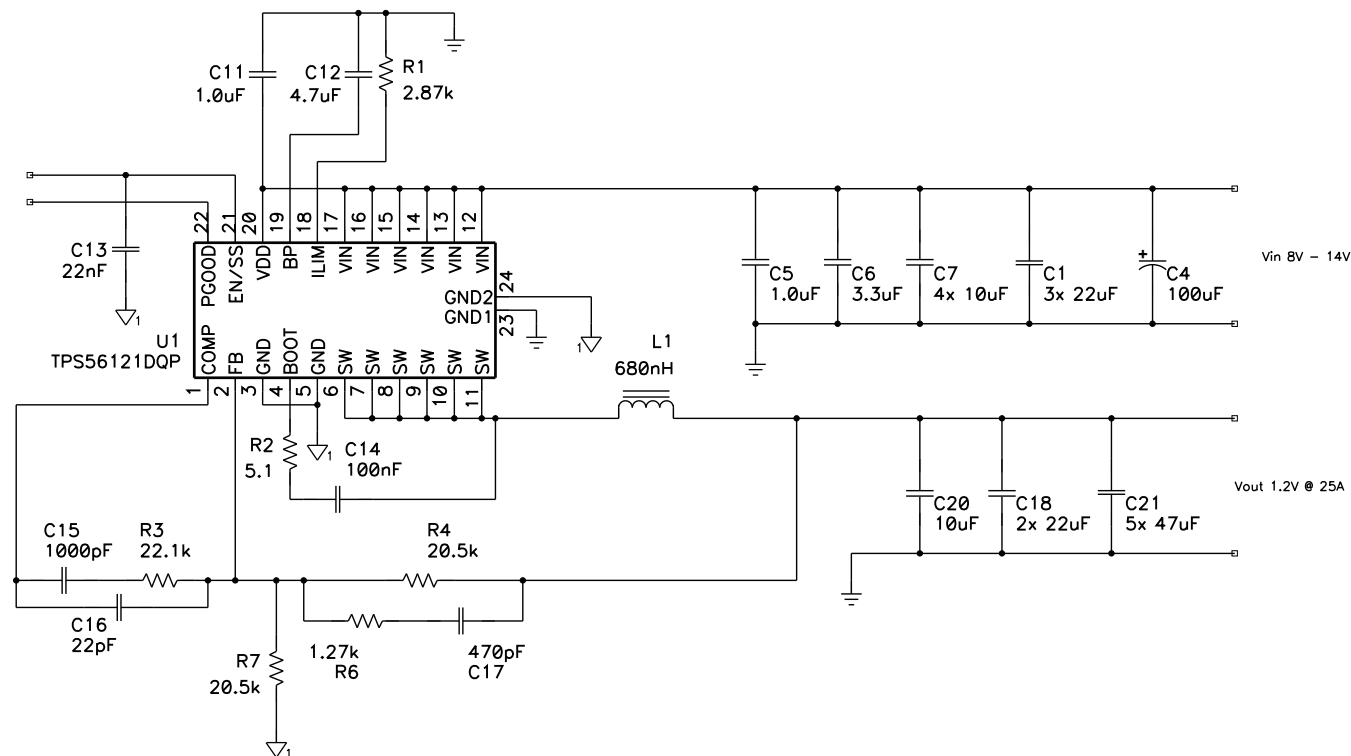
## DESIGN EXAMPLE

### Introduction

This design example describes a 15-A, 12-V to 1.2-V design using the TPS56121 high-current integrated buck converter. The system specifications are listed in [Table 1](#).

**Table 1. TPS56121 Design Example Parameters**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage	8.0		14	V
$V_{IN(ripple)}$	Input ripple			0.5	V
$V_{OUT}$	Output voltage				
	Line regulation		1.164	1.236	V
	Load regulation			0.5%	
$V_{RIPPLE}$	Output ripple			24	mV
$V_{OVER}$	Output overshoot		50		mV
$V_{UNDER}$	Output undershoot		50		mV
$I_{OUT}$	Output current				
	Soft-start time		1.5		ms
$t_{SS}$	Short-circuit current trip point	20			A
$I_{SCP}$	Efficiency		90		%
$\eta$	Switching frequency		500		kHz
$f_{SW}$	Size			0.6	ln <sup>2</sup>



**Figure 20. Design Example Schematic**

## Design Procedure

### Switching Frequency Selection

To achieve a balance between small size and high efficiency for this design, use switching frequency of 500 kHz.

### Inductor Selection (L1)

Synchronous buck power inductors are typically sized for between approximately 20% and 40% peak-to-peak ripple current ( $I_{RIPPLE}$ ).

Using this target ripple current, the required inductor size can be calculated as shown in Equation 3.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{14V - 1.2V}{0.3 \times 15A} \times \frac{1.2V}{14V} \times \frac{1}{500kHz} = 487nH \quad (3)$$

Selecting a standard 680-nH inductor value,  $I_{RIPPLE} = 7.3A$ .

The RMS current through the inductor is approximated in Equation 4.

$$I_{L(rms)} = \sqrt{\left(I_{L(avg)}\right)^2 + \left(\frac{1}{12} \times (I_{RIPPLE})^2\right)} = \sqrt{\left(I_{OUT}\right)^2 + \left(\frac{1}{12} \times (I_{RIPPLE})^2\right)} = \sqrt{(15)^2 + \left(\frac{1}{12} \times (3.2)^2\right)} = 15.03A \quad (4)$$

### Output Capacitor Selection (C18, C20, C23)

The selection of the output capacitor is typically driven by the output transient response. The selection of the output capacitor is typically driven by the output transient response.

- loop bandwidth delay
- inductor slew-rate delay
- transient slew-rate

For applications with  $V_{IN(min)} > 2 \times V_{OUT}$  the calculation is shown in Equation 5.

$$C_{OUT(min)} = \frac{I_{TRAN(max)}}{3\pi \times BW \times V_{OVER}} + \frac{\left(I_{TRAN(max)}\right)^2 \times L}{2 \times (V_{OUT}) \times V_{OVER}} - \frac{I_{TRAN(max)} \times t_{FALL}}{V_{OVER}} =$$

$$\frac{5}{3\pi \times 60kHz \times 50mV} + \frac{(5)^2 \times 680nH}{2 \times 1.2 \times 50mV} - \frac{5A \times 1\mu s}{50mV} = 177\mu F + 142\mu F - 50\mu F = 269\mu F \quad (5)$$

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated in Equation 6.

$$ESR_{MAX} = \frac{V_{RIPPLE(tot)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(tot)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} = \frac{24mV - \left(\frac{3.2A}{8 \times 269\mu F \times 500kHz}\right)}{3.2A} = 6.5m\Omega \quad (6)$$

In order to meet the low ESR and high capacitance requirements of this design, 5 47-μF, 1210, 2 22-μF, 1206, and 1 10-μF, 0805 ceramic capacitors are selected. The combination of multiple capacitor types and ceramic capacitors of different sizes provides a wider band to the filtering frequencies of the output capacitors.

### Inductor Peak Current Rating

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated by [Equation 7](#).

$$I_{\text{CHARGE}} = \frac{V_{\text{OUT}} \times C_{\text{OUT}}}{t_{\text{SS}}} = \frac{1.2\text{V} \times 275\mu\text{F}}{1.5\text{ms}} = 0.22\text{A} \quad (7)$$

$$I_{\text{L(peak)}} = I_{\text{OUT(max)}} + \left(\frac{1}{2} \times I_{\text{RIPPLE}}\right) + I_{\text{CHARGE}} = 15\text{A} + \left(\frac{1}{2} \times 3.2\text{A}\right) + 0.22\text{A} = 16.8\text{A} \quad (8)$$

**Table 2. Inductor Requirements Summary**

PARAMETER		VALUE	UNITS
L	Inductance	680	nH
$I_{\text{L(rms)}}$	RMS current (thermal rating)	15.03	A
$I_{\text{L(peak)}}$	Peak current (saturation rating)	16.8	A

PG0871.681NL, 680-nH, 2.3-mΩ, 24-A inductor is selected with a 24-A saturation current and 19-A<sub>RMS</sub> thermal rating. A physically larger inductor with a lower DCR could be selected for higher efficiency, but this small inductor better meets the 0.6 maximum PCB area requirement.

### Bootstrap Capacitor (C14)

The bootstrap capacitor maintains power to the high-side driver during the high-side switch ON time. Per the requirements of the integrated MOSFET, the value of C<sub>BOOT</sub> is 100 nF with a minimum 10-V rating.

### Bootstrap Resistor (R2)

The bootstrap resistor slows the rising edge of the SW voltage to reduce ringing and improve EMI. Per the datasheet recommendation a 5.1-Ω resistor is selected.

### VDD Bypass Capacitor (C11)

Per the TPS56221 recommended pin terminations, VDD is bypassed to GND with a 1.0-μF capacitor.

### BP5 Bypass Capacitor (C12)

Per the TPS56221 recommended pin terminations, VDD is bypassed to GND with at least 1.0-μF capacitor. For additional filtering and noise immunity, a 4.7-μF capacitor is selected.

### Soft-Start Capacitor (C13)

The soft-start capacitor provides a constant ramp voltage to the error amplifier to provide controlled, smooth start-up. The soft-start capacitor is sized using [Equation 9](#).

$$C_{\text{SS}} = \frac{I_{\text{SS}}}{V_{\text{FB}}} \times t_{\text{SS}} = \frac{10\mu\text{A}}{0.6\text{V}} \times 1.5\text{ms} = 25\text{nF} \approx 22\text{nF} \quad (9)$$

### Current Limit (R1)

The TPS56221 uses the negative drop across the internal low-side FET at the end of the OFF-time to measure the valley of the inductor current. Allowing for a minimum of 30% over maximum load, the programming resistor is selected using [Equation 10](#).

$$R_{\text{OCSET}} = 95 \times \left( 1.3 \times I_{\text{OUT(max)}} - \left( \frac{I_{\text{RIPPLE}}}{2} \right) \right) + 500\Omega = 95 \times \left( 1.3 \times 15\text{A} - \left( \frac{3.2\text{A}}{2} \right) \right) + 500\Omega = 2.20\text{k}\Omega \approx 2.87\text{k}\Omega \quad (10)$$

# TPS56121

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## Feedback Divider (R4, R7)

The TPS56121 converter uses a full operational amplifier with an internally fixed 0.600-V reference. R4 is selected between 10 kΩ and 50 kΩ for a balance of feedback current and noise immunity. With R4 set to 20.5 kΩ, The output voltage is programmed with a resistor divider given by Equation 11.

$$R_{BIAS} = \frac{V_{FB} \times R_{FB}}{(V_{OUT} - V_{FB})} = \frac{0.600 \text{ V} \times 20.5 \text{ k}\Omega}{1.2 \text{ V} - 0.600 \text{ V}} = 20.5 \text{ k}\Omega \approx 20.5 \text{ k}\Omega \quad (11)$$

## Compensation (C15, C16, C17, R3, R6)

Using the *TPS40k Loop Stability Tool* for 60 kHz of bandwidth and 60 degrees of phase margin with an R4 value of 20.5 kΩ, the following values are obtained.

- C17 = C\_1 = 470 pF
- C15 = C\_2 = 1000 pF
- C16 = C\_3 = 22 pF
- R6 = R\_2 = 1.27 kΩ
- R3 = R\_3 = 22.1 kΩ

## DESIGN EXAMPLE PERFORMANCE CHARACTERISTICS

Output voltage 12 V to 1.2V at 0-A to 15-A input current.

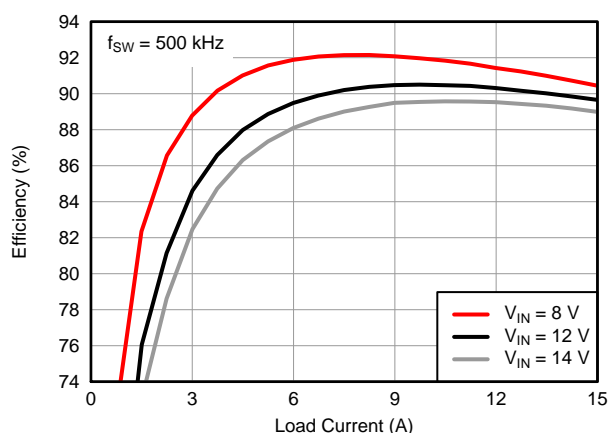


Figure 21. Efficiency vs Load Current

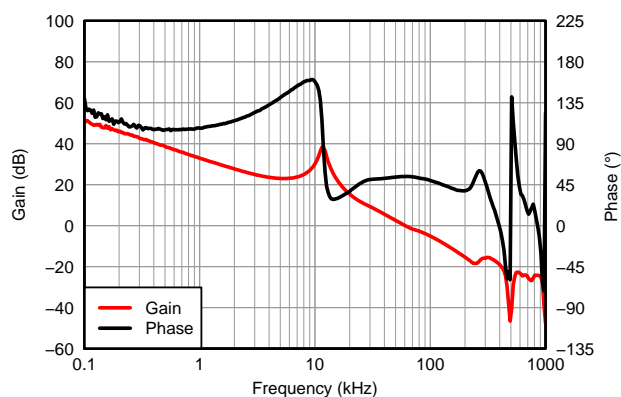


Figure 22. Loop Response 60 kHz Bandwidth, 54° Phase Margin



Figure 23. Output Ripple 20 mV/div, 1.0 μs/div, 20 MHz Bandwidth, AC Coupled



**Table 3. List of Materials for TPS56221 Design Example**

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MANUFACTURER
C1	3	22 $\mu$ F	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
C4	1	100 $\mu$ F	Capacitor, Aluminum, 16VDC, $\pm$ 20%	D8	EEEF1C101AP	Panasonic
C5	1	1.0 $\mu$ F	Capacitor, Ceramic, 25V, X7R, 20%	0805	Std	Std
C6	1	3.3 $\mu$ F	Capacitor, Ceramic, 25V, X7R, 20%	0805	Std	Std
C7	4	10 $\mu$ F	Capacitor, Ceramic, 25V, X7R, 20%	1206	Std	Std
C11	1	1.0 $\mu$ F	Capacitor, Ceramic, 25V, X5R, 20%	0805	Std	Std
C12	1	4.7 $\mu$ F	Capacitor, Ceramic, 10V, X5R, 20%	0805	Std	Std
C13	1	22 $\mu$ F	Capacitor, Ceramic, 16V, X7R, 20%	0402	Std	Std
C14	1	100 $\mu$ F	Capacitor, Ceramic, 16V, X7R, 20%	0402	Std	Std
C15	1	1000 pF	Capacitor, Ceramic, 25V, X7R, 10%	0402	Std	Std
C16	1	22 pF	Capacitor, Ceramic, 25V, C0G, 10%	0402	Std	Std
C17	1	470 pF	Capacitor, Ceramic, 25V, C0G, 10%	0402	Std	Std
C18	2	22 $\mu$ F	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	Std	Std
C20	1	10 $\mu$ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	Std	Std
C21	5	47 $\mu$ F	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	Std	Vishay
L1	1	320 nH	IND, SMT Power $\pm$ 15%	7.6 x 7.4 mm	PG0871.681NL	Pulse
R1	1	2.87 k $\Omega$	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R2	1	5.1 $\Omega$	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R3	1	22.1 k $\Omega$	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R4	1	20.5 k $\Omega$	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R6	1	1.27 k $\Omega$	Resistor, Chip, 1/16W, 1%	0402	Std	Std
R7	1	20.5 k $\Omega$	Resistor, Chip, 1/16W, 1%	0402	Std	Std
U1	1	TPS56121 DQP	15 A, 600 kHz, synchronous buck converter	QFN-22 6 x 5 mm	TPS56121DQP	TI

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS56121DQPR	ACTIVE	SON	DQP	22	2500	Pb-Free (RoHS Exempt)	CU SN	Level-2-260C-1 YEAR	
TPS56121DQPT	ACTIVE	SON	DQP	22	250	TBD	Call TI	Call TI	

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**ACTIVE:** Product device recommended for new designs.

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**OBSOLETE:** TI has discontinued the production of the device.

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**TBD:** The Pb-Free/Green conversion plan has not been defined.

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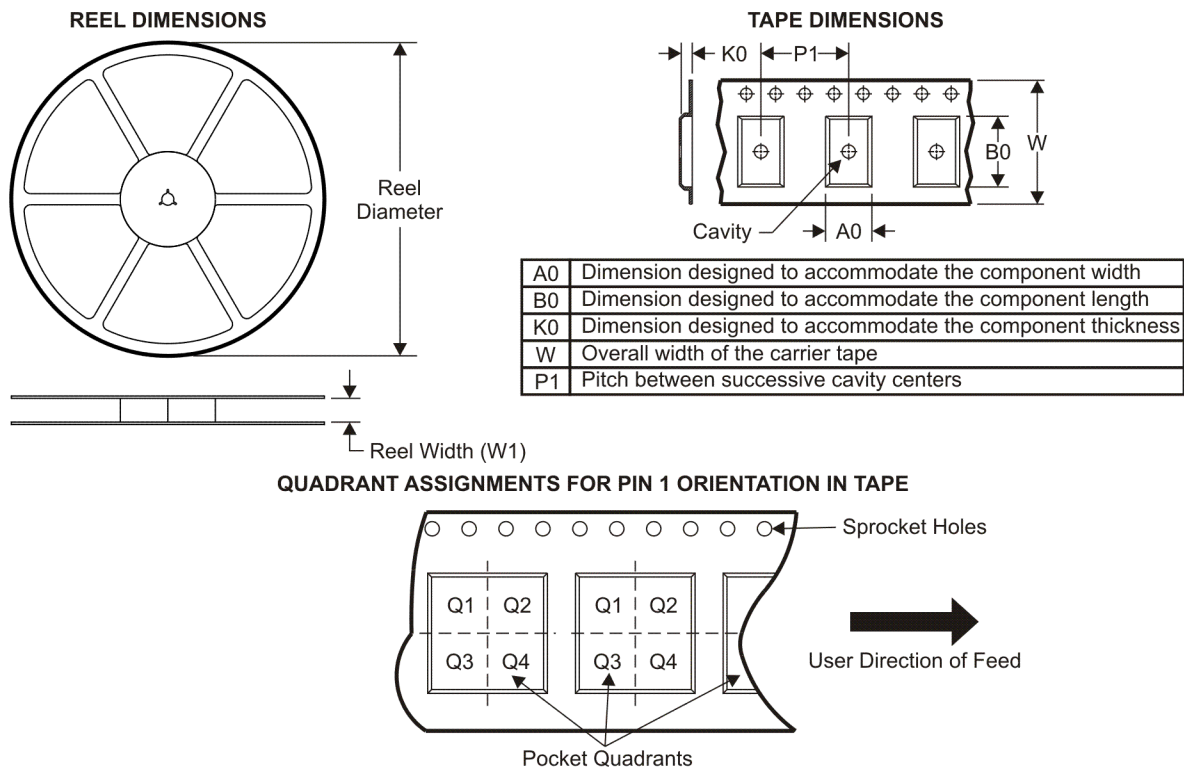
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56121DQPR	SON	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

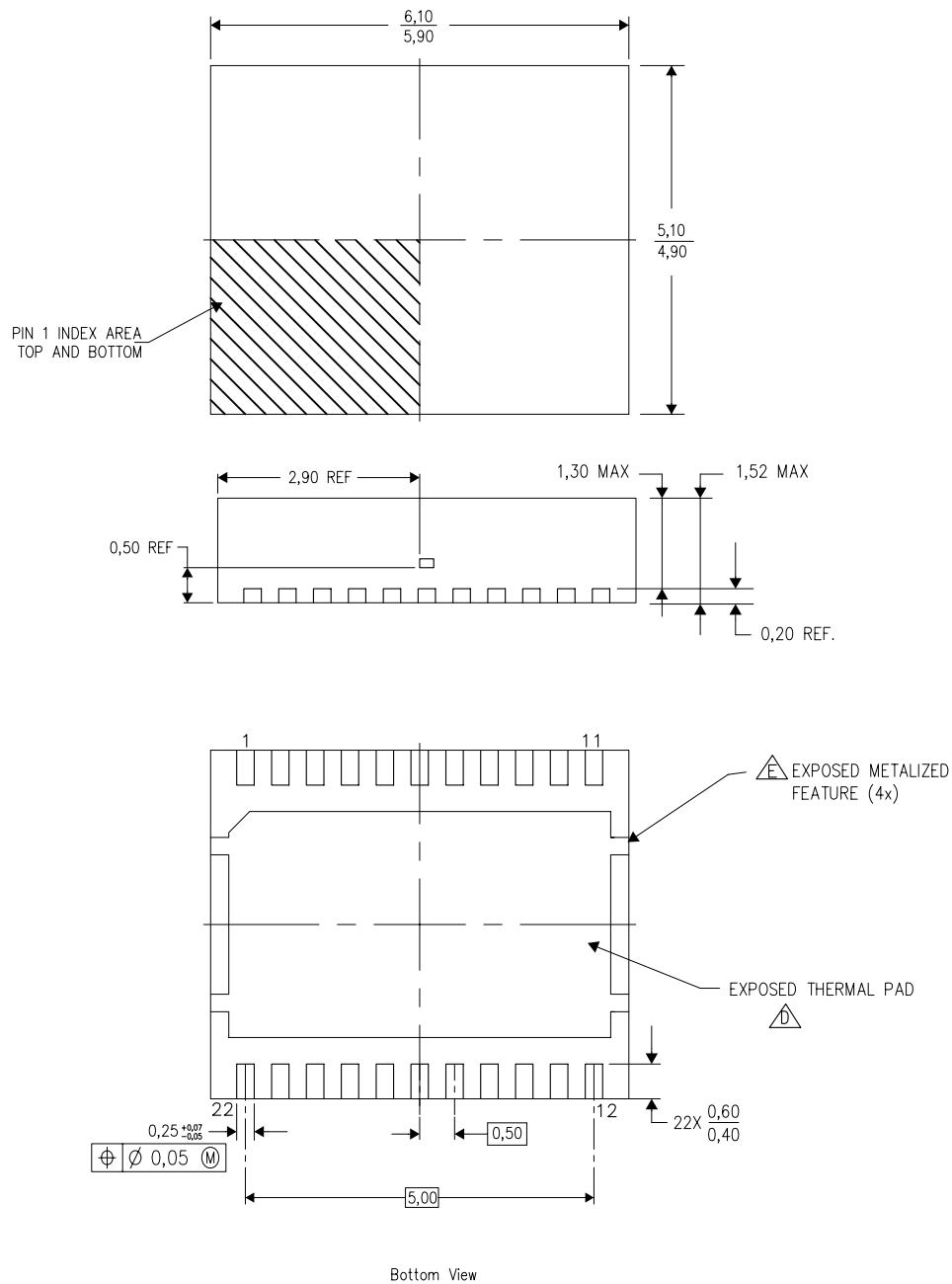


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56121DQPR	SON	DQP	22	2500	346.0	346.0	29.0

DQP (R-PSON-N22)

PLASTIC SMALL OUTLINE NO-LEAD



4210472/C 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
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