# Low Cost, High Performance, CMOS Rail-to-Rail Output Operational Amplifier

# AD8692

## FEATURES

**Offset voltage: 400 μV typ**
**Low offset voltage drift: 6 μV/°C maximum**
**Very low input bias currents: 1 pA maximum**
**Low noise: 8 nV/√Hz**
**Low distortion: 0.0006%**
**Wide bandwidth: 10 MHz**
**Unity gain stable**
**Single-supply operation: 2.7 V to 6 V**

## APPLICATIONS

**Photodiode amplification**
**Battery-powered instrumentation**
**Medical instruments**
**Multipole filters**
**Sensors**
**Portable audio devices**

## PIN CONFIGURATIONS

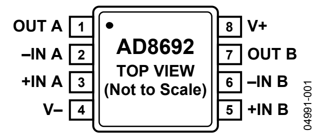


*Figure 1. 8-Lead MSOP Pin Configuration*

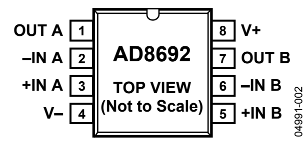


*Figure 2. 8-Lead SOIC Pin Configuration*

## GENERAL DESCRIPTION

The AD8692 is a low cost, dual rail-to-rail output, single-supply amplifier featuring low offset voltage, low input voltage and current noise, and wide signal bandwidth. The combination of low offset, low noise, very low input bias currents, and high speed makes this amplifier useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion.

Applications for this amplifier include PA controls, laser diode control loops, portable and loop-powered instrumentation, audio amplification for portable devices, and ASIC input and output amplifiers.

The AD8692 is specified over the extended industrial temperature range of −40°C to +125°C. The AD8692 is available in the micro-SOIC and 8-lead narrow SOIC surface-mount packages.

**Rev. 0**


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## REVISION HISTORY

**10/04—Revision 0: Initial Version**

# ELECTRICAL CHARACTERISTICS

$V_S$ = 2.7 V, $V_{CM}$ = $V_S$/2, $T_A$ = 25°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = −0.3 V to +1.6 V | | 0.4 | 2.0 | mV |
| | | $V_{CM}$ = −0.1 V to +1.6 V; −40°C < $T_A$ < +125°C | | | 3.0 | mV |
| Input Bias Current | $I_B$ | | | 0.2 | 1 | pA |
| | | −40°C < $T_A$ < +85°C | | | 50 | pA |
| | | −40°C < $T_A$ < +125°C | | | 260 | pA |
| Input Offset Current | $I_{OS}$ | | | 0.1 | 0.5 | pA |
| | | −40°C < $T_A$ < +85°C | | | 20 | pA |
| | | −40°C < $T_A$ < +125°C | | | 75 | pA |
| Input Voltage Range | | | −0.3 | | +1.6 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = −0.3 V to +1.6 V | 70 | 90 | | dB |
| | | $V_{CM}$ = −0.1 V to +1.6 V; −40°C < $T_A$ < +125°C | 65 | 85 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = 0.5 V to 2.2 V | 90 | 250 | | V/mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 1.3 | 6.0 | μV/°C |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_L$ = 1 mA | 2.64 | 2.66 | | V |
| | | −40°C < $T_A$ < +125°C | 2.6 | | | V |
| Output Voltage Low | $V_{OL}$ | $I_L$ = 1 mA | | 25 | 40 | mV |
| | | −40°C < $T_A$ < +125°C | | | 50 | mV |
| Short-Circuit Current | $I_{SC}$ | | | ±20 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | f = 1 MHz, $A_V$ = 1 | | 12 | | Ω |
| POWER SUPPLY | | | | | | |
| Power-Supply Rejection Ratio | PSRR | $V_S$ = 2.7 V to 5.5 V | 80 | 95 | | dB |
| | | −40°C < $T_A$ < +125°C | 75 | 95 | | dB |
| Supply Current/Amplifier | $I_{SY}$ | $V_O$ = 0 V | | 0.85 | 0.95 | mA |
| | | −40°C < $T_A$ < +125°C | | | 1.2 | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 5 | | V/μs |
| Settling Time | $t_S$ | To 0.01% | | 1 | | μs |
| Gain Bandwidth Product | GBP | | | 10 | | MHz |
| Phase Margin | Øo | | | 60 | | Degrees |
| Total Harmonic Distortion + Noise | THD+N | G = 1, $R_L$ = 600 Ω, f = 1 kHz, $V_O$ = 250 mV p-p | | 0.003 | | % |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_{n\ p\text{-}p}$ | f = 0.1 Hz to 10 Hz | | 1.6 | 3.0 | μV p-p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 8 | 12 | nV/√Hz |
| | $e_n$ | f = 10 kHz | | 6.5 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 1 kHz | | 0.05 | | pA/√Hz |

$V_S$ = 5.0 V, $V_{CM}$ = $V_S$/2, $T_A$ = 5°C, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Conditions | A Grade Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = −0.3 V to +3.9 V | | 0.4 | 2.0 | mV |
| | | $V_{CM}$ = −0.1 V to +3.9 V; −40°C < $T_A$ < +125°C | | | 3.0 | mV |
| Input Bias Current | $I_B$ | | | 0.2 | 1 | pA |
| | | −40°C < $T_A$ < +85°C | | | 50 | pA |
| | | −40°C < $T_A$ < +125°C | | | 260 | pA |
| Input Offset Current | $I_{OS}$ | | | 0.1 | 0.5 | pA |
| | | −40°C < $T_A$ < +85°C | | | 20 | pA |
| | | −40°C < $T_A$ < +125°C | | | 75 | pA |
| Input Voltage Range | | | −0.3 | | +3.9 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = −0.3 V to +3.9 V | 75 | 95 | | dB |
| | | $V_{CM}$ = −0.1 V to +3.9 V; −40°C < $T_A$ < +125°C | 70 | 95 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $V_O$ = 0.5 V to 4.5 V, $R_L$ = 2 kΩ, $V_{CM}$ = 0 V | 250 | 2,000 | | V/mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 1.3 | 6 | µV/°C |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_L$ = 1 mA | 4.96 | 4.98 | | V |
| | | $I_L$ = 10 mA | 4.7 | 4.78 | | V |
| | | −40°C to +125°C | 4.6 | | | V |
| Voltage Low | $V_{OL}$ | $I_L$ = 1 mA | | 16.5 | 40 | mV |
| | | $I_L$ = 10 mA | | 165 | 210 | mV |
| | | −40°C to +125°C | | | 290 | mV |
| Short-Circuit Current | $I_{SC}$ | | | ±80 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | f = 1 MHz, $A_V$ = 1 | | 10 | | Ω |
| POWER SUPPLY | | | | | | |
| Power-Supply Rejection Ratio | PSRR | $V_S$ = 2.7 V to 5.5 V | 80 | 95 | | dB |
| | | −40°C < $T_A$ < +125°C | 75 | 95 | | dB |
| Supply Current/Amplifier | $I_{SY}$ | $V_O$ = 0 V | | 0.95 | 1.05 | mA |
| | | −40°C < $T_A$ < +125°C | | | 1.3 | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 5 | | V/µs |
| Settling Time | $t_S$ | To 0.01% | | 1 | | µs |
| Full Power Bandwidth | $BW_P$ | <1% distortion | | 360 | | kHz |
| Gain Bandwidth Product | GBP | | | 10 | | MHz |
| Phase Margin | Øo | | | 65 | | Degrees |
| Total Harmonic Distortion + Noise | THD+N | G = 1, $R_L$ = 600 Ω, f = 1 kHz, $V_O$ = 1 V p-p | | 0.0006 | | % |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_{n\,p\text{-}p}$ | f = 0.1 Hz to 10 Hz | | 1.6 | 3.0 | µV p-p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 8 | 12 | nV/√Hz |
| | $e_n$ | f = 10 kHz | | 6.5 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 1 kHz | | 0.05 | | pA/√Hz |

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameters | Ratings |
|---|---|
| Supply Voltage | 6 V |
| Input Voltage | $V_{SS}$ – 0.3 V to $V_{DD}$ + 0.3 V |
| Differential Input Voltage | ±6 V |
| Output Short-Circuit Duration to Gnd[1] | Observe derating curves |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Junction Temperature Range | −65°C to +150°C |
| Lead Temperature Range (Soldering, 60 s) | 300°C |

[1] $\theta_{JA}$ is specified for the worst-case conditions, that is, the device soldered in the circuit board for surface-mount packages.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

**Table 4.**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-Lead MSOP (RM) | 210 | 45 | °C/W |
| 8-Lead SOIC (R) | 158 | 43 | °C/W |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_S$ = +5 V or ±2.5 V.

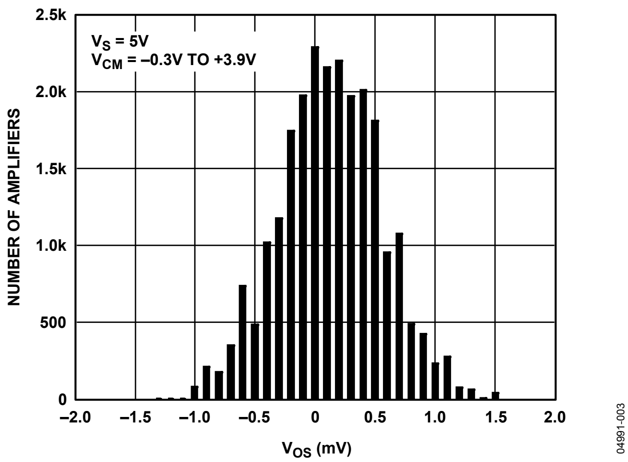


Figure 3. Input Offset Voltage Distribution

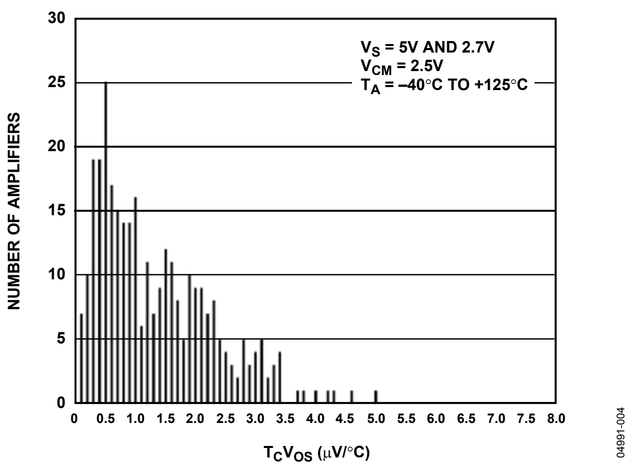


Figure 4. Input Offset Voltage Drift Distribution

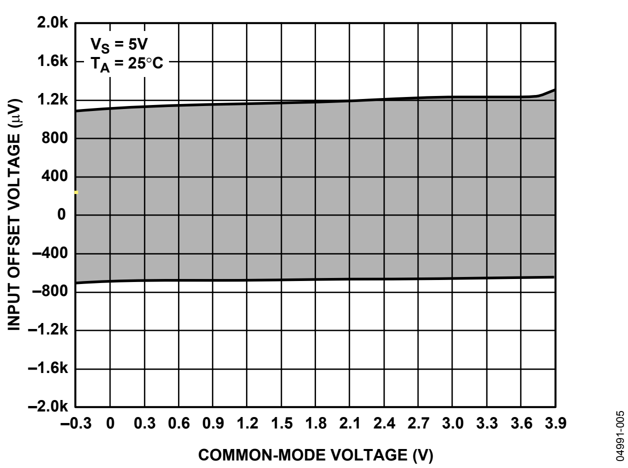


Figure 5. Input Offset Voltage vs. Common-Mode Voltage

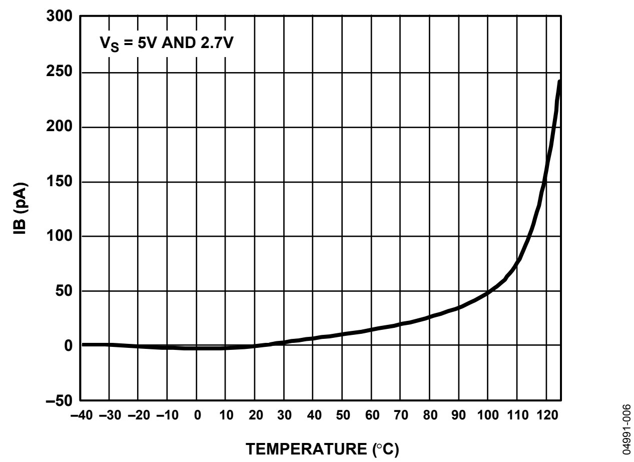


Figure 6. Input Bias Current vs. Temperature

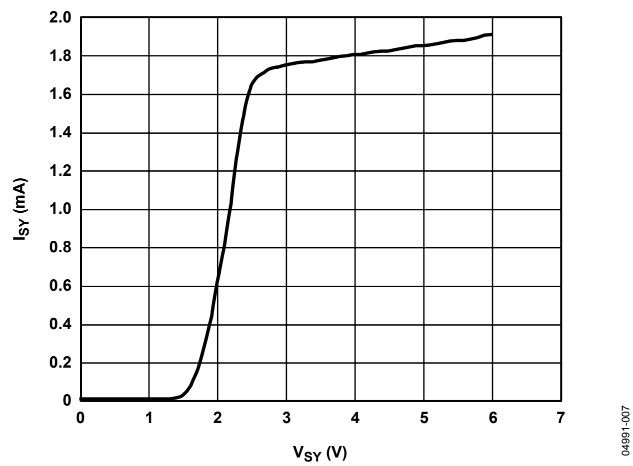


Figure 7. Supply Current vs. Supply Voltage

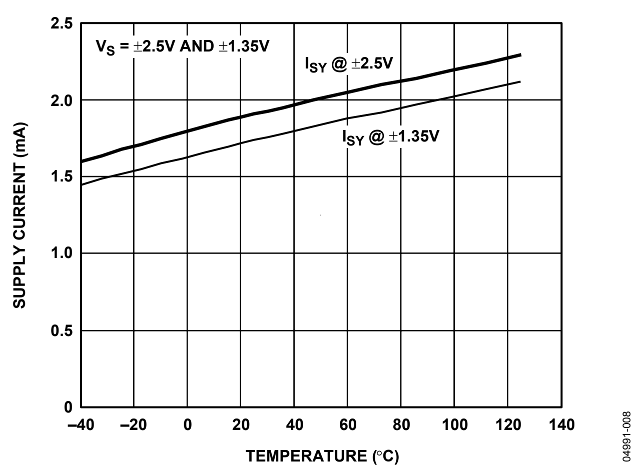


Figure 8. Supply Current vs. Temperature

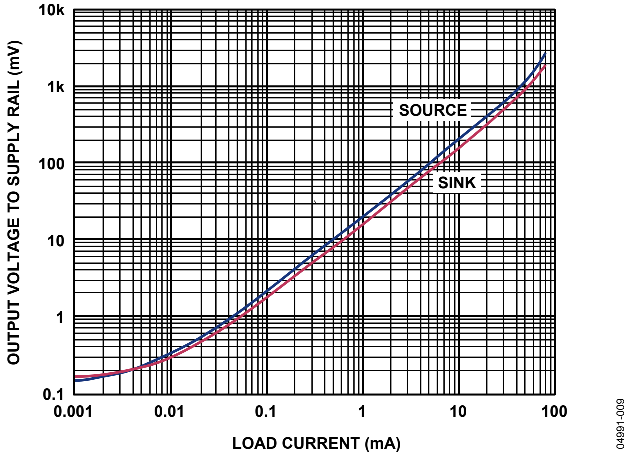


Figure 9. Output Voltage to Supply Rail vs. Load Current

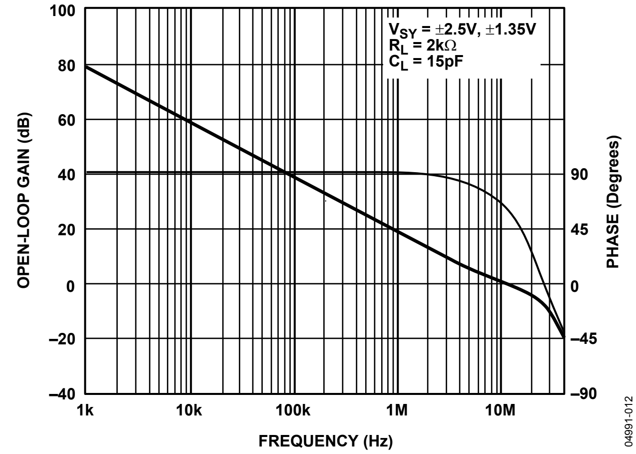


Figure 12. Open-Loop Gain and Phase vs. Frequency

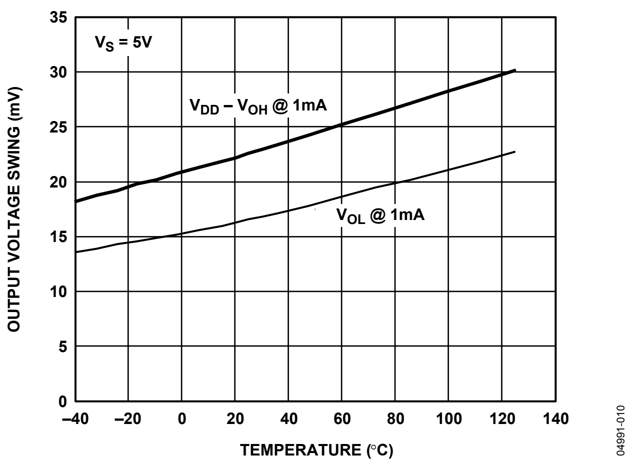


Figure 10. Output Voltage Swing vs. Temperature (IL = 1 mA)

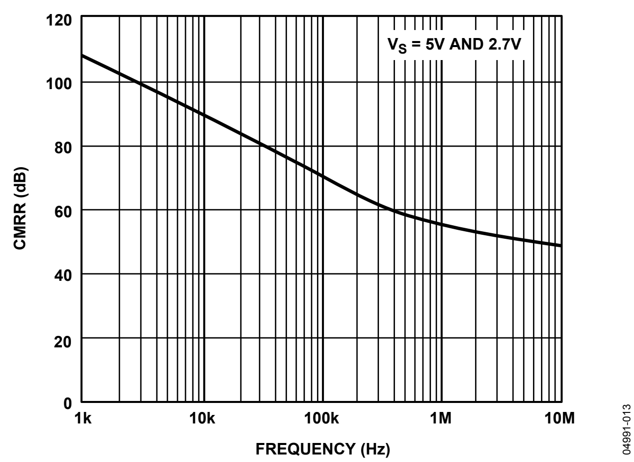


Figure 13. CMRR vs. Frequency

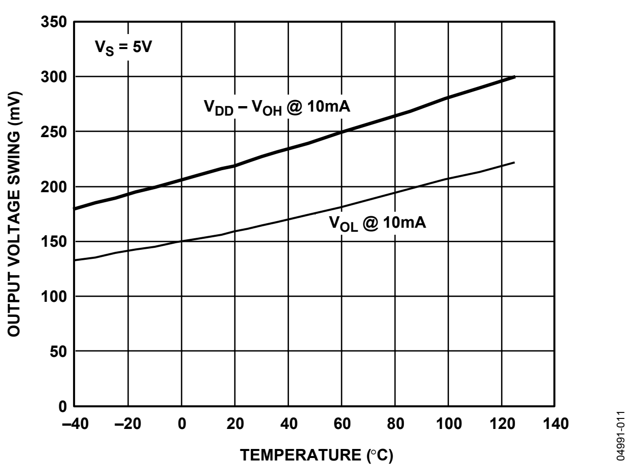


Figure 11. Output Voltage Swing vs. Temperature (IL = 10 mA)

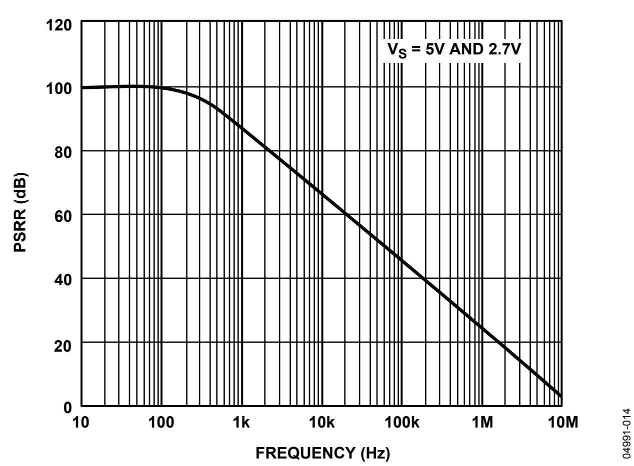


Figure 14. PSRR vs. Frequency

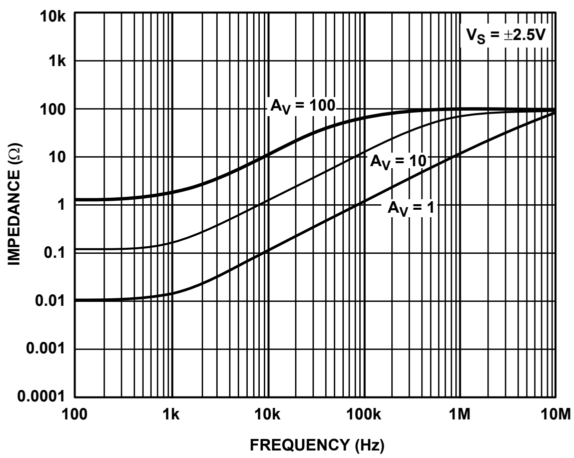


Figure 15. Closed-Loop Output Impedance vs. Frequency

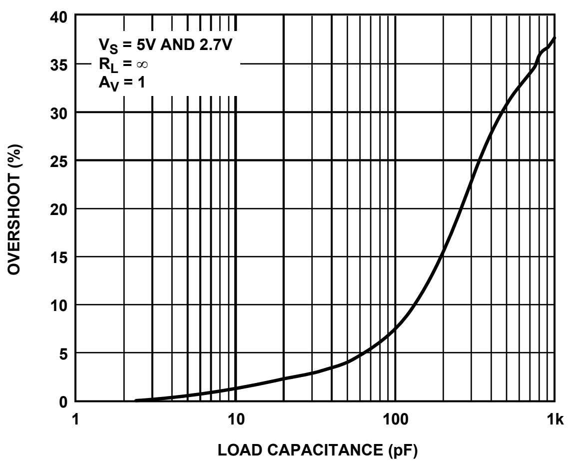


Figure 16. Small Signal Overshoot vs. Load Capacitance

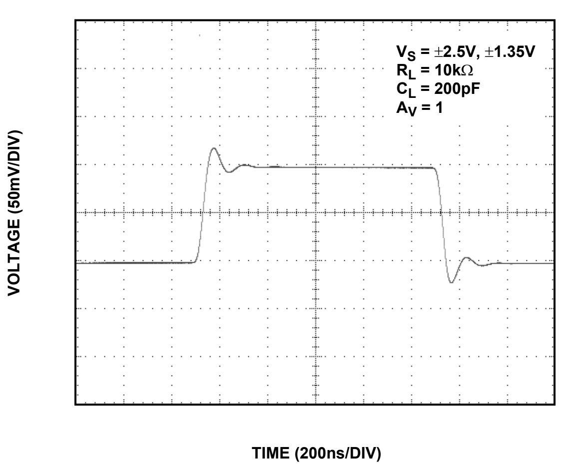


Figure 17. Small Signal Transient Response

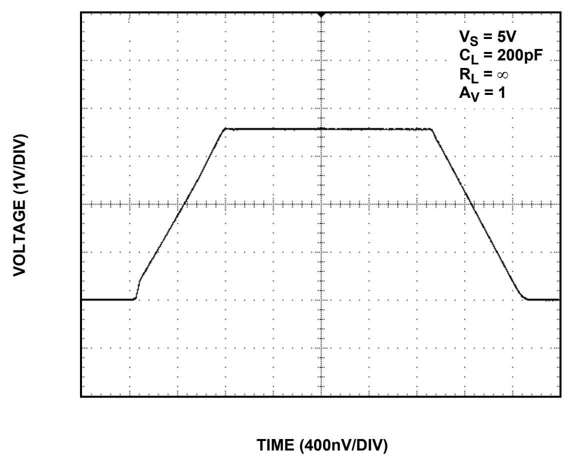


Figure 18. Large Signal Transient Response

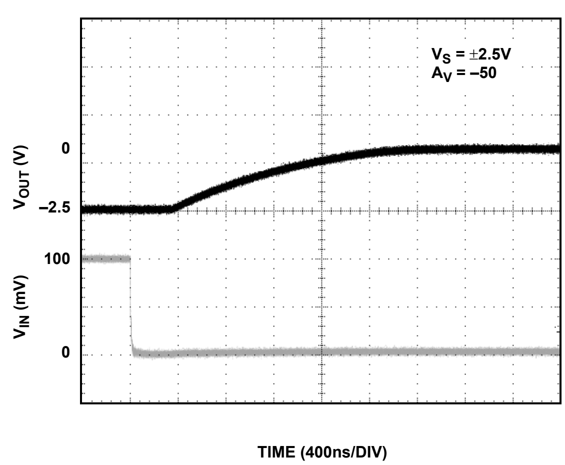


Figure 19. Positive Overload Recovery

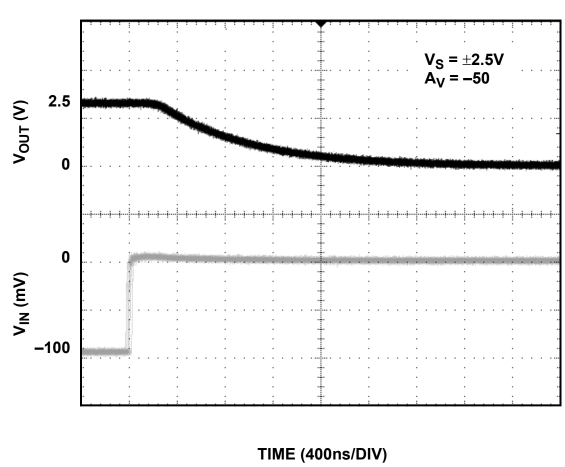


Figure 20. Negative Overload Recovery

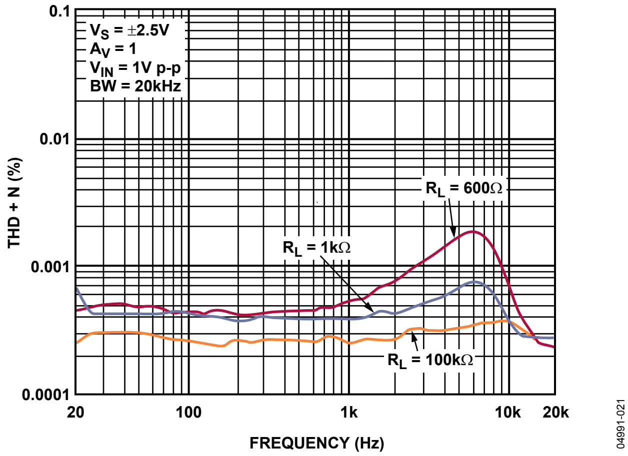


Figure 21. THD + N vs. Frequency

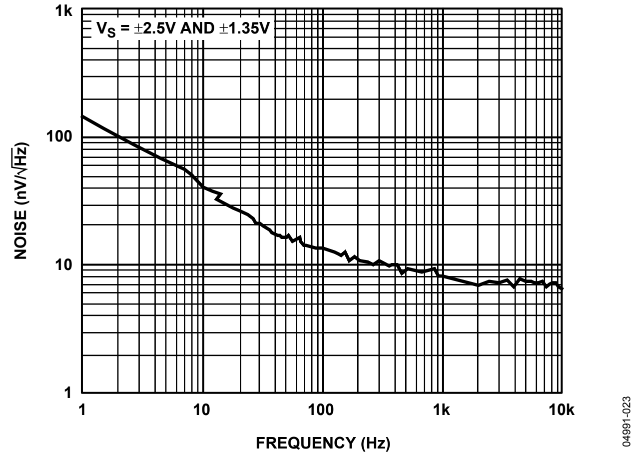


Figure 23. Voltage Noise Density

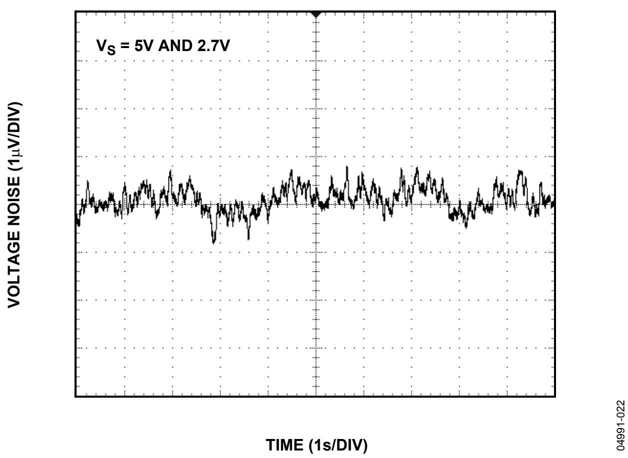


Figure 22. 0.1 Hz to 10 Hz Input Voltage Noise

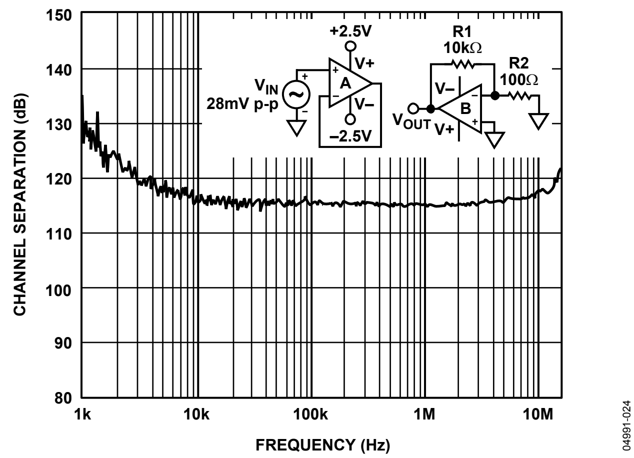


Figure 24. Channel Separation

$V_S$ = +2.7 V or ±1.35 V.

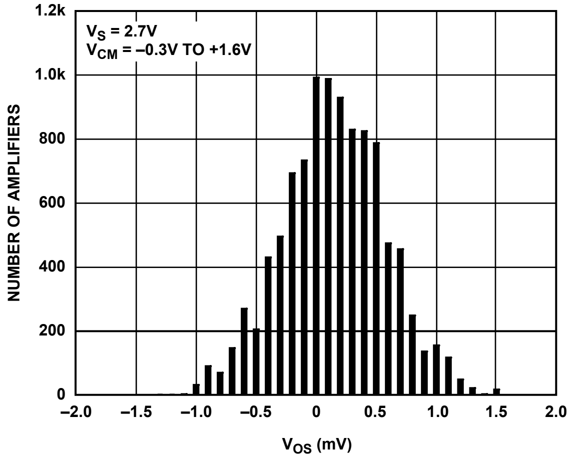


*Figure 25. Input Offset Voltage Distribution*

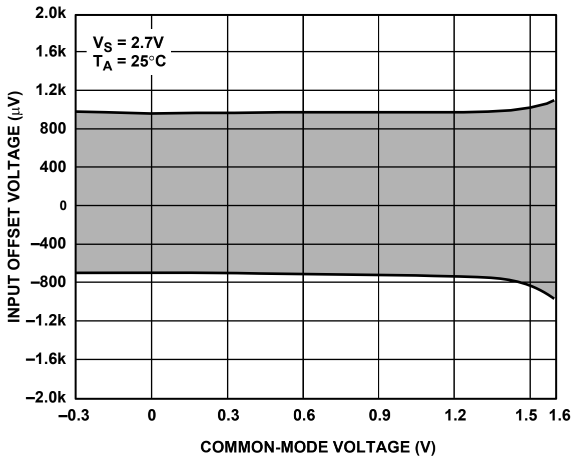


*Figure 26. Input Offset Voltage vs. Common-Mode Voltage*

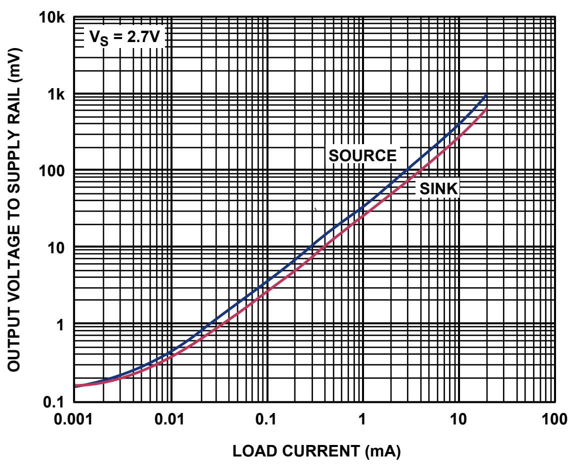


*Figure 27. Output Voltage to Supply Rail vs. Load Current*

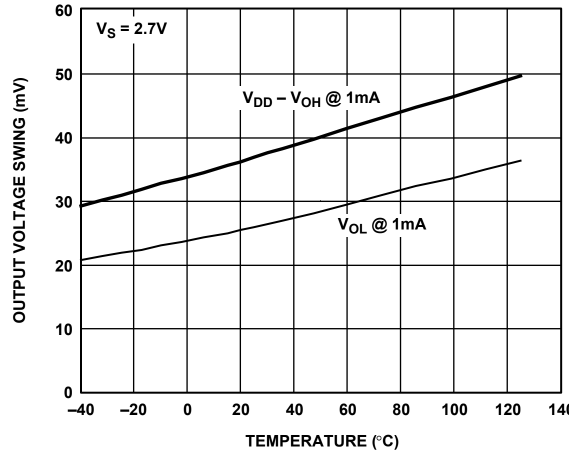


*Figure 28. Output Voltage Swing vs. Temperature*

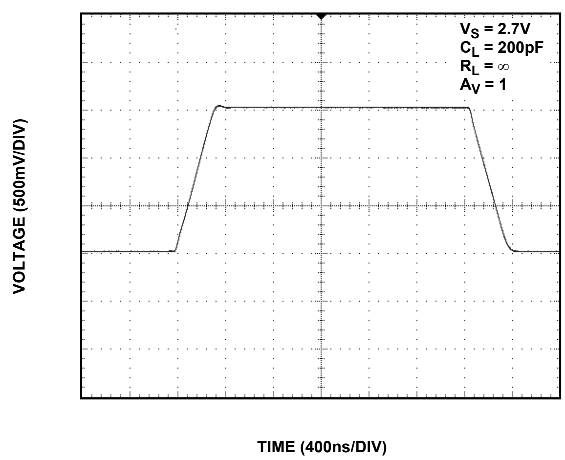


*Figure 29. Large Signal Transient Response*

# OUTLINE DIMENSIONS

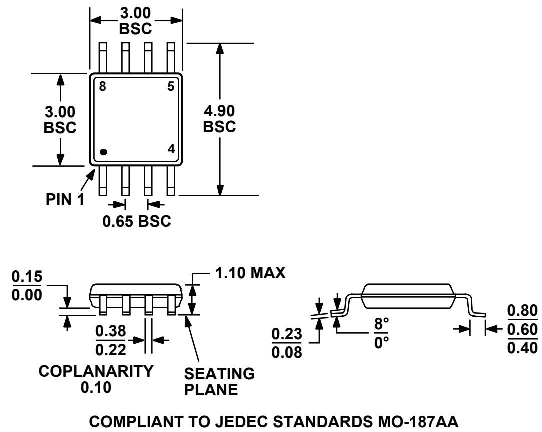


*Figure 30. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*

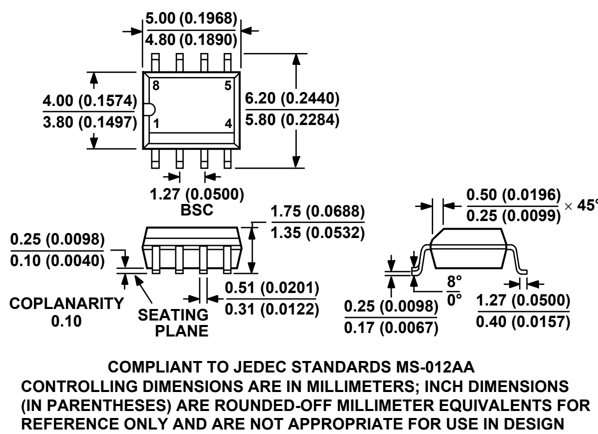


*Figure 31. 8-Lead Standard Small Outline Package [SOIC]*
*(R-8)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| AD8692ARMZ-R2[1] | −40°C to +125°C | 8-Lead MSOP | RM-8 | APA |
| AD8692ARMZ-REEL[1] | −40°C to +125°C | 8-Lead MSOP | RM-8 | APA |
| AD8692ARZ[1] | −40°C to +125°C | 8-Lead SOIC | R-8 | |
| AD8692ARZ-REEL[1] | −40°C to +125°C | 8-Lead SOIC | R-8 | |
| AD8692ARZ-REEL7[1] | −40°C to +125°C | 8-Lead SOIC | R-8 | |

[1] Z = Pb-free part.

# NOTES


D04991–0–10/04(0)

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