

2-Mbit (128K x 16) Static RAM

Features

- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62137CV30**
- **Ultra-low standby power**
 - Typical standby current: 1 μ A
 - Maximum standby current: 7 μ A
- **Ultra-low active power**
 - Typical active current: 2 mA @ f = 1 MHz
- **Easy memory expansion with $\overline{\text{CE}}$, and $\overline{\text{OE}}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Byte power-down feature**
- **Offered in Pb-free 48-ball VFBGA and 44-pin TSOPII package**

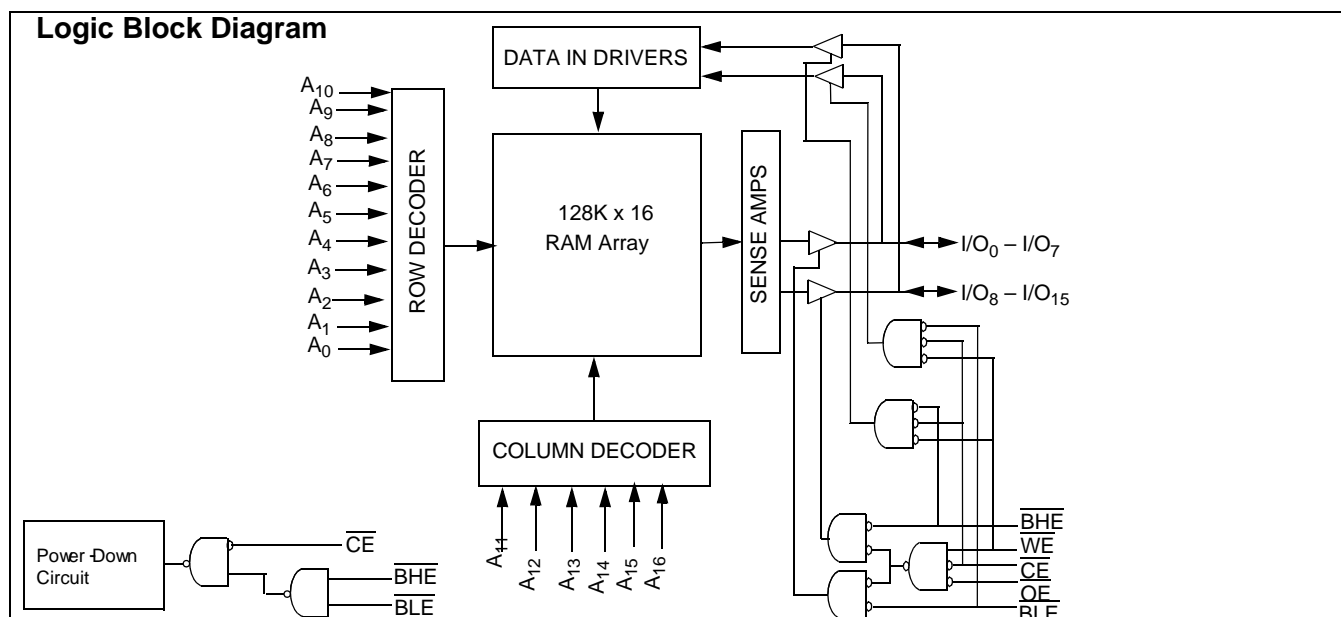
Functional Description^[1]

The CY62137EV30 is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{\text{CE}}$ HIGH or both BLE and BHE are HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}$ HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

Writing to the device is accomplished by asserting Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by asserting Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62137EV30 is available in 48-ball VFBGA and 44-pin TSOPII packages.

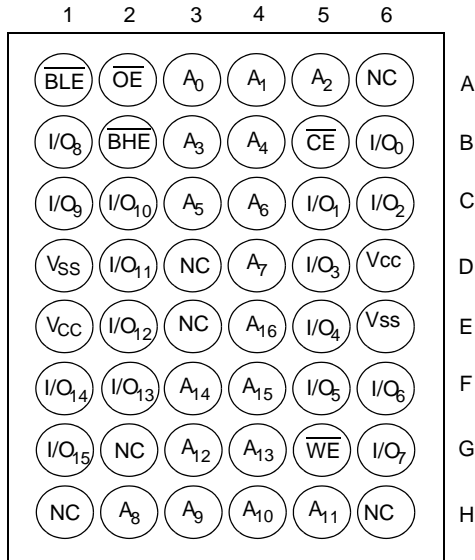


Note:

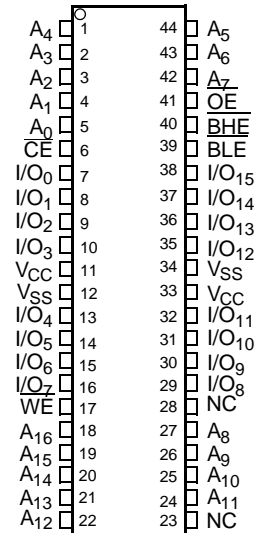
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configurations^[2, 3]

VFBGA (Top View)



44 TSOP II (Top View)



Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
	f = 1MHz		f = f _{max}							
	Min.	Typ. ^[7]	Max.		Typ. ^[7]	Max.	Typ. ^[7]	Max.	Typ. ^[7]	Max.
CY62137EV30-45LL	2.2V	3.0V	3.6V	45 ns	2	2.5	15	20	1	7

Note:

- NC pins are not connected on the die.
- Pins D3, H1, G2, and H6 in the BGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb, respectively.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to + 150°C

Ambient Temperature with
Power Applied -55°C to + 125°C

Supply Voltage to Ground
Potential -0.3V to 3.9V ($V_{CC(MAX)} + 0.3V$)

DC Voltage Applied to Outputs
in High-Z State^[4, 5] -0.3V to 3.9V ($V_{CC MAX} + 0.3V$)

DC Input Voltage^[4, 5] -0.3V to 3.9V ($V_{CC MAX} + 0.3V$)

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Device	Range	Ambient Temperature	$V_{CC}^{[6]}$
CY62137EV30-45LL	Industrial	-40°C to +85°C	2.2V to 3.6V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min.	Typ. ^[7]	Max.	
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$	$V_{CC} = 2.20V$	2.0			V
		$I_{OH} = -1.0 \text{ mA}$	$V_{CC} = 2.70V$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$	$V_{CC} = 2.20V$			0.4	V
		$I_{OL} = 2.1 \text{ mA}$	$V_{CC} = 2.70V$			0.4	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 2.2V \text{ to } 2.7V$		1.8		$V_{CC} + 0.3$	V
		$V_{CC} = 2.7V \text{ to } 3.6V$		2.2		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage	$V_{CC} = 2.2V \text{ to } 2.7V$		-0.3		0.6	V
		$V_{CC} = 2.7V \text{ to } 3.6V$		-0.3		0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled		-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$		15	20	mA
		$f = 1 \text{ MHz}$	$I_{OUT} = 0 \text{ mA}$ CMOS levels		2.0	2.5	
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$ $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE and WE), $V_{CC} = 3.60V$			1	7	μA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 3.60V$			1	7	μA

Notes:

4. $V_{IL(min.)} = -2.0V$ for pulse durations less than 20 ns.

5. $V_{IH(max)} = V_{CC} + 0.75V$ for pulse durations less than 20ns.

6. Full Device AC operation assumes a 100 μs ramp time from 0 to $V_{CC(min)}$ and 200 μs wait time after V_{CC} stabilization.

7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25^\circ C$.

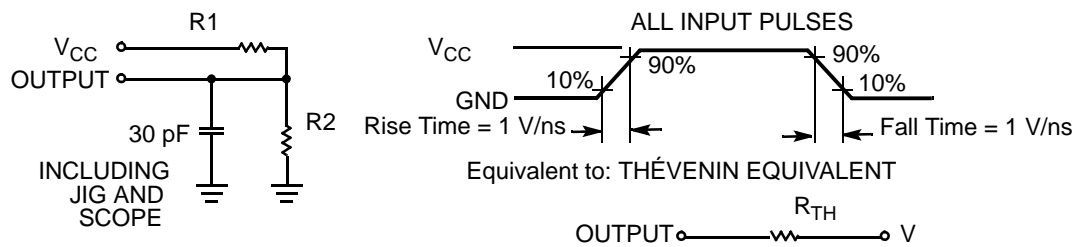
Capacitance (for all packages)^[8]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output Capacitance		10	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	TSOP II	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient) ^[8]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	77	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case) ^[8]		10	13	°C/W

AC Test Loads and Waveforms

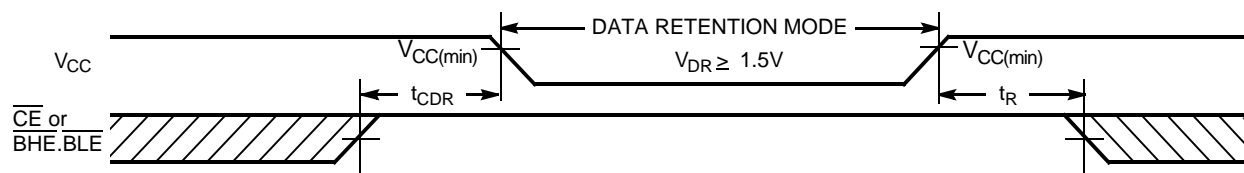


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[7]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1			V
I _{CCDR}	Data Retention Current	V _{CC} = 1V CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		0.8	3	μA
t _{CDR} ^[8]	Chip Deselect to Data Retention Time		0			ns
t _R ^[9]	Operation Recovery Time		t _{RC}			ns

Data Retention Waveform^[10]



Notes:

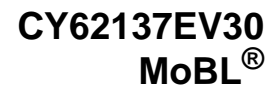
8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 100 μs or stable at V_{CC(min.)} ≥ 100 μs.

Switching Characteristics Over the Operating Range ^[11]

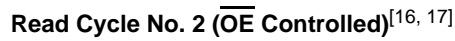
Parameter	Description	45 ns		Unit
		Min.	Max.	
Read Cycle				
t _{RC}	Read Cycle Time	45		ns
t _{AA}	Address to Data Valid		45	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		45	ns
t _{DOE}	\overline{OE} LOW to Data Valid		22	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[12]	5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[12, 13]		18	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[12]	10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[12, 13]		18	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		45	ns
t _{DBE}	$\overline{BLE/BHE}$ LOW to Data Valid		45	ns
t _{LZBE}	$\overline{BLE/BHE}$ LOW to Low Z ^[12]	5		ns
t _{HZBE}	$\overline{BLE/BHE}$ HIGH to HIGH Z ^[12, 13]		18	ns
Write Cycle ^[14]				
t _{WC}	Write Cycle Time	45		ns
t _{SCE}	\overline{CE} LOW to Write End	35		ns
t _{AW}	Address Set-Up to Write End	35		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-Up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	35		ns
t _{BW}	$\overline{BLE/BHE}$ LOW to Write End	35		ns
t _{SD}	Data Set-Up to Write End	25		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High-Z ^[12, 13]		18	ns
t _{LZWE}	\overline{WE} HIGH to Low-Z ^[12]	10		ns

Notes:

10. $\overline{BHE}.\overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . The chip can be deselected by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .
11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
13. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
14. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

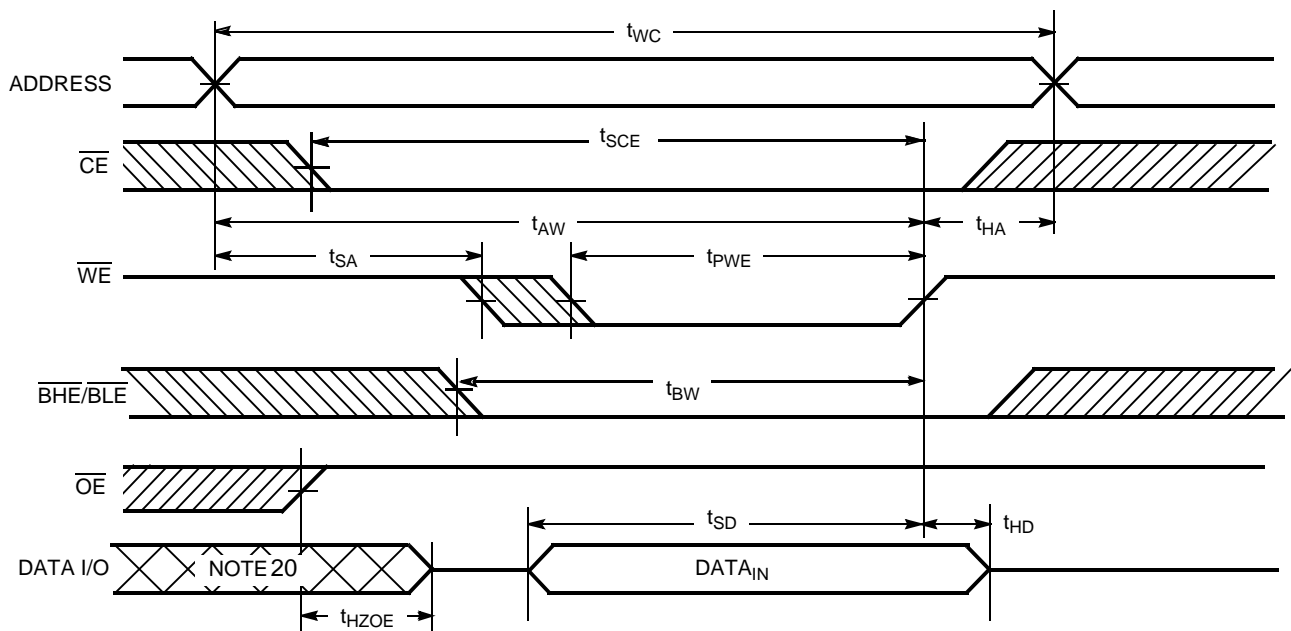


Read Cycle 1 (Address Transition Controlled)^[15, 16]

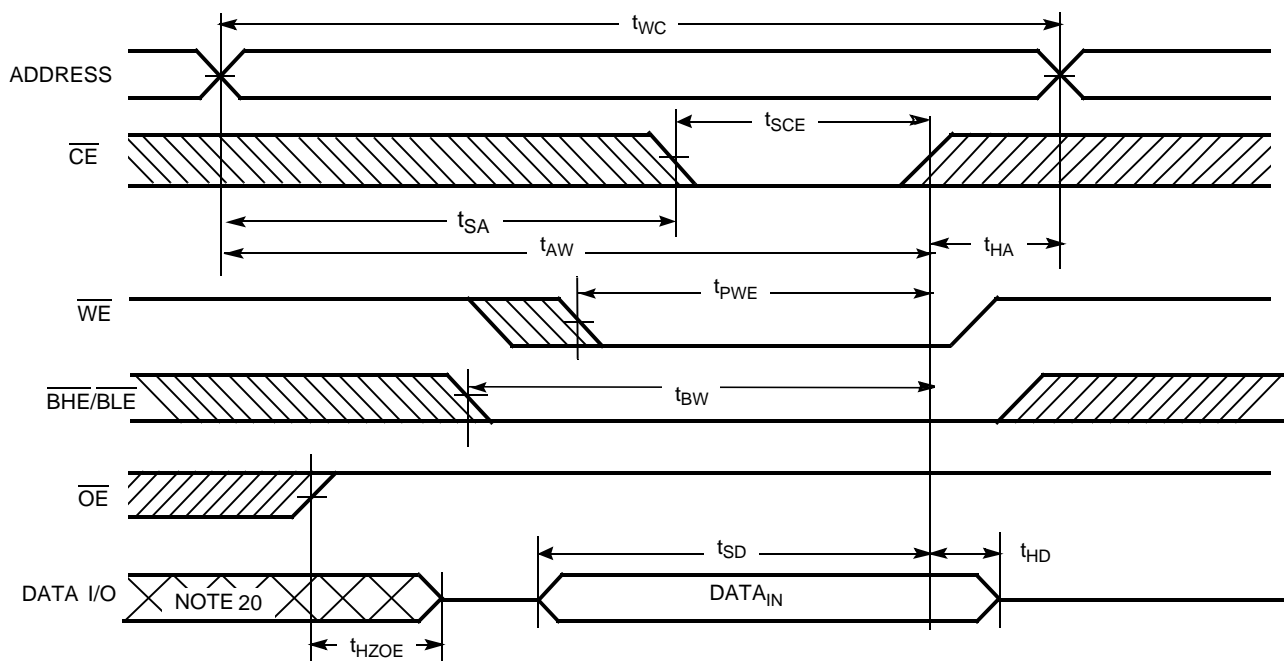


Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)^[14, 18, 19]



Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[14, 18, 19]

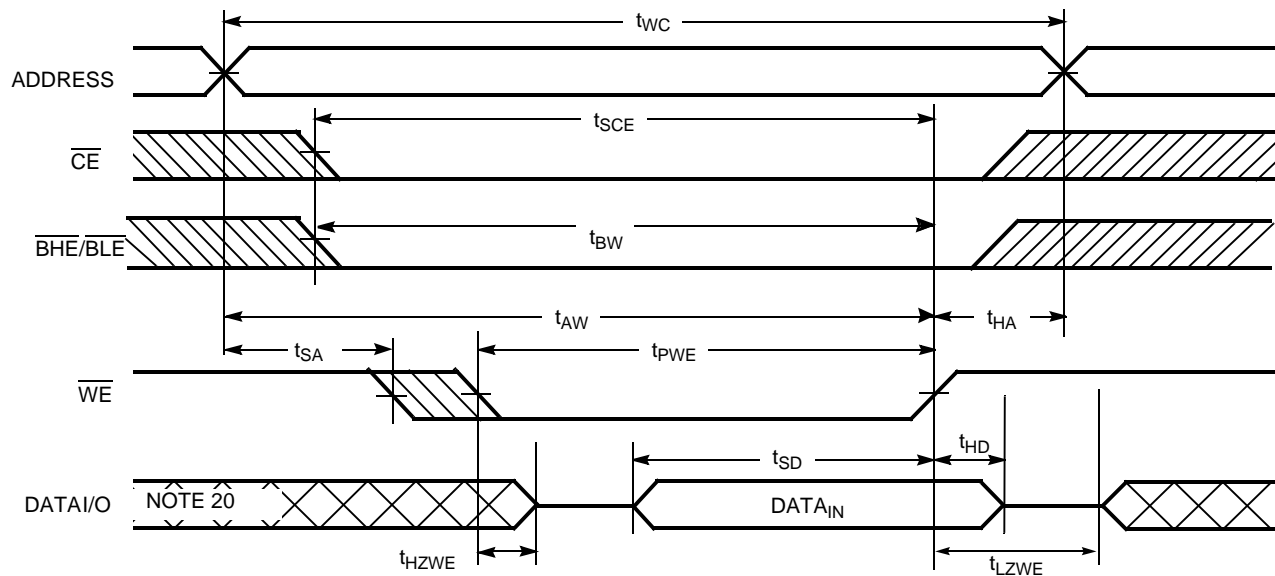


Notes:

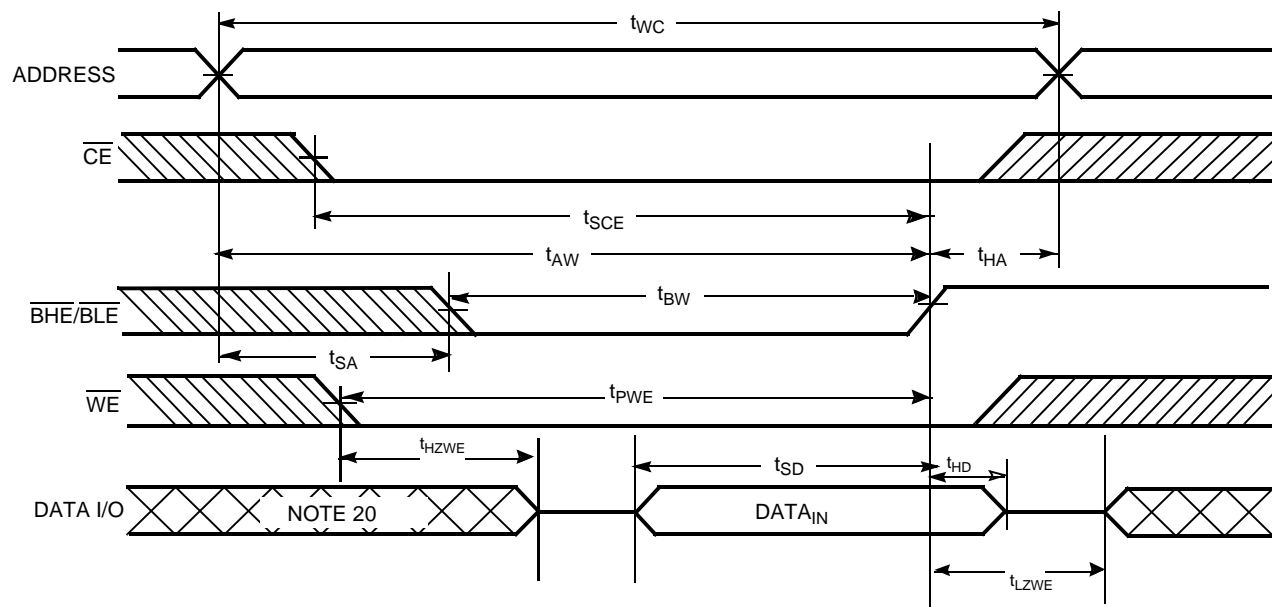
18. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
19. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\text{WE} = V_{\text{IH}}$, the output remains in a high-impedance state.
20. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[19]



Write Cycle No. 4 ($\overline{\text{BHE/BLER}}$ Controlled, $\overline{\text{OE}}$ LOW)^[19]



Truth Table

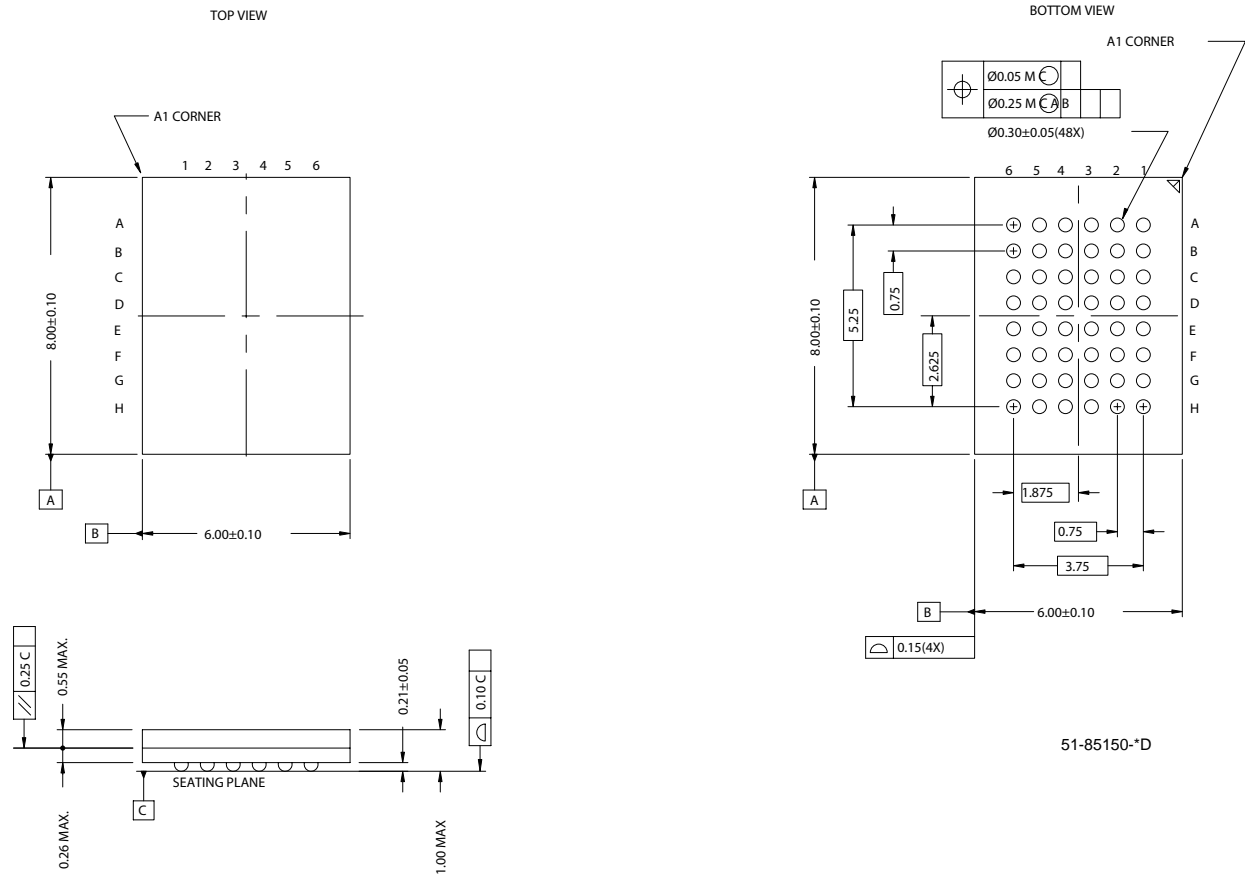
$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62137EV30LL-45BVXI	51-85150	48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	Industrial
45	CY62137EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Package Diagrams

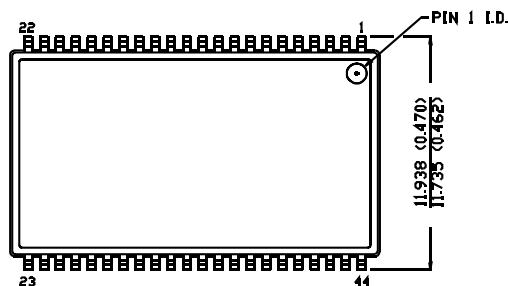
48-pin VFBGA (6 x 8 x 1 mm) (51-85150)



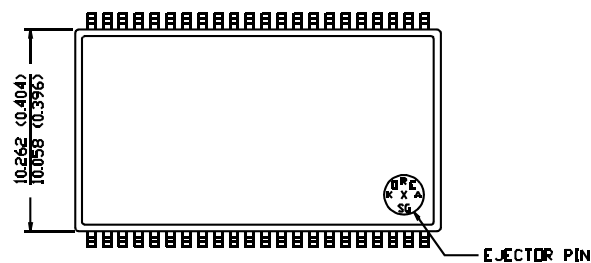
Package Diagrams (continued)

44-Pin TSOP II (51-85087)

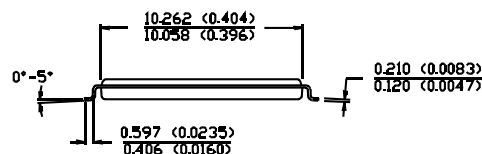
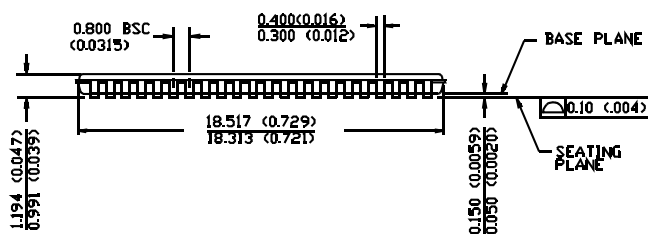
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-*A

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Document History Page

Document Title: CY62137EV30 MoBL® 2-Mbit (128K x 16) Static RAM Document Number: 38-05443				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	203720	See ECN	AJU	New Data Sheet
*A	234196	See ECN	AJU	<p>Changed I_{CC} MAX at $f=1\text{MHz}$ from 1.7 mA to 2.0 mA</p> <p>Changed I_{CC} TYP from 12 mA (35 ns speed bin) and 10 mA (45 ns speed bin) to 15 mA and 12 mA respectively</p> <p>Changed I_{CC} MAX from 20 mA (35 ns speed bin) and 15 mA (45 ns speed bin) to 25 mA and 20 mA respectively</p> <p>Changed I_{SB1} and I_{SB2} TYP from 0.6 μA to 0.7 μA</p> <p>Changed I_{SB1} and I_{SB2} MAX from 1.5 μA to 2.5 μA</p> <p>Changed I_{CCDR} from 1 μA to 2 μA</p> <p>Fixed typos on TSOP II pinout:</p> <p>Pin 18-22: address lines</p> <p>Pin 23: NC</p> <p>Added Pb-free information</p>
*B	427817	See ECN	NXR	<p>Converted from Advanced Information to Final.</p> <p>Removed 35 ns Speed Bin</p> <p>Removed "L" version</p> <p>Changed ball E3 from DNU to NC.</p> <p>Removed the redundant footnote on DNU.</p> <p>Moved Product Portfolio from Page # 3 to Page #2.</p> <p>Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at $f=1\text{ MHz}$</p> <p>Changed I_{CC} (Typ) value from 12 mA to 15 mA at $f = f_{\text{max}}=1/t_{RC}$</p> <p>Changed I_{SB1} and I_{SB2} Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA.</p> <p>Changed V_{CC} stabilization time in footnote #7 from 100 μs to 200 μs</p> <p>Changed the AC test load capacitance from 50pF to 30pF on Page# 4</p> <p>Changed V_{DR} from 1.5V to 1V on Page# 4.</p> <p>Changed I_{CCDR} from 2 μA to 3 μA.</p> <p>Added I_{CCDR} typical value.</p> <p>Corrected t_R in Data Retention Characteristics from 100 μs to t_{RC} ns</p> <p>Changed t_{OHA}, t_{LZCE} and t_{LZWE} from 6 ns to 10 ns</p> <p>Changed t_{LZBE} from 6 ns to 5 ns</p> <p>Changed t_{LZOE} from 3 ns to 5 ns</p> <p>Changed t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} from 15 ns to 18 ns</p> <p>Changed t_{SCE}, t_{AW} and t_{BW} from 40 ns to 35 ns</p> <p>Changed t_{PWE} from 30 ns to 35 ns</p> <p>Changed t_{SD} from 20 ns to 25 ns</p> <p>Updated the Ordering Information table and replaced the Package Name column with Package Diagram.</p>